



SPXXHC73
SPXXHC74
SPXXHC76
SPXXHC107
SPXXHC109
SPXXHC112
SPXXHC273

Features

- Utilizes SPI's Selective Oxidation, Silicon-Gate CMOS Process.
- Speed, function and pin-out compatible to 74LS series Logic.
- High Noise Immunity.
- Low quiescent power consumption.
- Wide power supply range.
- Operates over V_{CC} range of 2.0 to 6.0 Volts.
- Symmetric current drive.
- All Inputs are fully buffered.
- All devices have Input Protection diodes to V_{CC} and ground.
- All devices have Logic Input voltage levels consistent with CMOS.

All devices contain diodes to protect inputs against damage due to high static voltages or electric fields; however, it is advised that precautions be taken not to exceed the maximum recommended input voltages. All unused inputs must be connected to an appropriate logic voltage level (either V_{CC} or GND).

54/74 Series
Flip Flops

Ordering Information

Plastic DIP, Industrial Temp Range	Ceramic DIP, Industrial Temp Range	Ceramic DIP, Military Temp Range
SP74HCXXXN	SP74HCXXXJ	SP54HCXXXJ

Absolute Maximum Ratings

Parameter	Min	Max	Units
V_{CC} DC Supply Voltage	-0.5	+7.0	V
V_I, V_O Input or Output Voltage	-0.5	$V_{CC} + 0.5$	V
I_L DC Current Per Pin Any Input or Output	—	25	mA
I_{CC} DC Current Drain, V_{CC} or GND	—	50	mA
T_S Storage Temperature	-65	+150	°C
P_D Power Dissipation (Note 1)	—	500	mW
T_L Lead Temperature (1/16" from mounting surface for 10 sec)	—	+300	°C

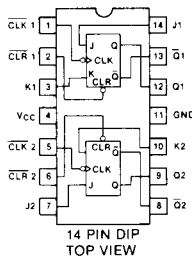
Note 1: Derate at 12mW/°C over +45 to +85°C for Plastic "N" Package.

Recommended Operating Conditions

Parameter	SP74HCXXX		SP54HCXXX		Units
	Min	Max	Min	Max	
V_{CC} DC Supply Voltage Range	2.0	6.0	2.0	6.0	V
V_I, V_O Input Voltage, Output Voltage	0	V_{CC}	0	V_{CC}	V
T_A Operating Temperature Range	-40	+85	-55	+125	°C

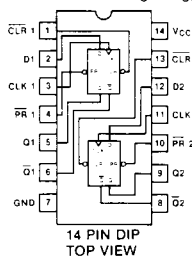
SPXXHC73

Dual J K Flip-Flops with Clear



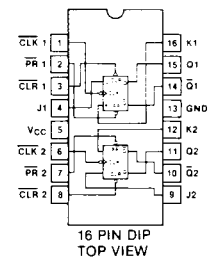
SPXXHC74

Dual D Flip-Flops with Set and Clear, Positive Edge Triggered



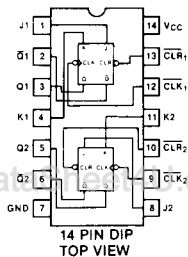
SPXXHC76

Dual J K Flip-Flops with Preset and Clear



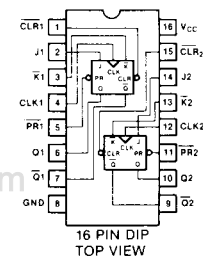
SPXXHC107

Dual J K Flip-Flops with Clear



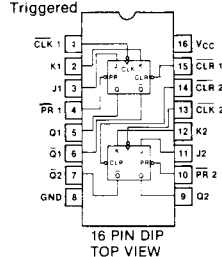
SPXXHC109

Dual J K Flip-Flops with Preset Clear, Positive Edge Triggered



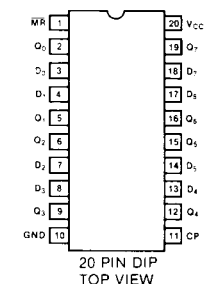
SPXXHC112

Dual J K Flip-Flops with Preset and Clear, Negative Edge Triggered



SPXXHC273

Octal D-Type Flip-Flop



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DC Electrical Characteristics

Symbol	Parameter	Conditions	V _{CC}	Typ T = 25 °C	Guaranteed Limits		Units	
					SP74HC -40 to +85 °C	SP54HC -55 to +125 °C		
V _{IH}	Minimum High Level Input Voltage	V _O = 0.1V or V _{CC} - 0.1V I _O ≤ 20 μA	2.0V		1.5	1.5	V	
			4.5V		3.15	3.15		
			6.0V		4.2	4.2		
V _{IL}	Maximum Low Level Input Voltage	V _O = 0.1V or V _{CC} - 0.1V I _O ≤ 20 μA	2.0V		0.3	0.3	V	
			4.5V		0.9	0.9		
			6.0V		1.2	1.2		
V _{OH}	Minimum High Level Output Voltage	I _{OH} = 20 μA V _I = V _{CC} or GND	2.0V	2.0	1.9	1.9	V	
			4.5V	4.5	4.4	4.4		
			6.0V	6.0	5.9	5.9		
			4.5V		3.7	3.7	V	
			6.0V		5.2	5.2		
V _{OL}	Maximum Low Level Output Voltage	I _{OL} = 20 μA V _I = V _{CC} or GND	2.0V	0	0.1	0.1	V	
			4.5V	0	0.1	0.1		
			6.0V	0	0.1	0.1		
			4.5V	0.1	0.3	0.4	V	
			6.0V		0.3	0.4		
I _{IN}	Input Leakage Current	V _I = V _{CC} or GND V _{CC} = 2.0 to 6.0V			±1.0	±1.0	μA	
I _{CC}	Maximum Quiescent Supply Current	V _I = V _{CC} or GND I _O = 0 μA	T _A = 25 °C	5.0V	0.1	2.0	2.0	μA
			T _A = 85 °C	5.0V		20.0	20.0	
			T _A = 125 °C	5.0V			40.0	

* 4ma STD outputs 6ma Bus-Drivers

AC Electrical Characteristics (V_{CC} = 5.0V, t_r = t_f = 6ns, T_A = 25 °C, unless otherwise specified)

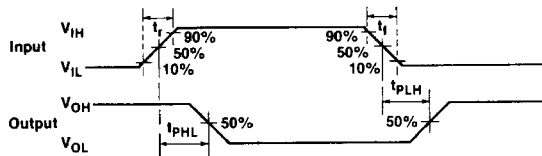
Device Type	Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
73	t _{PHL} , t _{PLH}	Clock to Q	C _L = 15pF	15		ns
			C _L = 50pF	17		
	t _{PHL} , t _{PLH}	Clock to Q	C _L = 15pF C _L = 50pF	17 19		ns
	t _w	Min. Clock Pulse Width Low		10		ns
	t _w	Min. Set Pulse Width High		10		ns
	f _{max}	Maximum Clock Frequency		40		MHz
	C _{in}	Input Capacitance		2		pF
74, 273	t _{PHL} , t _{PLH}	Clock to Q	C _L = 15pF	18		ns
			C _L = 50pF	20		
	t _{PHL} , t _{PLH}	Set/Reset to Q	C _L = 15pF C _L = 50pF	20 22		ns
	t _w	Minimum Clock Pulse Width		8		ns
	f _{max}	Maximum Clock Frequency		40		Mhz
	C _{in}	Input Capacitance		2		pF
	76	t _{PHL} , t _{PLH}	Clock to Q	C _L = 15pF	19	
C _L = 50pF				21		
t _{PHL} , t _{PLH}		Clock to Q	C _L = 15pF C _L = 50pF	19 21		ns
t _{PHL} , t _{PLH}		Set to Q	C _L = 15pF C _L = 50pF	23 25		ns
t _w		Minimum Clock Pulse Width		7		ns
f _{max}		Maximum Clock Frequency		10		MHz
C _{in}		Input Capacitance		2		pF
107	t _{PHL} , t _{PLH}	Clock to Q	C _L = 15pF	20		ns
			C _L = 50pF	22		
	t _{PHL} , t _{PLH}	Reset to Q	C _L = 15pF C _L = 50pF	25 27		ns
	f _{max}	Maximum Clock Frequency		50		Mhz
	C _{in}	Input Capacitance		2		pF

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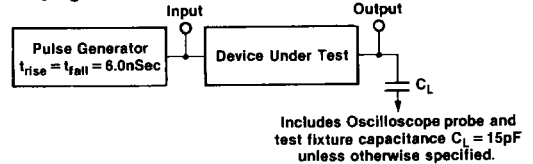
AC Electrical Characteristics ($V_{CC} = 5.0V$, $t_r = t_f = 6ns$, $T_A = 25^\circ C$, unless otherwise specified) CONTINUED

Device Type	Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units	
109	t_{PHL} , t_{PLH}	Clock to Q	$C_L = 15pF$	16		ns	
			$C_L = 50pF$	18			
	t_{PHL} , t_{PLH}	Clock to \bar{Q}	$C_L = 15pF$	15		ns	
			$C_L = 50pF$	17			
	t_{PHL} , t_{PLH}	Set to Q	$C_L = 15pF$	21		ns	
			$C_L = 50pF$	23			
	t_{PHL} , t_{PLH}	Clear to Q	$C_L = 15pF$	20		ns	
			$C_L = 50pF$	22			
t_w	Minimum Clock Pulse Width			6		ns	
t_w	Minimum Set Pulse Width			14		ns	
f_{max}	Maximum Clock Frequency			40		MHz	
C_{in}	Input Capacitance			2		pF	
112	t_{PHL} , t_{PLH}	Clock to Q	$C_L = 15pF$	16		ns	
			$C_L = 50pF$	18			
	t_{PHL} , t_{PLH}	\bar{SD} to Q	$C_L = 15pF$	19		ns	
			$C_L = 50pF$	21			
	t_{PHL} , t_{PLH}	RD to Q	$C_L = 15pF$	20		ns	
			$C_L = 50pF$	22			
	t_w	Minimum Clock Pulse Width			8		ns
	f_{max}	Maximum Clock Frequency			40		MHz
C_{in}	Input Capacitance			2		pF	

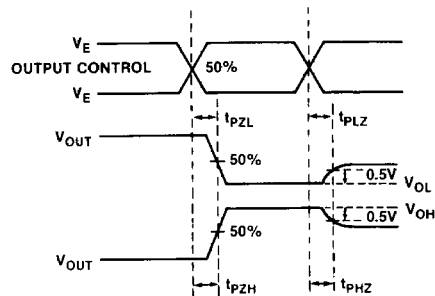
AC Waveforms



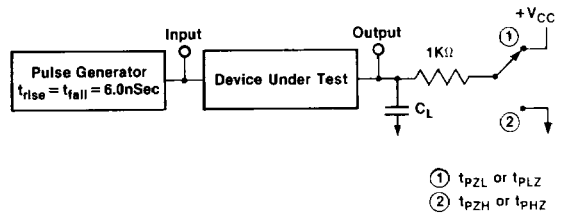
Propagation Time Test Circuit



Voltage Waveforms Enable & Disable Times, 3-State Outputs



Propagation Time Test Circuit Normal Output Devices



Mode Select and Truth Table Information

HC73

Operating Mode	Inputs				Outputs	
	\bar{R}_D	CP (d)	J	K	Q	\bar{Q}
Asynchronous Reset (Clear)	L	X	X	X	L	H
Toggle	H		h	h	\bar{q}	q
Load "0" (Reset)	H		l	h	L	H
Load "1" (Set)	H		h	l	H	L
Hold "no change"	H		l	l	q	\bar{q}

HC74

Operating Mode	Inputs				Outputs	
	\bar{S}_D	\bar{R}_D	CP	D	Q	\bar{Q}
Asynchronous Set	L	H	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	L	H
Undetermined (c)	L	L	X	X	H	H
Load "1" (Set)	H	H	↑	h	H	L
Load "0" (Reset)	H	H	↑	l	L	H

HC76

Operating Mode	Inputs					Outputs	
	\bar{S}_D	\bar{R}_D	CP (d)	J	K	Q	\bar{Q}
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined (c)	L	L	X	X	X	H	H
Toggle	H	H		h	h	\bar{q}	q
Load "0" (Reset)	H	H		l	h	L	H
Load "1" (Set)	H	H		h	l	H	L
Hold "no change"	H	H		l	l	q	\bar{q}

HC107

Operating Mode	Inputs				Outputs	
	\bar{R}_D	CP (d)	J	K	Q	\bar{Q}
Asynchronous Reset (Clear)	L	X	X	X	L	H
Toggle	H		h	h	\bar{q}	q
Load "0" (Reset)	H		l	h	L	H
Load "1" (Set)	H		h	l	H	L
Hold "no change"	H		l	l	q	\bar{q}

HC109

Operating Mode	Inputs					Outputs	
	\bar{S}_D	\bar{R}_D	CP (d)	J	K	Q	\bar{Q}
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined (c)	L	L	X	X	X	H	H
Toggle	H	H	↑	h	l	\bar{q}	q
Load "0" (Reset)	H	H	↑	l	h	L	H
Load "1" (Set)	H	H	↑	h	l	H	L
Hold "no change"	H	H	↑	l	h	q	\bar{q}

HC112

Operating Mode	Inputs					Outputs	
	\bar{S}_D	\bar{R}_D	CP (d)	J	K	Q	\bar{Q}
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined (c)	L	L	X	X	X	H	H
Toggle	H	H	↑	h	h	\bar{q}	q
Load "0" (Reset)	H	H	↓	l	h	L	H
Load "1" (Set)	H	H	↓	h	l	H	L
Hold "no change"	H	H	↓	l	l	q	\bar{q}

H = HIGH voltage level steady state.
 = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.
 L = LOW voltage level steady state.
 = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.
 q = Lower case letters indicate the state of the reference output one setup time prior to the HIGH-to-LOW Clock transition.
 x = Don't care.