

**SPXXHC113**  
**SPXXHC173**  
**SPXXHC174**  
**SPXXHC175**  
**SPXXHC374**  
**SPXXHC574**

**54/74 Series**  
**Flip Flops**

**Ordering Information**

Plastic DIP, Industrial Temp Range	Ceramic DIP, Industrial Temp Range	Ceramic DIP, Military Temp Range
SP74HCXXXN	SP74HCXXXJ	SP54HCXXXJ

**Absolute Maximum Ratings**

Parameter	Min	Max	Units
$V_{CC}$ DC Supply Voltage	-0.5	+7.0	V
$V_I, V_O$ Input or Output Voltage	-0.5	$V_{CC} + 0.5$	V
$I_L$ DC Current Per Pin Any Input or Output	—	25	mA
$I_{CC}$ DC Current Drain, $V_{CC}$ or GND	—	50	mA
$T_S$ Storage Temperature	-65	+150	°C
$P_D$ Power Dissipation (Note 1)	—	500	mW
$T_L$ Lead Temperature (1/16" from mounting surface for 10 sec)	—	+300	°C

Note 1: Derate at 12mW/°C over +45 to +85°C for Plastic "N" Package.

**Recommended Operating Conditions**

Parameter	SP74HCXXX		SP54HCXXX		Units
	Min	Max	Min	Max	
$V_{CC}$ DC Supply Voltage Range	2.0	6.0	2.0	6.0	V
$V_I, V_O$ Input Voltage, Output Voltage	0	$V_{CC}$	0	$V_{CC}$	V
$T_A$ Operating Temperature Range	-40	+85	-55	+125	°C

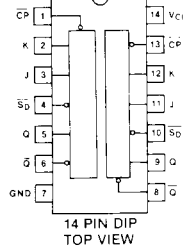
**Features**

- Utilizes SPI's Selective Oxidation, Silicon-Gate CMOS Process.
- Speed, function and pin-out compatible to 74LS series Logic.
- High Noise Immunity.
- Low quiescent power consumption.
- Wide power supply range.
- Operates over  $V_{CC}$  range of 2.0 to 6.0 Volts.
- Symmetric current drive.
- All inputs are fully buffered.
- All devices have Input Protection diodes to  $V_{CC}$  and ground.
- All devices have Logic Input voltage levels consistent with CMOS.

All devices contain diodes to protect inputs against damage due to high static voltages or electric fields; however, it is advised that precautions be taken not to exceed the maximum recommended input voltages. All unused inputs must be connected to an appropriate logic voltage level (either  $V_{CC}$  or GND).

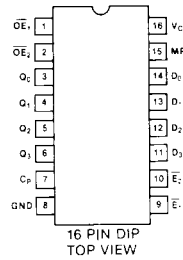
**SPXXHC113**

Dual J-K Flip-Flop with Preset, Negative-Edge Triggered



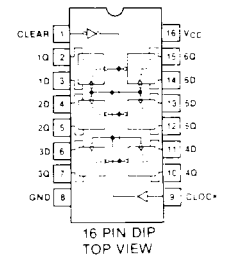
**SPXXHC173**

Quad D-Type Flip-Flop with 3-State Outputs



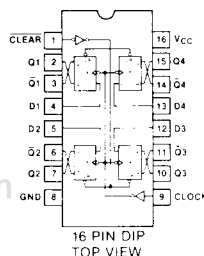
**SPXXHC174**

Hex D-Type Flip-Flops with Common Direct Clear



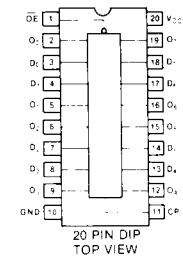
**SPXXHC175**

Quad D-Type Flip-Flops with Common Direct Clear



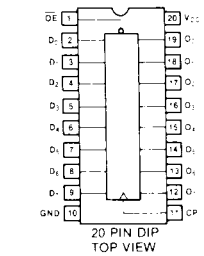
**SPXXHC374**

Octal D-Type Flip-Flop 3-State Outputs



**SPXXHC574**

Octal D-Type Flip-Flops 3-State Outputs



### DC Electrical Characteristics

Symbol	Parameter	Conditions	V <sub>CC</sub>	Typ T = 25 °C	Guaranteed Limits		Units	
					SP74HC -40 to +85 °C	SP54HC -55 to +125 °C		
V <sub>IH</sub>	Minimum High Level Input Voltage	V <sub>O</sub> = 0.1V or V <sub>CC</sub> - 0.1V I <sub>O</sub> ≤ 20 μA	2.0V		1.5	1.5	V	
			4.5V		3.15	3.15		
			6.0V		4.2	4.2		
V <sub>IL</sub>	Maximum Low Level Input Voltage	V <sub>O</sub> = 0.1V or V <sub>CC</sub> - 0.1V I <sub>O</sub> ≤ 20 μA	2.0V		0.3	0.3	V	
			4.5V		0.9	0.9		
			6.0V		1.2	1.2		
V <sub>OH</sub>	Minimum High Level Output Voltage	I <sub>OH</sub> = 20 μA V <sub>I</sub> = V <sub>CC</sub> or GND	2.0V	2.0	1.9	1.9	V	
			4.5V	4.5	4.4	4.4		
			6.0V	6.0	5.9	5.9		
			4.5V	*	3.7	3.7	V	
			6.0V	V <sub>I</sub> = V <sub>CC</sub> or GND	5.2	5.2		
V <sub>OL</sub>	Maximum Low Level Output Voltage	I <sub>OL</sub> = 20 μA V <sub>I</sub> = V <sub>CC</sub> or GND	2.0V	0	0.1	0.1	V	
			4.5V	0	0.1	0.1		
			6.0V	0	0.1	0.1		
			4.5V	*	0.3	0.4	V	
			6.0V	V <sub>I</sub> = V <sub>CC</sub> or GND	0.3	0.4		
I <sub>IN</sub>	Input Leakage Current	V <sub>I</sub> = V <sub>CC</sub> or GND V <sub>CC</sub> = 2.0 to 6.0V			± 1.0	± 1.0	μA	
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>I</sub> = V <sub>CC</sub> or GND I <sub>O</sub> = 0 μA	T <sub>A</sub> = 25 °C	5.0V	0.1	2.0	2.0	μA
			T <sub>A</sub> = 85 °C	5.0V		20.0	20.0	
			T <sub>A</sub> = 125 °C	5.0V			40.0	
I <sub>OZH</sub> I <sub>OZL</sub>	Output Off Current	V <sub>OUT</sub> = V <sub>CC</sub> or GND	T <sub>A</sub> = 25 °C	5.0V	0.1	1.0	1.0	μA
			T <sub>A</sub> = 85 °C	5.0V		5.0	5.0	
			T <sub>A</sub> = 125 °C	5.0V			10.0	

\* 4ma STD outputs 6ma Bus-Drivers

### AC Electrical Characteristics (V<sub>CC</sub> = 5.0V, t<sub>r</sub> = t<sub>f</sub> = 6ns, T<sub>A</sub> = 25 °C, unless otherwise specified)

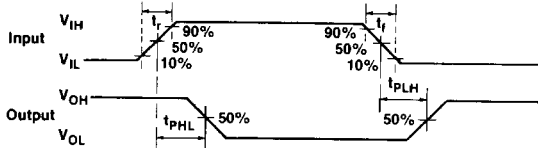
Device Type	Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
113	t <sub>PHL</sub> , t <sub>PLH</sub>	Clock to Q <sub>A</sub>	C <sub>L</sub> = 15pF	24		ns
			C <sub>L</sub> = 50pF	26		
	t <sub>PHL</sub> , t <sub>PLH</sub>	Clock to $\bar{Q}_A$	C <sub>L</sub> = 15pF	22		ns
			C <sub>L</sub> = 50pF	24		
	t <sub>PHL</sub> , t <sub>PLH</sub>	Clock to Q <sub>B</sub>	C <sub>L</sub> = 15pF	22		ns
			C <sub>L</sub> = 50pF	24		
	t <sub>PHL</sub> , t <sub>PLH</sub>	Clock to $\bar{Q}_B$	C <sub>L</sub> = 15pF	22		ns
			C <sub>L</sub> = 50pF	24		
	t <sub>w</sub>	Minimum Clock Pulse Width		7		ns
	t <sub>w</sub>	Minimum Set Pulse Width		8		ns
f <sub>max</sub>	Maximum Clock Frequency		40		MHz	
C <sub>in</sub>	Input Capacitance		2		pF	
173	t <sub>PHL</sub> , t <sub>PLH</sub>	Clock to Q	C <sub>L</sub> = 15pF	23		ns
			C <sub>L</sub> = 50pF	25		
	t <sub>w</sub>	Minimum Clock Pulse Width		10		ns
	f <sub>max</sub>	Maximum Clock Frequency		50		MHz
	C <sub>in</sub>	Input Capacitance		2		pF
174	t <sub>PHL</sub> , t <sub>PLH</sub>	Clock to Output	C <sub>L</sub> = 15pF	25		ns
			C <sub>L</sub> = 50pF	27		
	t <sub>PHL</sub> , t <sub>PLH</sub>	MR to Output	C <sub>L</sub> = 15pF	25		ns
			C <sub>L</sub> = 50pF	27		
	t <sub>w</sub>	Minimum Clock Pulse Width		9		ns
	t <sub>w</sub>	Minimum MR Pulse Width		8		ns
	f <sub>max</sub>	Maximum Clock Frequency		40		MHz
	C <sub>in</sub>	Input Capacitance		2		pF

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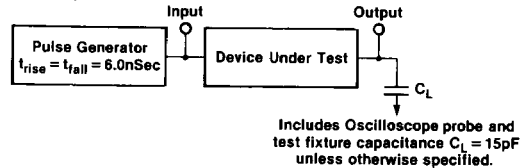
### AC Electrical Characteristics ( $V_{CC} = 5.0V$ , $t_r = t_f = 6ns$ , $T_A = 25^\circ C$ , unless otherwise specified) CONTINUED

Device Type	Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
175	$t_{PHL}$ , $t_{PLH}$	Clock to Q	$C_L = 15pF$	18		ns
			$C_L = 50pF$	21		
	$t_{PHL}$ , $t_{PLH}$	MR to Q	$C_L = 15pF$	15		ns
			$C_L = 50pF$	18		
	$t_{PHL}$ , $t_{PLH}$	MR to $\bar{Q}$	$C_L = 15pF$	20		ns
			$C_L = 50pF$	22		
		$t_w$	Minimum Clock Pulse Width		8	
	$t_w$	Minimum MR Pulse Width		7		ns
	$f_{max}$	Maximum Clock Frequency		40		Mhz
	$C_{in}$	Input Capacitance		2		pF
374	$t_{PHL}$ , $t_{PLH}$	Clock to Output	$C_L = 15pF$	23		ns
			$C_L = 50pF$	26		
	$t_{PZL}$ , $t_{PZL}$	Enable to High/Low	$C_L = 15pF$	14		ns
			$C_L = 50pF$	17		
	$t_{PHZ}$ , $t_{PLZ}$	Disable from High/Low	$C_L = 15pF$	14		ns
			$C_L = 50pF$	17		
	$f_{max}$	Maximum Clock Frequency		30		MHz
	$C_{in}$	Input Capacitance		2		pF
574	$t_{PHL}$ , $t_{PLH}$	Clock to Output	$C_L = 15pF$	17		ns
			$C_L = 50pF$	20		
	$t_{PHL}$ , $t_{PLH}$	Enable to High/Low	$C_L = 15pF$	19		ns
			$C_L = 50pF$	22		
	$t_{PHL}$ , $t_{PLH}$	Disable from High/Low	$C_L = 15pF$	18		ns
			$C_L = 50pF$	21		
	$f_{max}$	Maximum Clock Frequency		30		MHz
	$C_{in}$	Input Capacitance		2		pF

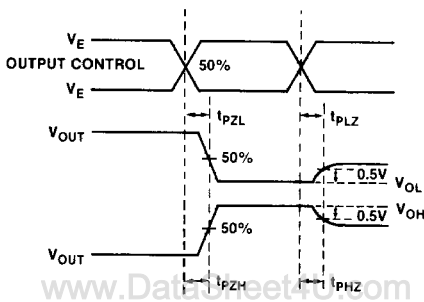
#### AC Waveforms



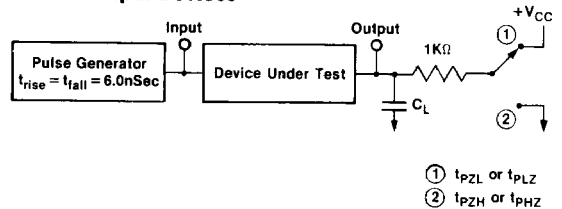
#### Propagation Time Test Circuit



#### Voltage Waveforms Enable & Disable Times, 3-State Outputs



#### Propagation Time Test Circuit 3-State Output Devices



## Mode Select and Function Tables

### HC113

Operating Mode	Inputs				Outputs	
	$\overline{S_D}$	CP	J	K	Q	$\overline{Q}$
Asynchronous Set	L	X	X	X	H	L
Toggle	H	↓	h	h	$\overline{q}$	q
Load "0" (Reset)	H	↓	l	h	L	H
Load "1" (Set)	H	↓	h	l	H	L
Hold "no change"	H	↓	l	l	q	$\overline{q}$

### HC173

Register Operating Modes	Inputs					Outputs
	MR	CP	$\overline{E_1}$	$\overline{E_2}$	$\overline{D_n}$	$Q_n$ (Register)
Reset (clear)	H	X	X	X	X	L
Parallel Load	L	↑	l	l	l	L
	L	↑	l	l	h	H
Hold (No change)	L	X	h	X	X	$q_n$
	L	X	X	h	X	$q_n$

### HC173

3-State Buffer Operating Modes	Inputs			Outputs	
	$Q_n$ (Register)	$\overline{OE_1}$	$\overline{OE_2}$	$Q_0, Q_1, Q_2, Q_3$	
Read	L	L	L	L	L
	H	L	L	L	H
Disabled	X	H	X	(Z)	(Z)
	X	X	H	(Z)	(Z)

### HC374

Operating Modes	Inputs			Internal Register	Outputs
	OE	CP	$\overline{D_n}$		$Q_0-Q_7$
Load & read register	l	↑	l	L	L
	L	↑	h	H	H
Load register & disable outputs	H	↑	l	L	(Z)
	H	↑	h	H	(Z)

### HC174

Operating Mode	Inputs			Outputs
	MR	CP	$\overline{D_n}$	$Q_n$
Reset (clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

### HC17

Operating Mode	Inputs			Outputs	
	MR	CP	$\overline{D_n}$	$Q_n$	$\overline{Q_n}$
Reset (clear)	L	X	X	L	H
Load "1"	H	↑	h	H	L
Load "0"	H	↑	l	L	H

H = HIGH voltage level.

h = HIGH voltage level one setup time prior to the LOW to HIGH clock transition.

L = LOW voltage level.

l = LOW voltage level one setup time prior to the LOW to HIGH clock transition

(Z) = HIGH impedance "off" state.

↑ = LOW to HIGH clock transition.