SPXXHC80
SPXXHC82
SPXXHC298

54/74 Series Adders/Registers

Features

- Utilizes SPI's Selective Oxidation, Silicon-Gate CMOS Process.
- Speed, function and pin-out compatible to 74LS series Logic.
- High Noise Immunity.
- Low quiescent power consumption.
- Wide power supply range.
- Operates over V_{CC} range of 2.0 to 6.0 Volts.
- Symmetric current drive.
- All Inputs are fully buffered.
- All devices have Input Protection diodes to V_{CC} and ground.
- All devices have Logic Input voltage levels consistent with CMOS.

All devices contain diodes to protect inputs against damage due to high static voltages or electric fields; however, it is advised that precautions be taken not to exceed the maximum recommended input voltages. All unused inputs must be connected to an appropriate logic voltage level (either V_{CC} or GND).

Ordering Information

Plastic DIP, Industrial Temp Range	Ceramic DIP, Industrial Temp Range	Ceramic DIP, Military Temp Range
SP74HCXXXN	SP74HCXXXJ	SP54HCXXXJ

Absolute Maximum Ratings

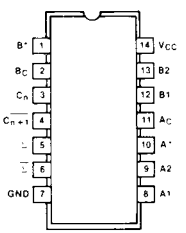
	Parameter	Min	Max	Units
V_{CC}	DC Supply Voltage	−0.5	+7.0	V
V_I, V_O	Input or Output Voltage	−0.5	V_{CC} +0.5	V
I_L	DC Current Per Pin Any Input or Output	—	25	mA
I_{CC}	DC Current Drain, V_{CC} or GND	—	50	mA
T_S	Storage Temperature	−65	+150	°C
P_D	Power Dissipation (Note 1)	—	500	mW
T_L	Lead Temperature (1/16" from mounting surface for 10 sec)	—	+300	°C

Note 1: Derate at 12mW/°C over +45 to +85°C for Plastic "N" Package.

Recommended Operating Conditions

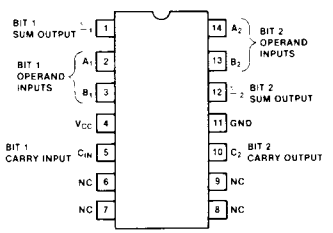
		SP74HCXXX		SP54HCXXX		
	Parameter	Min	Max	Min	Max	Units
V_{CC}	DC Supply Voltage Range	2.0	6.0	2.0	6.0	V
V_I, V_O	Input Voltage, Output Voltage	0	V_{CC}	0	V_{CC}	V
T_A	Operating Temperature Range	−40	+85	−55	+125	°C

SPXXHC80
Gated Full Adder



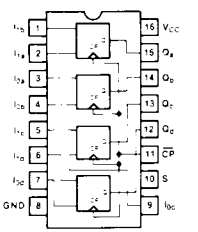
14 PIN DIP
TOP VIEW

SPXXHC82
2-Bit Full Adder



14 PIN DIP
TOP VIEW

SPXXHC298
Quad 2-Port Register



16 PIN DIP
TOP VIEW

DC Electrical Characteristics

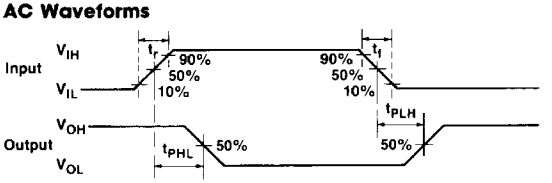
Symbol	Parameter	Conditions	V_{CC}	Typ T = 25 °C	Guaranteed Limits SP74HC −40 to +85 °C	Guaranteed Limits SP54HC −55 to +125 °C	Units
V_{IH}	Minimum High Level Input Voltage	V_O = 0.1V or V_{CC} − 0.1V $I_O \leq 20\ \mu A$	2.0V		1.5	1.5	V
			4.5V		3.15	3.15	
			6.0V		4.2	4.2	
V_{IL}	Maximum Low Level Input Voltage	V_O = 0.1V or V_{CC} − 0.1V $I_O \leq 20\ \mu A$	2.0V		0.3	0.3	V
			4.5V		0.9	0.9	
			6.0V		1.2	1.2	
V_{OH}	Minimum High Level Output Voltage	$I_{OH} = 20\ \mu A$ $V_I = V_{CC}$ or GND	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	
			6.0V	6.0	5.9	5.9	
		I_{OH} = * $V_I = V_{CC}$ or GND	4.5V		3.7	3.7	V
			6.0V		5.2	5.2	
V_{OL}	Maximum Low Level Output Voltage	$I_{OL} = 20\ \mu A$ $V_I = V_{CC}$ or GND	2.0V	0	0.1	0.1	V
			4.5V	0	0.1	0.1	
			6.0V	0	0.1	0.1	
		I_{OL} = * $V_I = V_{CC}$ or GND	4.5V	0.1	0.3	0.4	V
			6.0V		0.3	0.4	
I_{IN}	Input Leakage Current	$V_I = V_{CC}$ or GND V_{CC} = 2.0 to 6.0V			±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_I = V_{CC}$ or GND T_A = 25 °C $I_O = 0\ \mu A$ T_A = 85 °C	5.0V	0.1	2.0	2.0	μA
		T_A = 125 °C	5.0V		20.0	20.0	
			5.0V			40.0	

* 4ma STD outputs 6ma Bus-Drivers

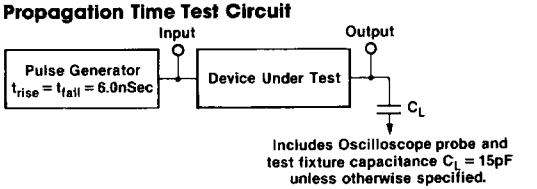
AC Electrical Characteristics (V_{CC} = 5.0V, $t_r = t_f$ = 6ns, T_A = 25 °C, unless otherwise specified)

Device Typ	Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
80	t_{PHL}, t_{PLH}	A_C to Σ	C_L = 15pF C_L = 50pF	23 25		ns
	t_{PHL}, t_{PLH}	B_C to Σ	C_L = 15pF C_L = 50pF	33 35		ns
	t_{PHL}, t_{PLH}	B_C to C_N + 1	C_L = 15pF C_L = 50pF	22 25		ns
	t_{PHL}, t_{PLH}	C_N to C_N + 1	C_L = 15pF C_L = 50pF	19 21		ns
	C_{IN}	Input Capacitance		2		pF
82	t_{PHL}, t_{PLH}	IC_0 to Σ_1	C_L = 15pF C_L = 50pF	17 19		ns
	t_{PHL}, t_{PLH}	C_0 to Σ_2	C_L = 15pF C_L = 50pF	32 35		ns
	t_{PHL}, t_{PLH}	C_0 to C_2	C_L = 15pF C_L = 50pF	30 33		ns
	t_{PHL}, t_{PLH}	B_2 to Σ_2	C_L = 15pF C_L = 50pF	21 23		ns
	C_{IN}	Input Capacitance		2		pF
298	t_{PHL}, t_{PLH}	Clock to Q_n	C_L = 15pF C_L = 50pF	20 23		ns
	C_{IN}	Input Capacitance		2		pF

AC Waveforms



Propagation Time Test Circuit



Includes Oscilloscope probe and test fixture capacitance C_L = 15pF unless otherwise specified.