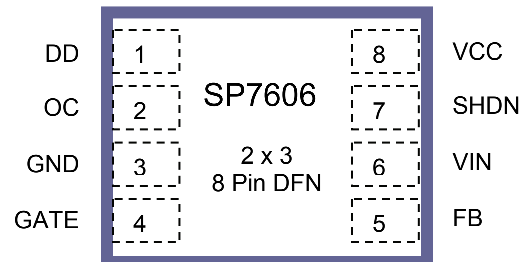
SP7606

Wide Input Voltage Boost Controller

FEATURES

- Fixed Frequency 1200kHz
  Voltage-Mode PWM Operation
- Requires Tiny Inductors and Capacitors
- Adjustable Output Voltage up to 38V
- Up to 85% Efficiency
- Internal Compensation
- Built in current limit
- Low Supply Current
- 8-pin 2x3 DFN

PINOUT



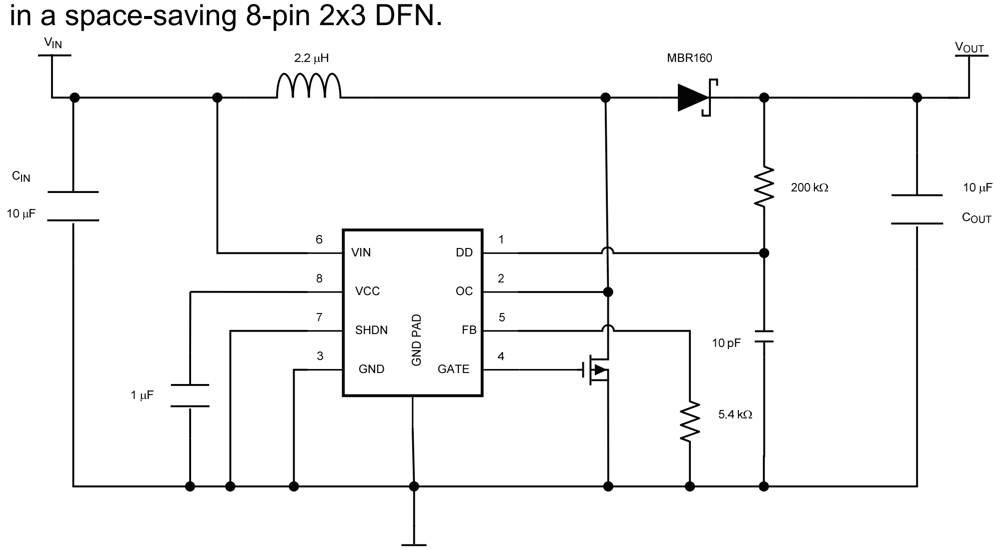
Now Available in Lead Free Packaging

APPLICATIONS

- White LED Backlighting when combined with SP7615 or SP7616
- Large LED arrays for general lighting
- General boost, flyback, or SEPIC converters

GENERAL DESCRIPTION

The SP7606 is a fixed frequency boost controller designed to drive loads up to 38V output voltage. The SP7606 was developed to be used in conjunction with the SP7616 to drive a wide range of led chains that require high anode voltages. The ability to disconnect the output voltage feedback resistors (DD Pin) reduces shutdown current. The high switching frequency allows the use of tiny external components and saves layout space and cost. The SP7606 is available in a space-saving 8-pin 2x3 DFN.



TYPICAL APPLICATION SCHEMATIC
Boost converter 12V to 30V

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Vin..-0.3V to 30V
EN, FB, SHDN, and Vcc ....-0.3V to 6V

DD, OC...0.3V to 40V
Storage Temperature................ -65°C to +150°C
Lead Temperature (Soldering, 10 sec)......300°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage (Vin)............................ 7V to 28V
Operating temperature .... $-40 \le T_J \le 125°C$
ESD Rating SHDN pin...................... 1.5KV HBM
ESD Rating all other pins .... 2KV HBM
Package Thermal Dissipation..................45°C/W

ELECTRICAL CHARACTERISTICS

Specifications are for $T_{AMB}=T_J=25°C$, and those denoted by ♦ apply over the full operating range, $-40°C \le T_J \le 125°C$

Unless otherwise specified: Vin = 7 -28V, C_{GATE} = 1000pF,

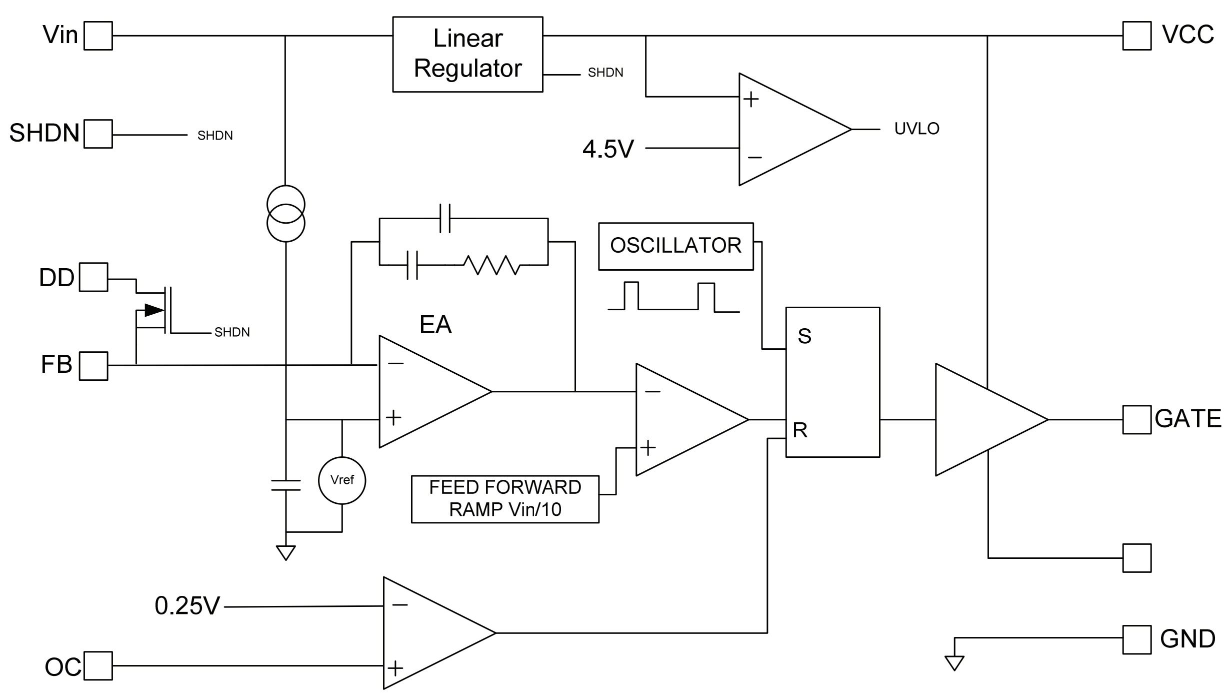
PARAMETER	MIN	TYP	MAX	UNITS	♦	CONDITIONS
Operating Input Voltage Range	7		28	V	♦	
Supply Current		2.2	4.2	mA	♦	Not switching Vin=28V
Supply current in shutdown		55	160	µA	♦	SHDN_ = HIGH
Vcc Output Voltage	4.8	5.0	5.3	V	♦	
Vcc Dropout Voltage			2	V		Icc = 20mA
Under Voltage Lockout	4.1	4.35	4.6	V	♦	
Switching Frequency	1.0	1.20	1.4	MHz		$0°C \le T_J \le 85°C$
Maximum Duty Cycle	86		91	%	♦	
Minimum On-time		30		ns		
Turn-on Time from Shutdown		200	500	µs	♦	
FB reference Voltage	784	800	816	mV	♦	
FB Input Current			0.5	µA	♦	V_{FB} = 1V
Error amplifier gain**		80		dB		
Ramp Amplitude**	1.25	Vin/10	4.2	V		
Gate Rising Time			50	ns		10 to 90%
Gate Falling Time			40			90 to 10%
Gate Pull-up Resistance		4		Ω		
Gate Pull-down Resistance		3				
Gate Pull Down Resistance in off state		50		kΩ		
SHDN Logic Low	0		.7	V	♦	Enabled
SHDN Logic High	3		5.3	V	♦	Disabled
SHDN Input Current		.01	0.5	µA		0 to Vcc
Over-Current Protection threshold	0.145	0.20	0.260	V	♦	
Over-Current Trip Point Delay			100	ns	♦	
DD FET impedance		155		Ω		

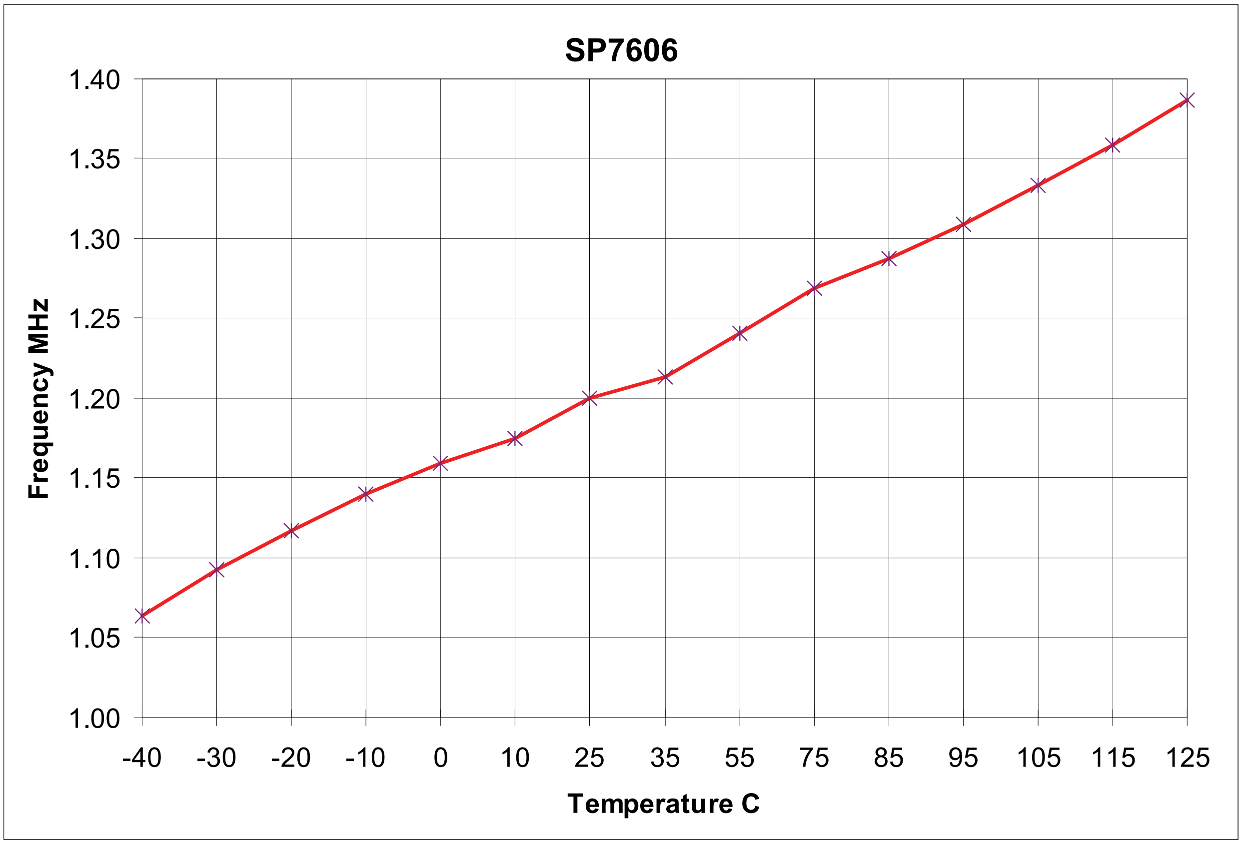
*Not tested but the specification is guaranteed by design.

PIN ASSIGNMENTS

Pin Name	Pin#	Pin Description
DD	1	Divider disconnect; Upper resistor of output voltage setting divider is connected to this point
OC	2	Over –current protection
GND	3	Ground pin
GATE	4	Gate pin. Connect external MOSFET gate to this pin. Minimize trace area to reduce EMI
Vcc	5	Internal circuit power source. Bypass Vcc to GND with 0.1μF capacitor.
SHDN	6	Shutdown pin. Device is active if SHDN is logic LOW (<0.7V)
Vin	7	Power input pin. Bypass Vin to GND with 1μF capacitor as close to Vin as possible
FB	8	Feedback pin. Reference voltage is 0.8V

BLOCK DIAGRAM





Oscillator Frequency vs Temperature

CIRCUIT DESCRIPTION THEORY OF OPERATION

The SP7606 converter is a voltage mode boost controller. The control loop has built in Type 2 compensation coupled with high switching frequency allows the user to use small components when designing the output filter. The equations below show generic relationships as applicable to the boost regulator running in discontinuous conduction mode (DCM) and continuous conduction mode (CCM) of operation.

Duty Cycle in continuous conduction mode (CCM)

$$D_{CCM} = 1 - \frac{Vin}{Vout + Vd}$$

Where

Vd= Forward voltage drop of D1

Duty Cycle in discontinuous conduction mode (DCM)

$$D_{DCM} = \sqrt{\frac{2L}{\left[\frac{Re}{fsw}\right]}}$$

Where fsw is the switching frequency
L is the inductor
Re is the effective resistance of the small signal model

Re can be found by using as follows:

$$Re = \frac{Vin^2}{Iout \cdot (Vout - Vin)}$$

Setting the output voltage

The output voltage of the SP7606 can be set by using an output voltage divider. The internal reference of this part is set to 0.8V. Due to the internal compensation, resistor R1 might need to be chosen according to the desired gain of the compensation loop. This resistor is typically between 100K and 1M ohm. Resistor R2 can be determined by:

$$Vout = Vfb \cdot \left[1 + \frac{R1 + 200}{R2}\right]$$

Vfb=800mV Feedback Voltage
R1=Top Voltage divider resistor
R2=Bottom Voltage divide resistor
200=the typical impedance of the DD FET

For typical applications resistor R1 should be connected between Vout and the DD pin. The DD pin serves as a disconnect for the output voltage divider when the SP7606 is disabled. This feature allows the user to save power when the converter is not running. The typical Impedance of the DD FET when enabled is 200 ohms. If the DD pin is not used the resistor R1 can be connected directly to the Vfb pin to get the proper output voltage. If this type of connection is used the Rdson of the DD Fet can be ignored and the equation becomes:

$$Vout = Vfb\left[1 + \frac{R1}{R2}\right]$$

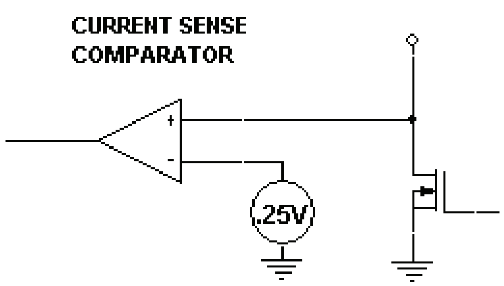
Vfb=800mV Feedback Voltage
R1=Top Voltage divider resistor
R2=Bottom Voltage divide resistor

If the DD pin is not used the converter can be used to boost voltages beyond 38V. A more detailed discussion on this topic can be found in the section “High Voltages Operation”. A 10 to 22pf decoupling capacitor from the feedback pin to ground is recommended when the SP7606 is used with resistor values above 20K in the voltage divider circuit.

Over current protection

The boost regulator topology inherently does not have short circuit protection. The SP7606 converter uses a simple comparator circuit to check for an over current condition on a pulse by pulse basis. The Vset voltage threshold for the over-current (OC) pin is set to 0.25V. Current limit set point is:

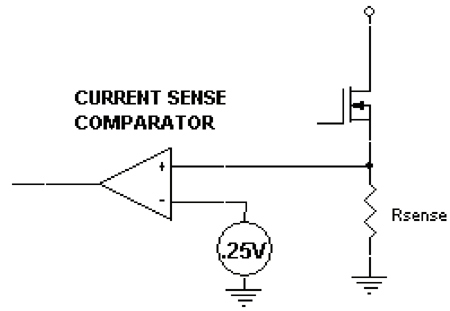
$$Iset = \frac{Vset}{RDSON}$$



Rdson current sense

Typically the converter current limit is set to about 150% of the normal output current. This allows the converter to function at maximum output current without accidentally triggering the current limit. 150% over current limit takes into effect the variations in RDSon of the FET, as well as the inductor inductance values. The accuracy of the current sensing can be increased by the use of a sense resistor. The resistor values tend to be more accurate down to 1%.

$$Iset = \frac{Vset}{Rsense}$$



Current sense using resistor

The approximate associated power loss in the resistor is:

$$Pr = Ip^2 \cdot \frac{ton}{3T} \cdot Rsense$$

Rsense=Current sense resistor

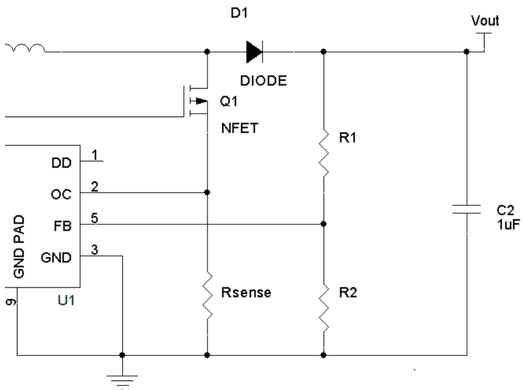
For continuous conduction mode the ton/T becomes the duty cycle of the converter. For DCM mode the value of K can be used.
The other benefit of this combination is that the OC pin does not see the high voltages and the converter can be used to generate much higher voltages then 38V. Please refer to the high output voltage operation section for a more detailed explanation.
The over current protection can be disabled by tying the OC pin to GND.

High Voltage Operation

The converter can be used to boost voltage to higher than the rated voltage of the DD pin and the OC pin. To do this two things need to be done for proper operation.

1) The voltage set resistors need to be connected directly to the Vfb pin bypassing the DD internal FET. By doing this the user can get voltages that are higher than Vout of 38V. By doing this the user does not have the output voltage disconnect feature.
2) The second thing that needs to be done is the circuit needs to use a current sense resistor for current limit. This prevents the OC pin from seeing high

switch-node voltages. The current sense resistor schematic setup is shown in Figure 2.



Schematic for High Voltage Operation

Other Topologies

The SP7606 is not only capable of driving boost regulator circuits, but can also be used in flyback and SEPIC topologies. Look for an application note in the future on EXAR's web site

Inductor selection

Typically the inductor needs to be chosen for its current capability and size. For most applications using the SP7606 the inductor should be chosen so that at light loads the inductor runs in discontinuous mode and then enters continuous mode of operation at high loads. This allows the inductor to be reasonably sized and helps with compensation of the overall circuit as well. The procedure for selecting the inductor current for discontinuous mode of operation is as follows.

1 The first thing that needs to be determined is the constant K. K represents a ratio of MOSFET conduction to diode conduction. Typically a value of 0.8 can be used, this will assure that there is about 20% dead time present to have DCM mode of operation.

2 The on time is calculated is:

$$Ton = \frac{0.8\left[\frac{1}{fsw}\right][Vo - Vinmin]}{Vo}$$

Vo is the output voltage
Vinmin is the minimum input voltage

3 The inductor inductance is:

$$L_{DCM} = \frac{K\left[\frac{Vo}{Io}\right]T_{on}}{2\cdot\left[\frac{Vo}{Vinmin}\right]^2}$$

Where
K is .8 ratio of MOSFET and diode conduction time to T (T=1/fsw)
$\frac{Vo}{Io}$= output impedance at full load.
Vo is the output voltage
Vinmin is the minimum input voltage
T_{on} is the maximum on time

4 The inductor peak current Ip is:

$$Ip_{DCM} - T_{on}\left[\frac{Vinmin}{L1}\right]$$

Although the SP7606 typical mode of operation is in DCM mode, due to easier compensation below are the formulas for when the SP7606 runs in CCM.

For continuous conduction mode the inductor current is:

$$\Delta IL_{CCM} = \frac{Vin(Vo+Vd-Vinmin)}{fsw + L\cdot(Vo+Vd)}$$

fsw is the switching frequency
Vd is forward diode drop of D1
Vo is the output voltage
Vinmin is the minimum input voltage

The approximate peak inductor current is:

$$Ip_{ccm} = Ioutmax\left(\frac{Vout}{Vin}\right) + \frac{\Delta IL}{2}$$

MOSFET selection

The MOSFET needs to be chosen based on three main criteria. The drain to source voltage needs to be higher than the output voltage of the converter. The MOSFET needs to be able to conduct the peak current that is calculated in the inductor selection section. The Rdson of the MOSFET needs to satisfy current limit criteria. Picking a MOSFET with the lowest Qg and Crss that meets the above requirement is crucial to good efficiency. At 1.2MHz the switching losses become a significant power loss in the system even compared to the Rdson of the MOSFET. For continuous conduction mode the power loss in the MOSFET is:

$$Ploss = (In\ Max)^2 \cdot D \cdot (1 + kt)Rdson + kg \cdot Vout \cdot (Iinmax) \cdot Crss \cdot fsw$$

Where In max is the maximum input current
D is the duty cycle
Vo is the output voltage
Crss reverse transfer capacitance of MOSFET
fsw is the switching frequency
kt is the temperature dependency of RDSon
kg is the constant inversely proportional to gate drive current a value of 1.5 should be used.

For discontinuous mode of operation the power loss in the FET will is similar.

$$Ploss = (Iinrms)^2 \cdot (1 + kt)Rdson + Z \cdot (Iinmax) \cdot Vout^2 \cdot Crss \cdot fsw$$

Crss reverse transfer capacitance of MOSFET
Fsw is the switching frequency
P is the temperature dependency of RDSon
Z is the constant inversely proportional to gate drive current
Where In max is the maximum input current
K is the duty cycle
Vo is the output voltage

Where Iinrms

$$Irms_{DCM} = Ip\sqrt{\frac{K}{3}}$$

The gate drive loss is associated with the FET but it actually is lost in the driver IC. Below is the formula for the gate charge loss Qg.

$$Pgateloss = Qg \cdot 5V \cdot fsw$$

5V is the gate drive voltage
Qg is the total gate charge
Fsw is the switching frequency

Input capacitor selection

For both continuous and discontinuous mode of operation the input capacitor needs to be chosen based on maximum input voltage rating and the RMS ripple current and minimum input capacitance. For DCM mode the RMS current is given by:

$$Irms_{DCM} = Ip\sqrt{\frac{K}{3}}$$

Where K is the conduction time constant
Ip is the peak inductor current

The minimum input capacitance that is required is:

$$Cin_{DCM} = Irms \cdot \frac{T - Ton}{.2 \cdot Vin}$$

Ton is the calculated on time
Vin is the minimum input voltage

For CCM of operation the input capacitor ripple current is:

$$Iinrms_{CCM} = \frac{.3 * (Vin)(Vo - Vinmin)}{Fsw \cdot (L)Vo}$$

Fsw is the switching frequency
Vo is the output voltage
Vinmin is the minimum input voltage
L inductor inductance

Output capacitor selection

For best performance a combination of both electrolytic and ceramic capacitors should be used. For both DCM and CCM mode the required ESR is approximately given by

$$ESR = \frac{\Delta Vo}{Ip}$$

For CCM mode of operation the output capacitor ripple is approximately:

$$Ioutrms = Ip\sqrt{\frac{Vout-Vin}{Vin}}$$

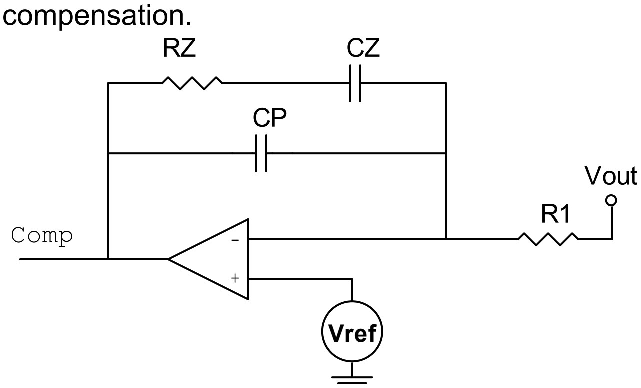
The minimum output capacitance required in CCM and DCM mode is approximated by

$$Cout \approx \frac{Ip \cdot D}{Fsw \cdot \Delta Vo}$$

Where D= duty cycle for different modes of operation
fsw=switching frequency

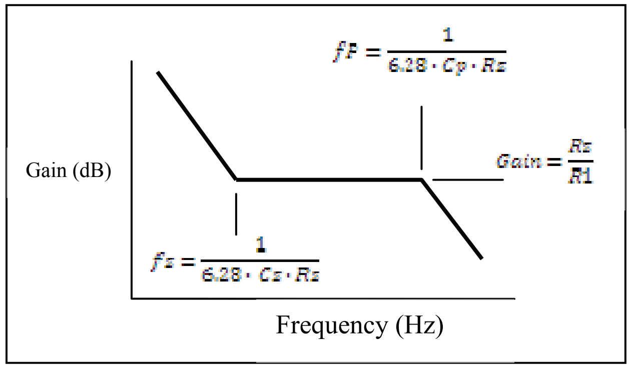
Error Amplifier

The SP7606 has built in internal Type 2 compensation.



Type II compensation

The values for Rz is 200K
Cz is 150pF
CP is 2pF
R1 is chosen for proper gain.



Bode plot of type two compensation

The internal pole and zero location for the SP7606 internal compensation is

Zero Location= 5.3KHz
Pole Location=398KHz

Modulator Gain CCM (feed forward)

The SP7606 has also built in a feed forward topology to allows the boost regulator to have the same modulator gain throughout its full input voltage range swing when running in CCM. The modulator gain is for the SP7606 is

$$Gain = \frac{10}{(1-D)^2}$$

Modulator Gain DCM (feed forward)

The SP7606 has also built in a feed forward topology to allow the boost regulator to have the same modulator gain throughout its full input voltage range swing when running in DCM. The modulator gain is for the SP7606 is

$$Gain = \left[\frac{2Vo}{D}\right]\left[\frac{M-1}{(2M)-1}\right]$$

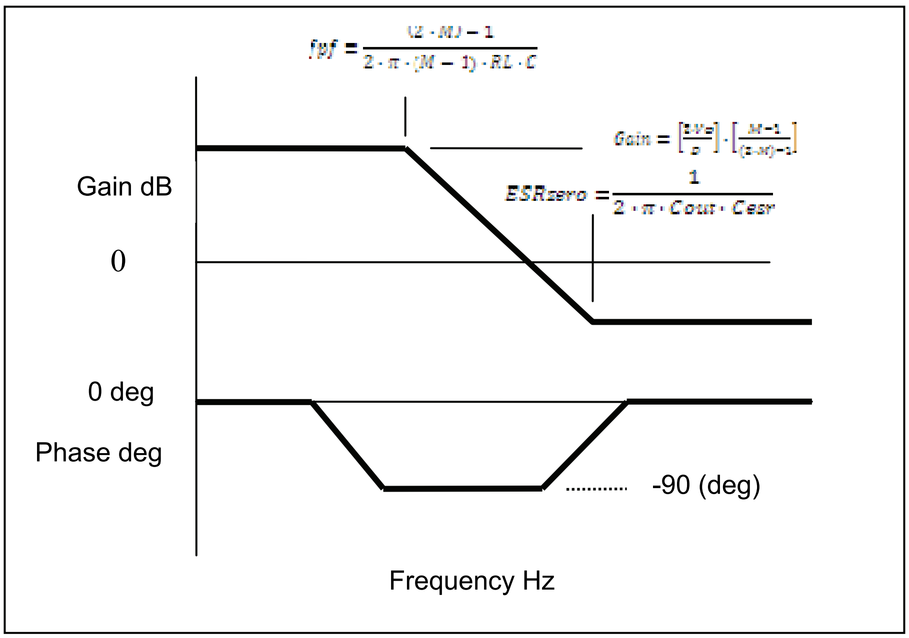
Where $M=\frac{Vout}{Vin}$
D= Duty Cycle in DCM

Boost regulator output filter DCM

When a boost regulator is running in discontinuous conduction mode the output filter characteristics are composed of a single pole and a single zero. The following equations show the location of the pole and zero for the output filter of the boost regulator.

$$fpf = \frac{(2 \cdot M) - 1}{2 \cdot \pi \cdot (M-1) \cdot RL \cdot C}$$

$$ESRzero = \frac{1}{2 \cdot \pi \cdot Cout \cdot Cesr}$$



Gain of Control to Output transfer DCM

For most applications that operate in discontinues conduction mode the internal compensation is sufficient and no external compensation is required.

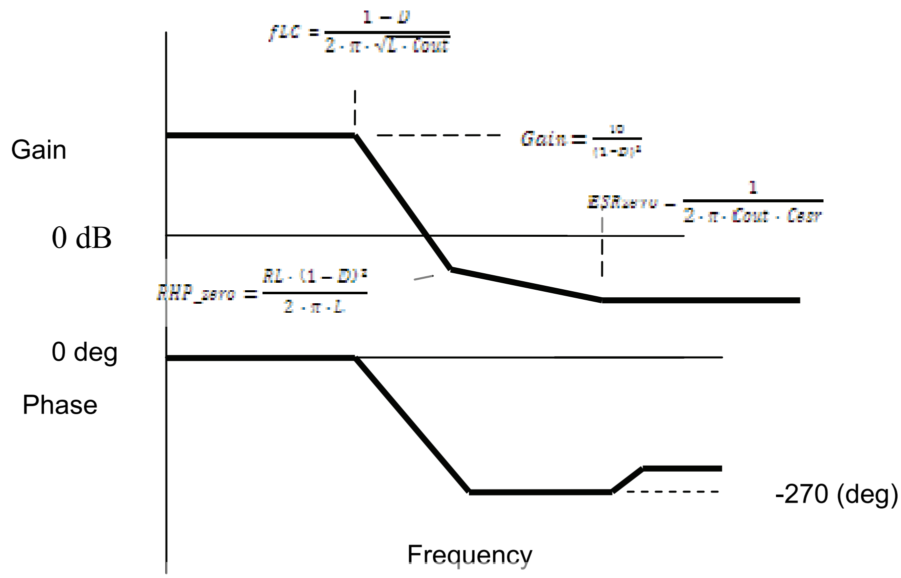
Boost regulator output filter CCM

When a boost regulator is running in continuous conduction mode the output filter characteristics are composed of a filter double pole an ESR_zero and a right half plane (RHP) zero.

$$fLC = \frac{1-D}{2 \cdot \pi \cdot \sqrt{L \cdot Cout}}$$

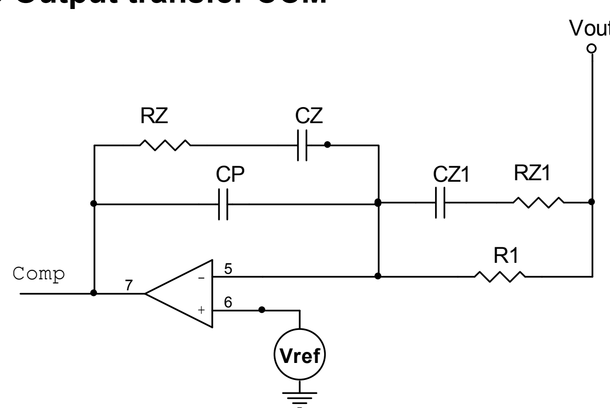
$$ESRzero = \frac{1}{2 \cdot \pi \cdot Cout \cdot Cesr}$$

$$RHP\_zero = \frac{RL(1-D)^2}{L \cdot 2 \cdot \pi}$$

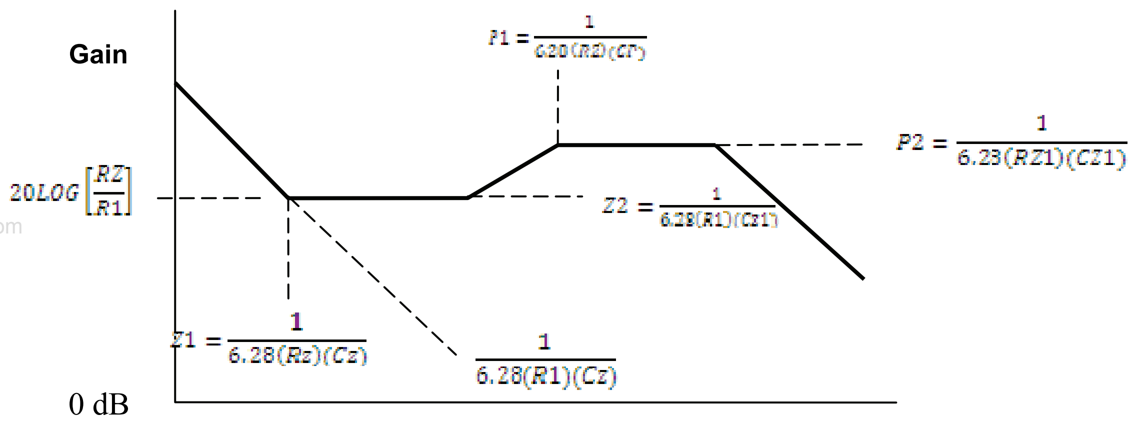


Gain of Control to Output transfer CCM

The compensation becomes much harder to accomplish when due to the RHP zero as well as the filter double pole. Unlike the DCM filter the gain drops off sharply at the filter double pole and does not recover. More over the Right Half plane zero also adds another -90 degrees to the phase. Due to the RHP zero the compensation network for a boost regulator needs to roll off below the RHP zero location. When compensating for CCM mode of operation the user will need to add a phase boost capacitor and resistor to help compensate for the filter double pole. The location of the zero and poles for Type 3 compensation is.



Error Amplifier Type 3 Compensation

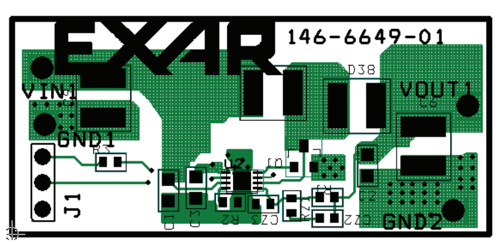


Type 3 Error amplifier Gain Plot

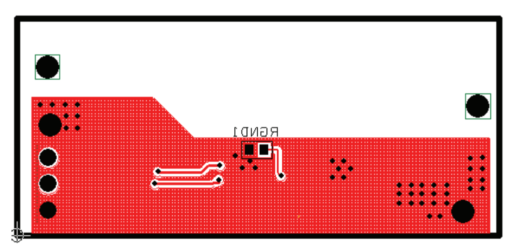
The compensation needs to be such that the Z2 phase boost zero needs to be located around the filter double pole to help offset the filter double pole. But the overall crossover frequency needs to occur below the RHP zero.

BOARD LAYOUT AND GROUNDING

To obtain the best performance from the SP7606, a printed circuit board with ground plane is required. High quality, low series resistance ceramic bypass capacitors should be used at the Vin and Vout pins (pins 1 and 8). These capacitors must be located as close to the pins as possible. The traces connecting the pins and these capacitors must be kept short and should be made as wide as possible. Below is a Typical Layout for the SP7606.

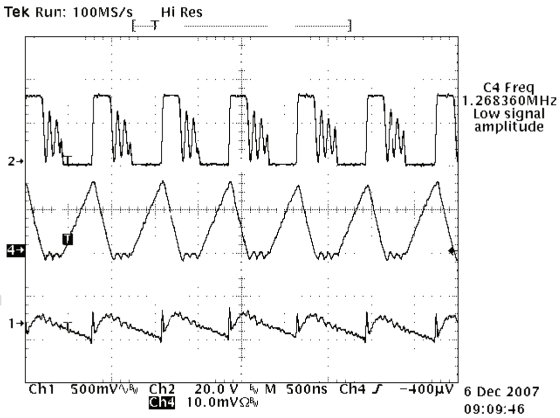


Top Side

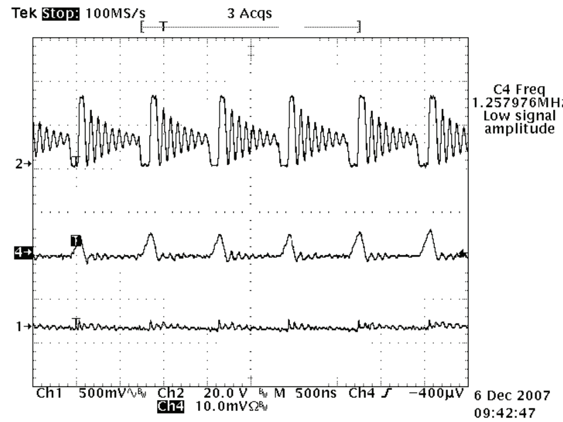


Bottom Side

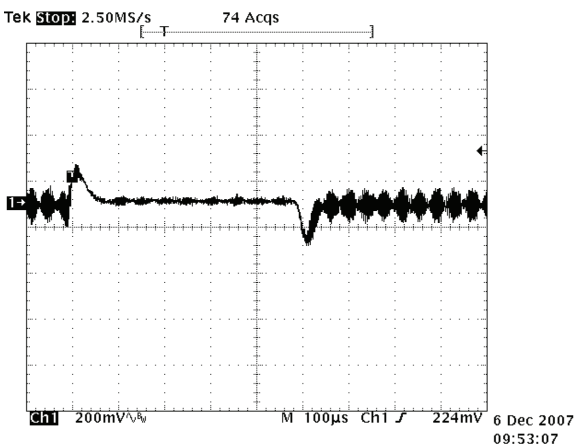
SP7606 WAVEFORMS



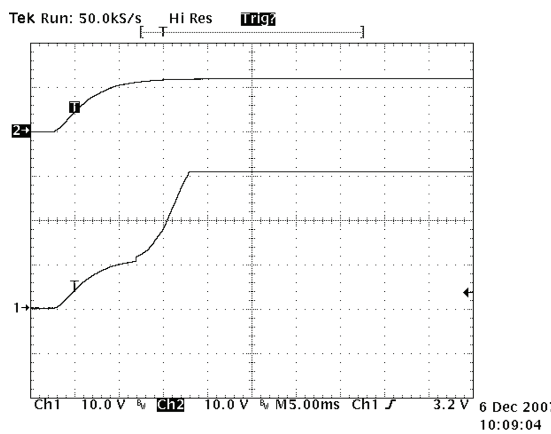
400mA Load switching characteristics 12Vin 30Vout
Channel 1 Vout Ripple
Channel 2 LX node
Channel 3 Inductor Current 2A/Div



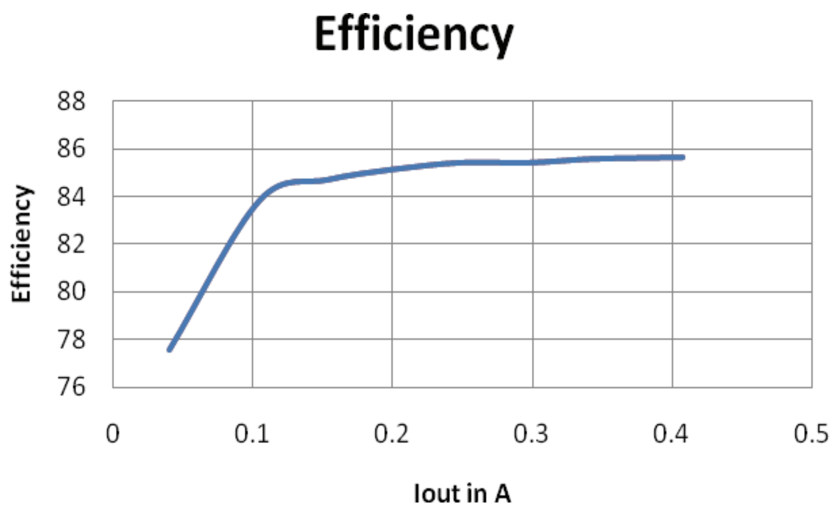
Light Load switching characteristics 12Vin 30Vout
Channel 1 Vout Ripple
Channel 2 LX node
Channel 3 Inductor Current 2A/Div



Transient Response load step
100mA to 400mA

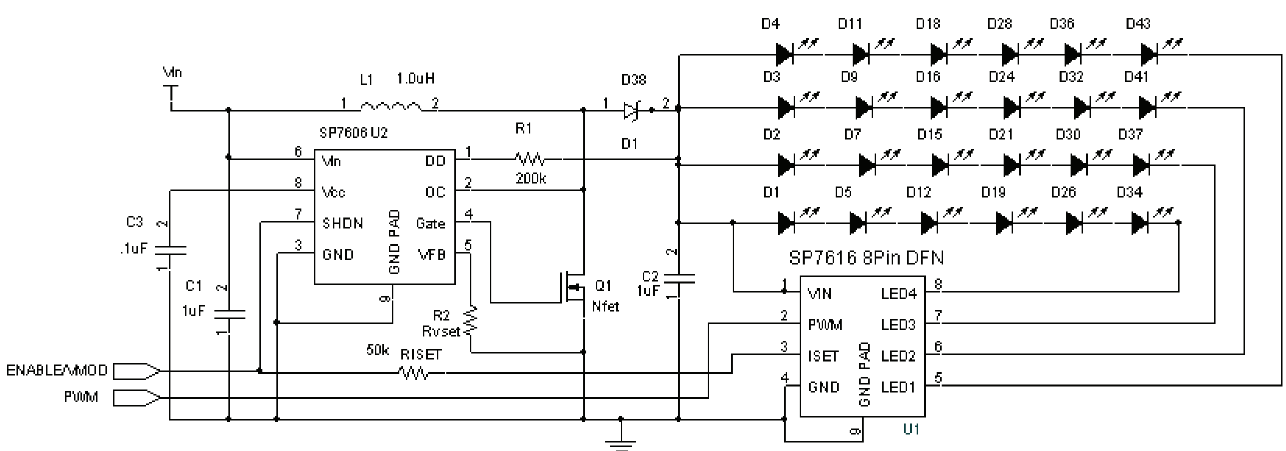


Startup characteristics into 400mA load
Channel 1 Vout Channel 2 Vin

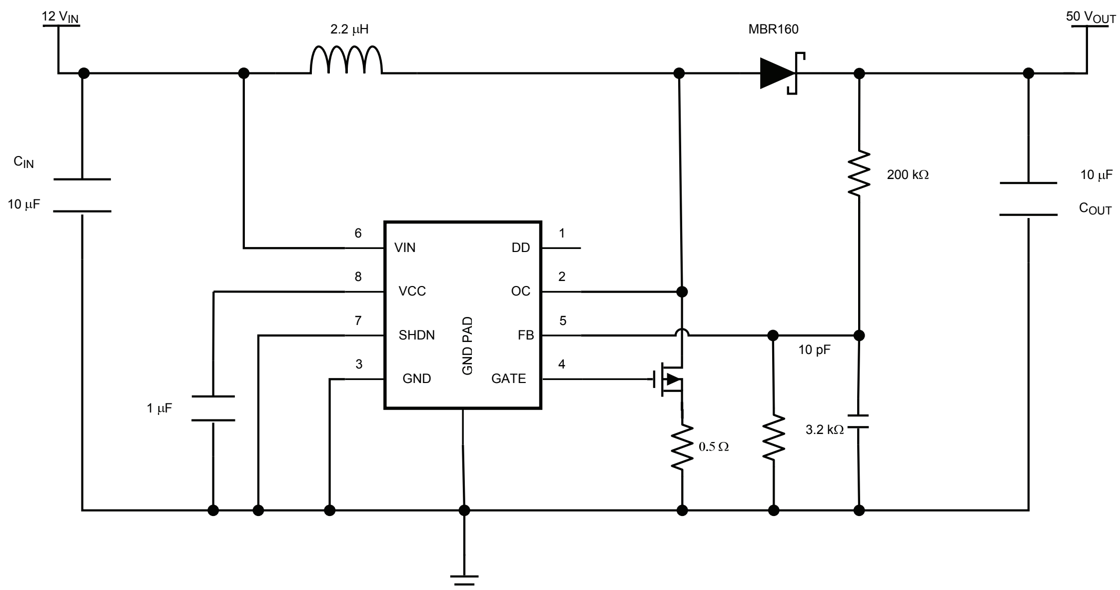


Efficiency Graph 12Vin 30Vout

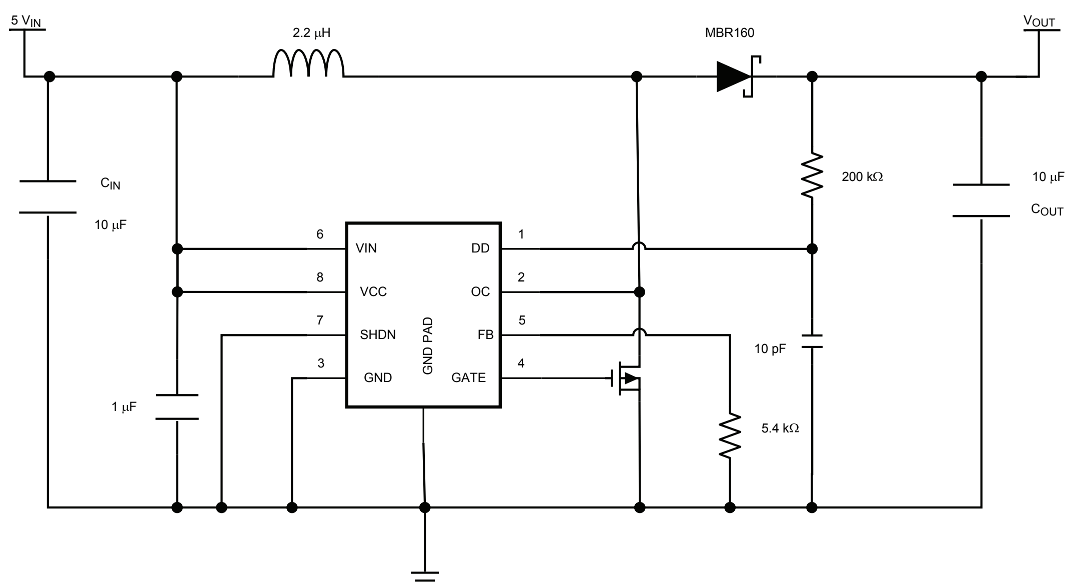
TYPICAL APPLICATIONS



Boost converter with Over Voltage/Over current Protection for LED driving

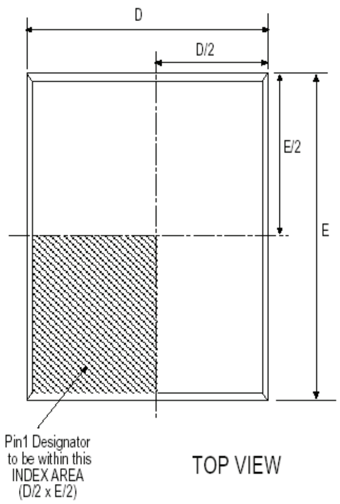


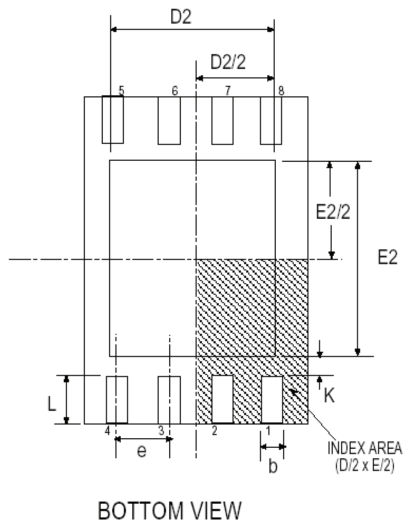
High output voltage solution

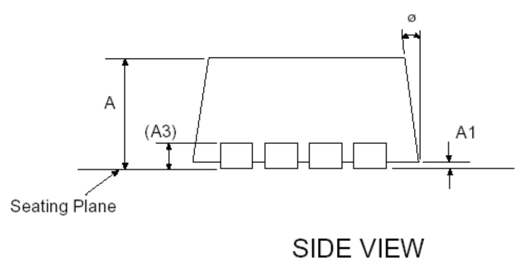


5Vin to 30Vout

8-PIN 2 x 3 mm DFN PACKAGE DIMENSIONS







2x3 8 Pin DFN	JEDEC MO-229			VARIATION VCED-2		
SYMBOL	Dimensions in Millimeters: Controlling Dimension			Dimensions in Inches Conversion Factor: 1 Inch = 25.40 mm		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.036	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
K	0.20	-	-	0.008	-	-
ø	0º	-	14º	0º	-	14º
b	0.18	0.25	0.30	0.008	0.010	0.012
D	2.00 BSC			0.079 BSC		
D2	1.50	-	1.75	0.059	-	0.069
E	3.00 BSC			0.118 BSC		
E2	1.60	-	1.90	0.063	-	0.075
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
SIPEX Pkg Signoff Date/Rev:				JL Aug18-05 / RevA		

SP7606

ORDERING INFORMATION

Part Number	Junction Temperature Range	Package
SP7606ER-L	-40°C to +125°C	Lead Free 8-PIN 2 x 3 mm DFN
SP7606ER-L/TR	-40°C to +125°C	Tape and Real Lead Free 8-PIN 2 x 3 mm DFN

Pack Quantity for tape and real is 3000

REVISION HISTORY

DATE	REVISION	DESCRIPTION
December 2007	A	Original Release

For further assistance:

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EXAR Technical Documentation: http://www.exar.com/TechDoc/default.aspx?

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