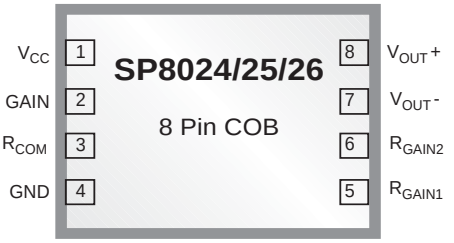
200V/μs Integrated APC Amplifier

with Gain Adjust & Differential Output

FEATURES

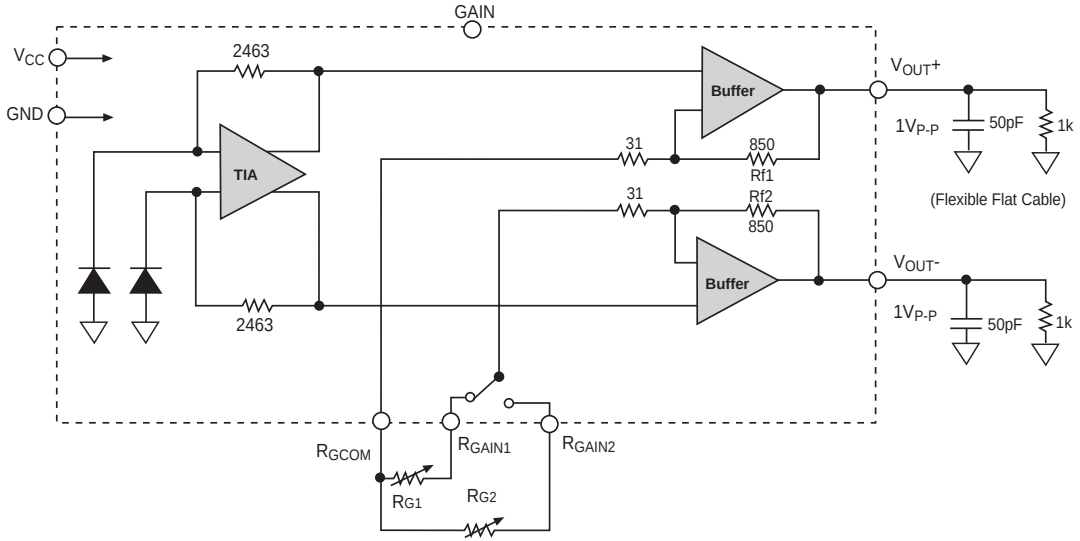
- Slew Rate of 200V/μs
- Fast Settling Time - 10ns
- Gain Switch
- 2V Output Swing
- Low Offset Voltage: < 10mV
- Low Offset Drift: < 20μV/°C
- 12dB External Gain Adjust Range



DESCRIPTION

The SP8024, SP8025, and SP8026 are high-speed, differential output APC amplifiers that integrate the photodiode and adjustable gain block on one chip. This allows the user to control the laser power of the system in high-speed DVDRW, DVDRAM and CDRW systems. The wide 2V output swing also allows better system performance.

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

$T_{J(MAX)}$ ..... 120°C
$V_{S(MAX)}$ 6V
$V_{IN(MAX)}$ 6V

ELECTRICAL SPECIFICATIONS

Unless otherwise noted: V_{CC} = +5.0V, C_{LOAD} = 50pF to GND, R_{GAIN}=262Ω and R_{LOAD} = 1kΩ. -20°C≤T_A≤ +85°C, nominal gain

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage		4.5	5	5.5	V
Nominal Output Sensitivity SP8024 SP8025 SP8026	Any Select Mode ODB Gain		 1000 2000 3000		V/W
Input Optical Power Required to Produce 2 V Output Swing SP8024 SP8025 SP8026	Any Select Mode ODB Gain		 2 1 0.666		mW
Full Scale Output Voltage Swing(Vp-p)		1.9	2		V
Output Common Mode Voltage			V_{CC}/2		V
Differential Output Offset Voltage		-10		10	mV
Differential Output Offset Voltage Drift		-20		20	µV/°C
Differential Output Noise	BW: 1kHz to 1MHz		1	2	mV
Differential Output Noise	BW: 1kHz to 100MHz		3	5	mV
Differential Output Slew Rate		200	250		V/µs
Differential Output Settling Time to 1% of Final Value, 2V Step			10	15	ns
Output Overshoot, 2V step				5	%
Bandwidth (-3db)		65	100		MHz
PSRR	4.5V < V_{CC} < 5.5V	60	65		dB
Power Supply Current	T_A = 25°C Full Temp No Load		20	 25	mA
Gain Adjust Range	< 5% Overshoot, 150 < R_{GAIN} < 1350Ω	-9		3	dB
Input Voltage Vlow(TTL Level) Vhigh(TTL Level)		 2.2		 0.8	 V V
T_{JA}, 3mm x 3.5mm Package			75		°C/W

PIN DESCRIPTION

PIN NUMBER	NAME	FUNCTION
1	V_{CC}	Supply Voltage
2	GAIN	Gain Select
3	R_{COM}	Common connection point for $R_{GAIN}1$ and $R_{GAIN}2$
4	GND	Power Ground
5	R_{GAIN1}	Gain Adjust 1
6	R_{GAIN2}	Gain Adjust 2
7	V_{OUT}-	Output Voltage -
8	V_{OUT}+	Output Voltage +

THEORY OF OPERATION

Internal Operation

The SP8024/25/26 APC circuits have an integrated photo detector and are designed with three nominal sensitivities of 1mV/μW, 2mV/μW and 3mV/μW respectively. Each part's sensitivity can also be adjusted continuously and independently for two different gain modes via two external resistors over a range of 12dB. The two gain modes are controlled by a TTL compatible logic input. This logic input also normalizes the internal photo detector's responsivity for 650nm and 780nm laser wavelengths. The logic pin selects between the two external gain setting resistors to allow independent control and settings for the two gain functions.

The 8024 APC family uses two stages of gain to optimize for speed and offset. The two stages consist of a differential trans-impedance amplifier (TIA), and a differential gain adjust amplifier.

TIA

The first stage is a differential trans-impedance amplifier (TIA) for converting the photo detector output current to a balanced differential voltage. This topology allows for fast settling of the photo detector and also cancels offset effects. The TIA has no external components.

Variable Gain Amplifier

This stage is used to vary the gain of the system. It provides selection for two different gain setting resistors, R_{GAIN1} and R_{GAIN2}, at pins 5 and 6 via internal MOSFET switches S1 and S2. The logic input at pin 2 controls the selection of the two external gain set resistors.

Table 1: Gain Select Logic Truth Table

Gain Select Pin 2	Rexternal, Pin 3 to:	Gain Factor (x)	Sensitivity (mV/μW) $R_{G1} = R_{G2} = 262\Omega$		
			SP8024	SP8025	SP8026
0 or Open	R_{G1} - Pin 5	6.25	1	2	3
1	R_{G2} - Pin 6	6.25	1	2	3

The gain of this balanced amplifier topology is given by:

$$GAIN = 1 + \frac{Rf1 + Rf2}{R_{EXT}}$$

where R_{GAIN} is external and Rf1 = Rf2 = 850Ω in feedback.

The nominal gain is defined as 6.25.

Variable Gain Amplifier: continued

There are internal buffering resistors and a MOSFET switch resistance in series with the external Rgain. These internal resistances add up to a nominal value of 62Ω. Therefore the true gain equation is:

$$GAIN = 1 + \frac{Rf1 + Rf2}{R_{EXT} + 62}$$

This gives a nominal external Rgain value of 324 - 62 = 262Ω for a gain of 6.25.

The constraints on this stage are the parasitic capacitances associated with the input pins. The resistors used for setting the system gain are actually subminiature potentiometers. They are used for calibrating out systematic variations in the optical path.

Pins 5 and 6 connect to the summing node of the gain stage through MOSFET switches. When a capacitor is added to the summing node of an inverting amplifier it creates a pole in the response. If this pole increases enough to interfere with the internal compensation of the amplifier, instability occurs. This instability appears as overshoot in the transient response. The stray capacitance at pins 5 and 6 should be kept below 1pF.

This stage also allows the part to drive high capacitive loads. The maximum load capacitance is 50pF bulk. The actual load is typically a flexible ribbon cable (FLEX) that acts like a transmission line. This presents a distributed capacitive load plus inductance and resistance. In this case care should be taken to match the characteristic impedance of the line at the far end to avoid standing waves and ringing. The buffer is designed to drive 1kΩ to ground. However, this resistor can be adjusted in value to accommodate the characteristic impedance of the signal trace.

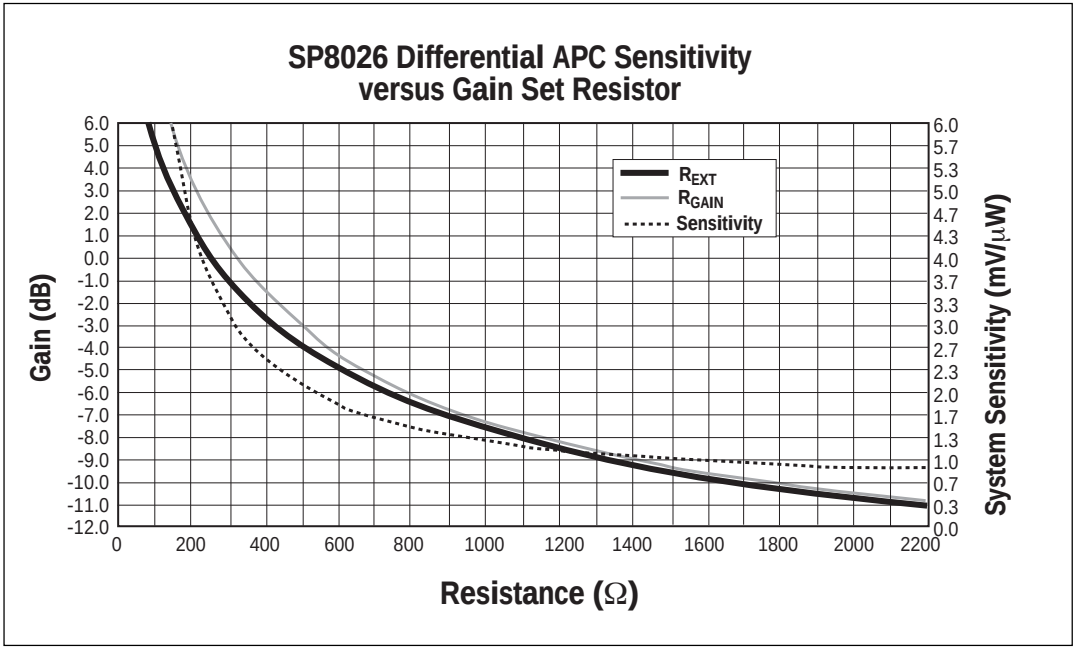


Figure 1. System Gain versus Gain Set Resisitor

Layout and Routing Considerations

Special care must be taken when designing the Flex or PCB for this part. The output peak current requirement is in the order of 12.5mA when driving 50pF of capacitive load with a slew rate of 200V/s Therefore care must be taken to provide low inductance, low resistance paths for power and ground and output traces.

Supply coupling is also very important. Good supply decoupling is important to ensure the high frequency performance of the system by eliminating supply lead inductance effects. The decoupling capacitor C1 should be as close to the part as possible. This capacitor should be 0.1μF ceramic. C2 is optional to improve decoupling and is recommended to be 1μF tantalum. The layout of the PCB is pictured here. Note the wide and short traces on the supply lines.

The traces for the gain resistors R1 and R2 are kept as short as possible to avoid excessive parasitics. Any parasitics on these nodes will limit the performance of the system. R1 and R2 are subminiature potentiometers in the application. This is a single layer board done on FR4 material.

In order to minimize coupling capacitance into the gain setting resistor nodes, it is also critical that V_{OUT}+ and V_{OUT}- are routed away from the traces associated with the gain-setting resistors.

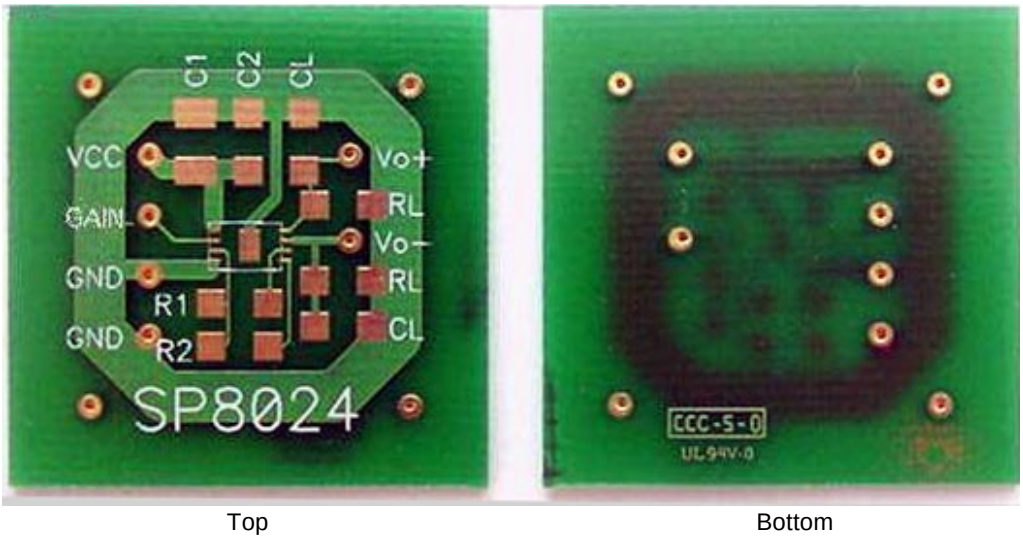


Figure 2. Test and Evaluation PCB Layout for COB 8 Lead Package

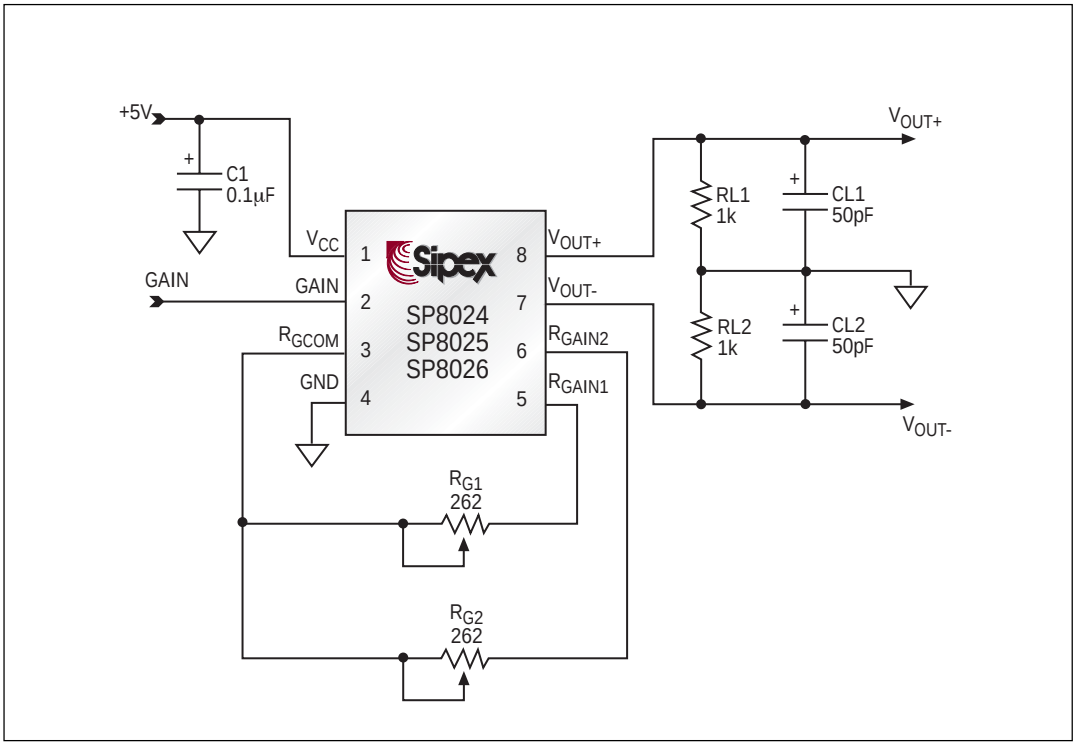
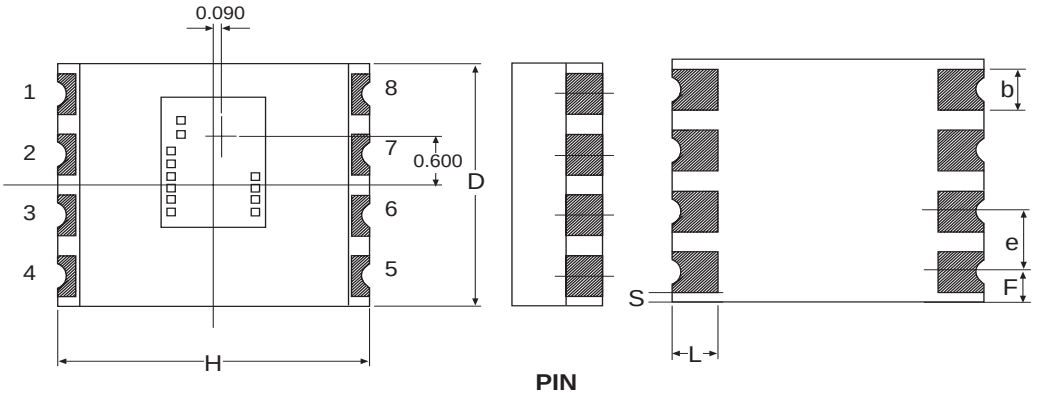
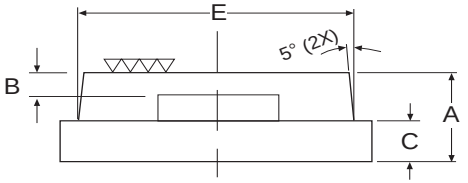


Figure 3. Test and Evaluation Schematic

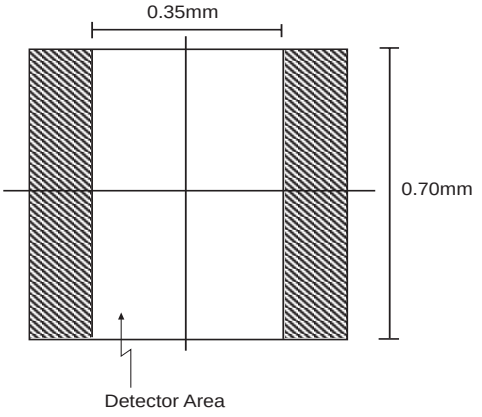


TOP VIEW **PIN SIDE VIEW** **BOTTOM VIEW**



SIDE VIEW

DETECTOR SIZE



DIMENSIONS in mm Minimum/Maximum	8–PIN COB
A	0.90/1.10
B	.127/.33
b	0.30/0.50
c	0.50 nom
D	2.90/3.10
E	3.00/3.20
e	0.75 nom
H	3.40/3.60
L	0.40/0.60
F	0.28/0.48
S	0.075/0.275

8 PIN COB
(3.5mm x 3.0mm)

ORDERING INFORMATION

Part Number	Temperature Range	Package Type
SP8024	-20°C to +85°C	8 lead COB (3.0mm x 3.5mm)
SP8025	-20°C to +85°C	8 lead COB (3.0mm x 3.5mm)
SP8026	-20°C to +85°C	8 lead COB (3.0mm x 3.5mm)

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