

# SP8647

## 250MHz ÷ 10/11

The SP8647 is an ECL variable modulus divider, with ECL10K and TTL/CMOS compatible outputs. It divides by 10 when either of the ECL control inputs, PE1 or PE2, is in the high state and by 11 when both are low (or open circuit).

The two clock inputs are interchangeable and either will act as a clock inhibit when connected to an ECL high level. Normally, one input is left open circuit and the other is AC-coupled, with externally applied bias.

### FEATURES

- ECL Compatible Inputs/Outputs
- Open Collector TTL/CMOS Output
- AC-Coupled Input (External Bias)

### QUICK REFERENCE DATA

- Supply Voltage:  $-5.2V \pm 0.25V$  (ECL),  $5.0V \pm 0.25V$  (TTL)
- Power Consumption: 260mW
- Temperature Range:  $-30^{\circ}C$  to  $+70^{\circ}C$

### ABSOLUTE MAXIMUM RATINGS

Supply voltage, $ V_{CC} - V_{EE} $	8V
Output current	20mA
Storage temperature range	$-65^{\circ}C$ to $+150^{\circ}C$
Max. junction temperature	$+175^{\circ}C$
Open collector voltage (pin 11)	+12V
Max. clock input voltage	2.5V p-p
Max. open collector current	15mA

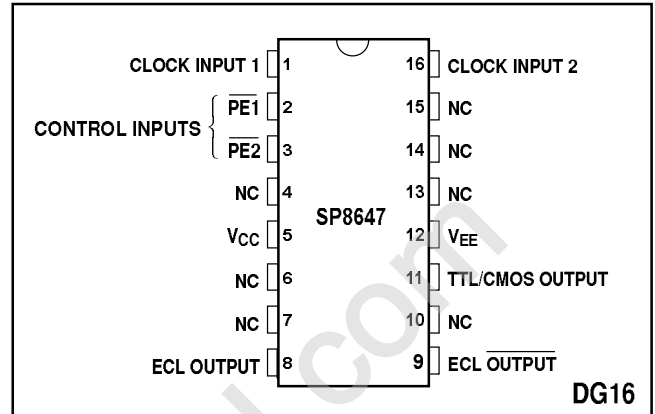


Fig. 1 Pin connections - top view

### ORDERING INFORMATION

**SP8647 B DG**  
**5962-90618 (SMD)**

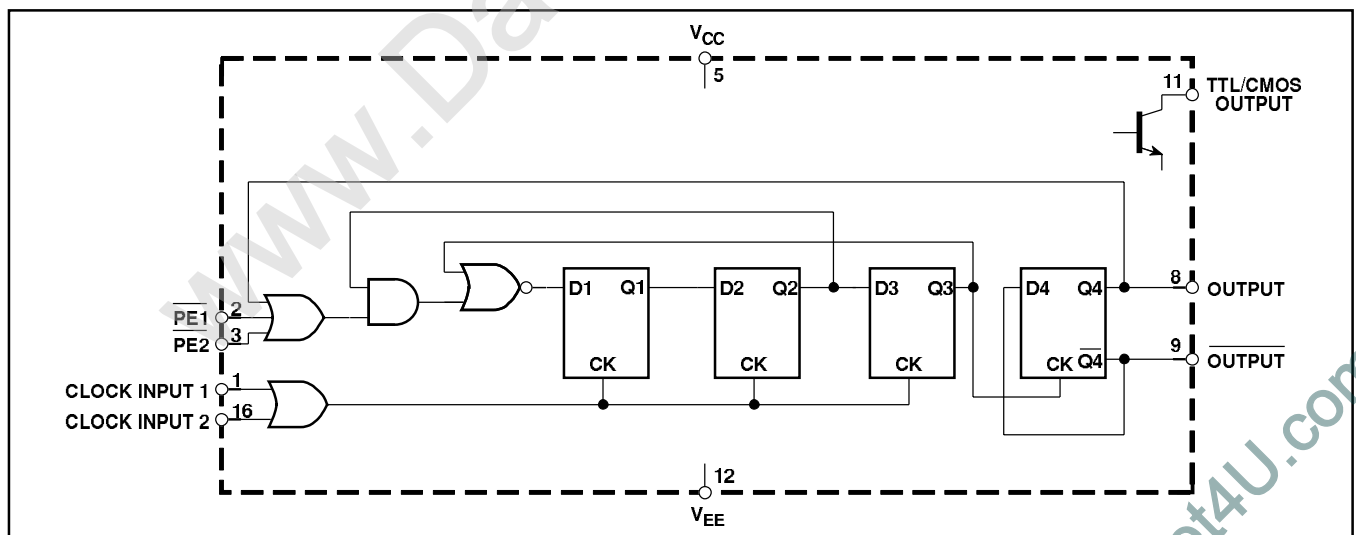


Fig. 2 Functional diagram

**ELECTRICAL CHARACTERISTICS**

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range

**ECL OPERATION**

Supply voltage,  $V_{CC} = 0V$ ,  $V_{EE} = -5.2V \pm 0.25V$   
 Temperature,  $T_{AMB} = -30^{\circ}C$  to  $+70^{\circ}C$

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	$f_{MAX}$	250		MHz	Input = 400-800mV p-p	5
Minimum frequency (sinewave input)	$f_{MIN}$		50	MHz	Input = 400-800mV p-p	5
Power supply current	$I_{EE}$		65	mA	$V_{EE} = -5.2V$	5
ECL output high voltage	$V_{OH}$	-0.85	-0.7	V	$V_{EE} = -5.2V$ (25°C)	
ECL output low voltage	$V_{OL}$	-1.8	-1.5	V	$V_{EE} = -5.2V$ (25°C)	
Clock and PE input high voltage	$V_{INH}$	-0.93		V	$V_{EE} = -5.2V$ (25°C)	
Clock and PE input low voltage	$V_{INL}$		-1.62	V	$V_{EE} = -5.2V$ (25°C)	
Clock to ECL output delay	$t_p$		6	ns		6
Set-up time	$t_s$	2.5		ns		3, 6
Release time	$t_r$	3		ns		4, 6

**TTL OPERATION**

Supply voltage,  $V_{CC} = 5V \pm 0.25V$ ,  $V_{EE} = 0V$   
 Temperature,  $T_{AMB} = -30^{\circ}C$  to  $+70^{\circ}C$

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	$f_{MAX}$	250		MHz	Input = 400-800mV p-p	5
Minimum frequency (sinewave input)	$f_{MIN}$		50	MHz	Input = 400-800mV p-p	5
Power supply current	$I_{EE}$		65	mA		5
TTL output low voltage	$V_{OL}$		0.5	V	$V_{CC} = 5.25V$ , sink current = 8mA	5, 7
TTL output high voltage	$V_{OH}$	3.5		V	$V_{CC} = 5.0V$	5, 7
Clock to TTL output high delay, +ve going	$t_{PLH}$		15	ns		6
Clock to TTL output low delay, -ve going	$t_{PHL}$		15	ns		6
Set-up time	$t_s$	2.5		ns		3, 6
Release time	$t_r$	3		ns		4, 6

**NOTES**

1. The temperature coefficients of  $V_{OH} = +1.63mV/^{\circ}C$ ,  $V_{OL} = +0.94mV/^{\circ}C$  and of  $V_{IN} = +1.22mV/^{\circ}C$ .
2. The test configuration for dynamic testing is shown in Fig.6.
3. The set-up time  $t_s$  is defined as the minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure that the ÷ 10 mode is obtained.
4. The release time  $t_r$  is defined as the minimum time that can elapse between H→L transition of control input and the next L→H clock pulse transition to ensure that the ÷ 11 mode is obtained.
5. Tested at 25°C only.
6. Guaranteed but not tested.
7. The open collector output is not recommended for use at output frequencies above 15MHz.  $C_{LOAD} \leq 5pF$ .

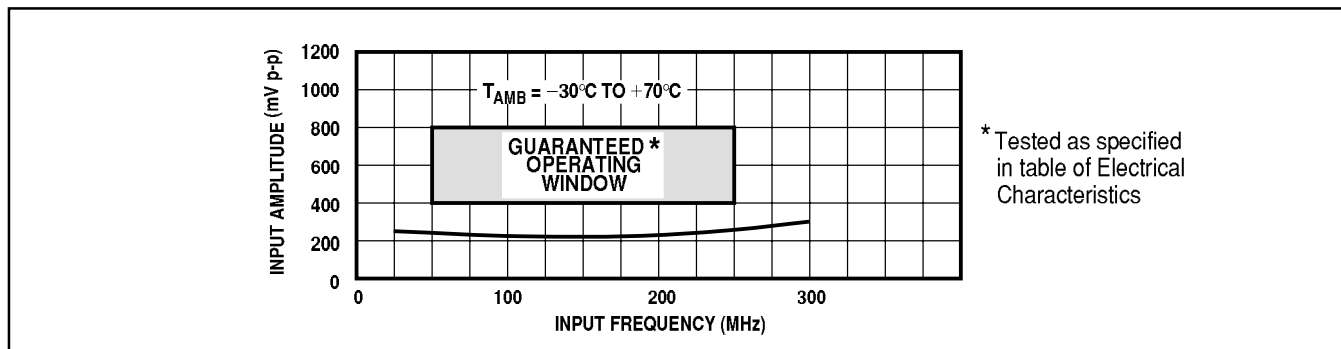


Fig. 3 Typical input characteristic

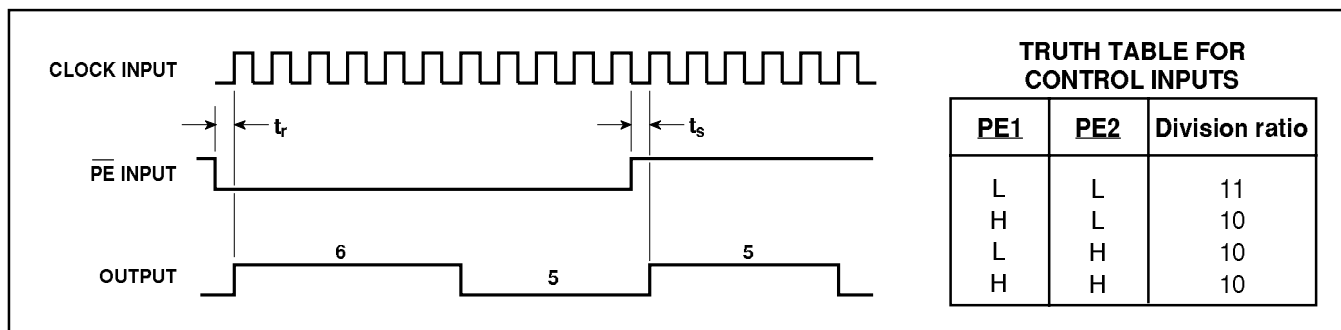


Fig. 4 Timing diagram

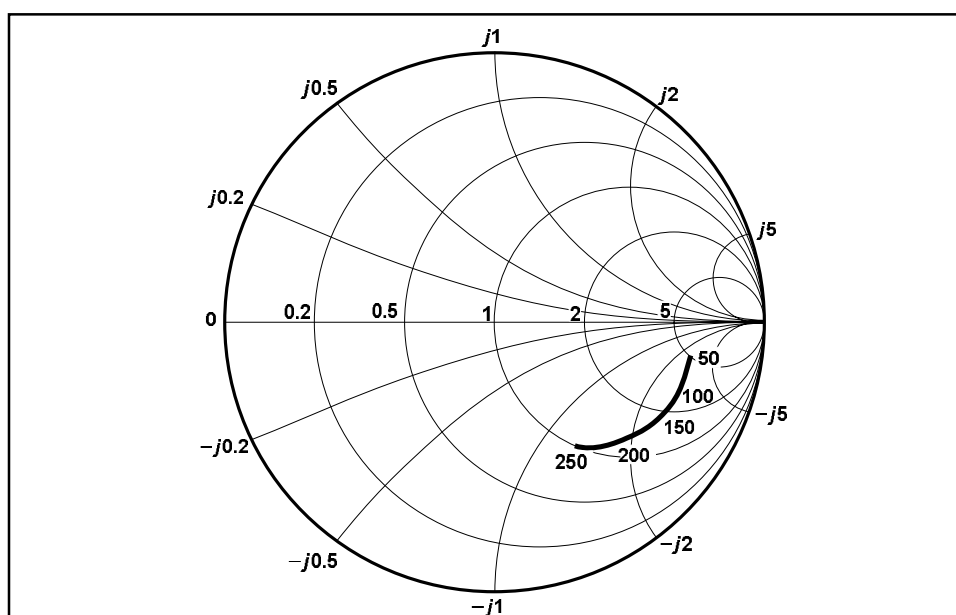


Fig. 5 Typical input impedance. Test conditions: Supply Voltage = 5V, Ambient Temperature = 25°C. Frequencies in MHz, impedances normalised to 50Ω.

### OPERATING NOTES

1. The clock and control inputs are ECLIII compatible. There is an internal pulldown resistor to  $V_{EE}$  of 4.3kΩ on each input and therefore any unused input can be left open circuit. If it is desirable to capacitively couple the signal source to the clock then an external bias is required as shown in Fig. 6. The external bias voltage should be -1.3V at 25°C.
2. The outputs are compatible with ECLII but can be interfaced to ECL10K as shown in Fig.8.
3. The circuit will operate down to DC but slew rate must be better than 100V/μs.

4. Input impedance is a function of frequency. See Fig. 5.
5. The TTL/CMOS output is a free collector, with an output rise/fall time which is a function of load resistance and load capacitance. The load capacitance should therefore be kept to a minimum and the load resistance should not be too small otherwise  $V_{OL}$  will be too great. For example, TTL output current = 8mA,  $V_{OL} = 0.5V$ . For CMOS outputs, the value of load resistor should be the maximum consistent with satisfactory rise times.
6. All components should be suitable for the frequency in use.

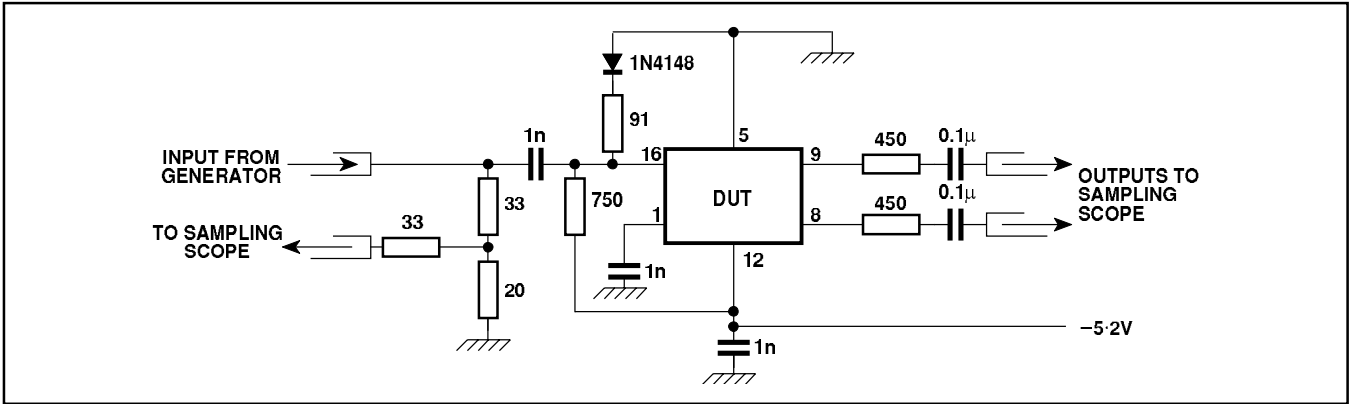


Fig. 6 Test circuit

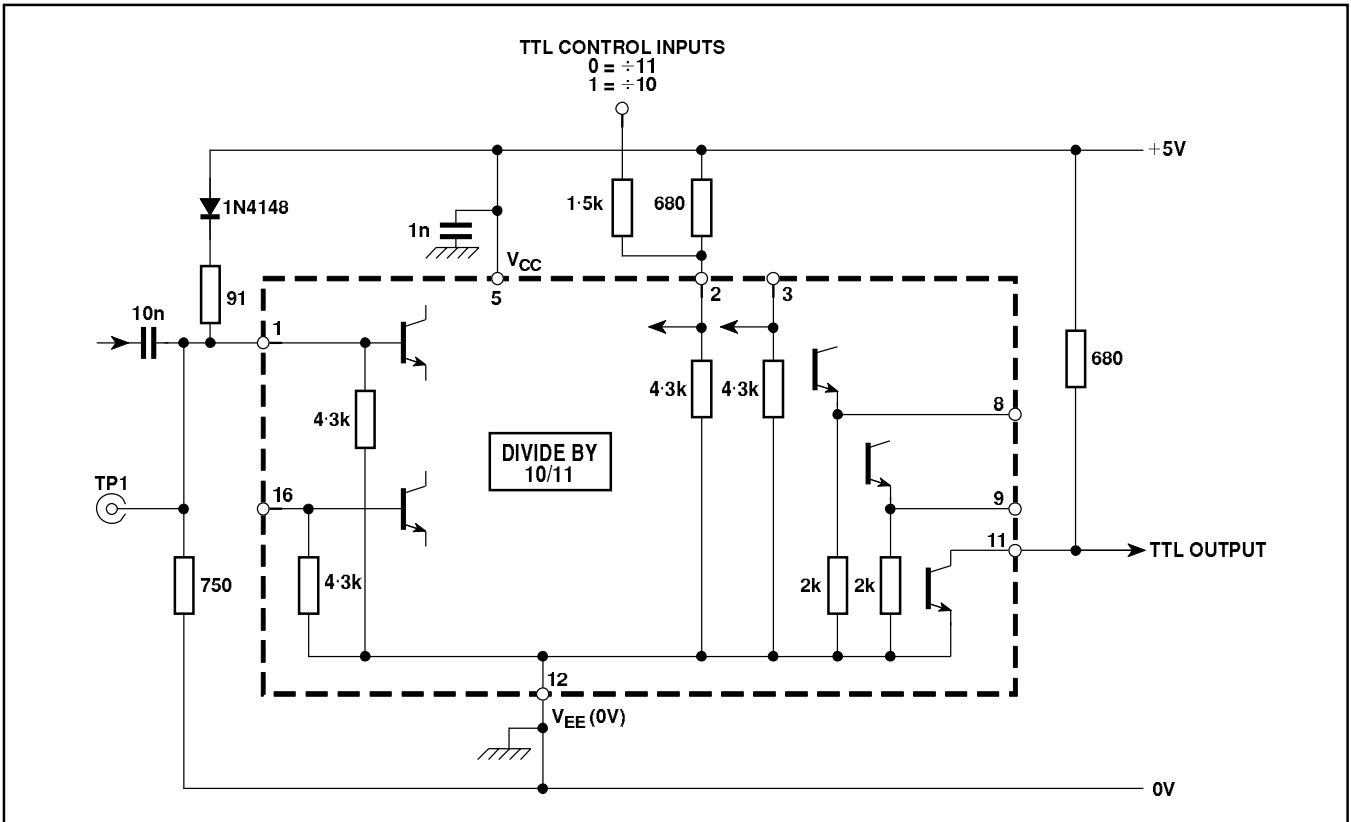


Fig. 7 Typical application showing TTL interfacing. NB: Voltage at TP1 should be +3.75V at 25°C.

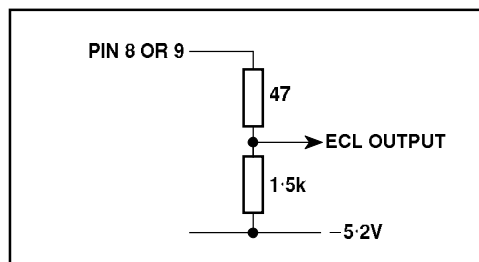
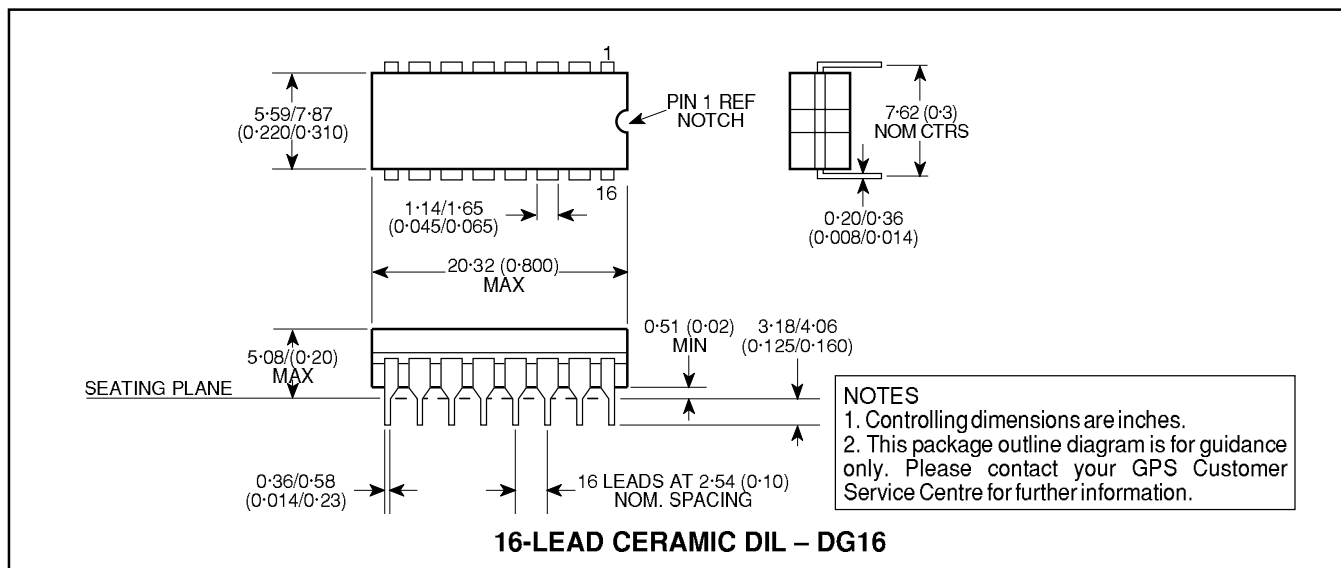


Fig. 8 Interfacing to ECL10K

NOTES

**PACKAGE DETAILS**

Dimensions are shown thus: mm (in).



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