SP8656 ÷ (24)
SP8658 ÷ (20)

The SP8656 and SP8658 are fixed ratio (divide by 24 and 20) low power counters for operation at frequencies in excess of 200MHz over the temperature ranges -30°C to -70°C.

In all cases the input can be either single or double driven and must be capacitively coupled to the signal source. If single drive is used the unused input must be decoupled to the ground plane.

The free collector saturating output stage is capable of interfacing with TTL and CMOS.

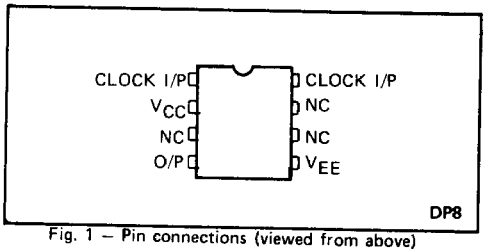

Fig. 1 – Pin connections (viewed from above)

FEATURES

- VHF Operation
- Low Power Dissipation
- Output TTL and CMOS Compatible

APPLICATIONS

- Low Power VHF Communications
- Portable Counters

ABSOLUTE MAXIMUM RATINGS

Power supply voltage: $[V_{CC} - V_{EE}]$	8V
Input voltage V_{IN}	Not greater than supply voltage in use.
Output sink current I_O	10mA
Operating junction temperature	+150°C
Storage temperature	-55°C to +125°C

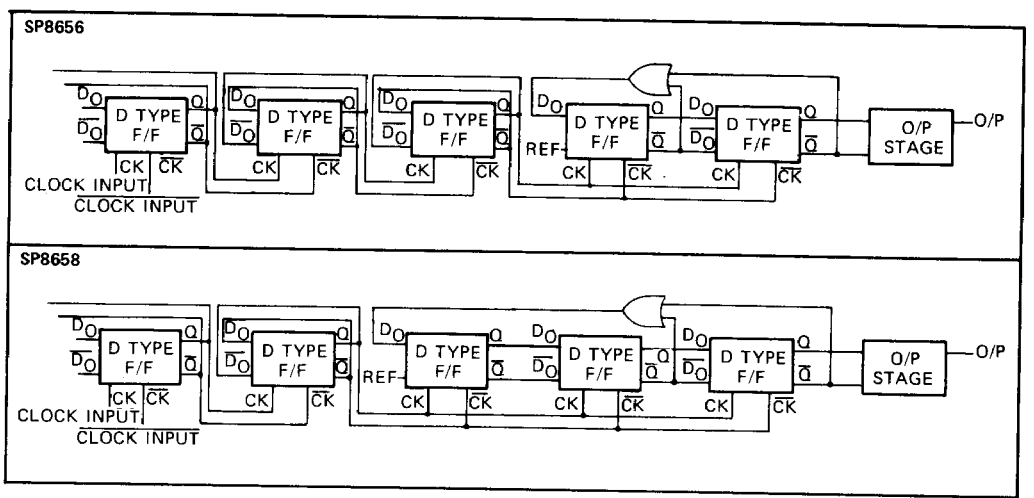

Fig. 2 Logic diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Operating ambient temperature T_{amb} -30°C to + 70°C

Operating supply voltage V_{cc} : 4.75v to 5.25v

Input voltage single drive: 400mV to 800mV pk-pk

double drive: 250mV to 800mV pk-pk

Output load 3.3kΩ to -10V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Maximum input frequency	200			MHz	
Minimum sinusoidal input frequency		20	40	MHz	
Minimum slew rate of square wave input		30	100	V/μsec	
Power supply drain current		20	30	mA	Vcc= +5.5V
Output level (high)	9.0			V	
Output level (low)			400	mV	

OPERATING NOTES

Fig. 3 gives capacitive values for AC and DC coupling of the input capacitor and bias points on the test circuit – these values are not critical and will depend on the operating frequency.

The devices will normally self-oscillate in the absence of an input signal. This can be easily prevented by connecting a 39kΩ resistor from either input (double drive) to V_{EE}; if the device is single driven then it is recommended that the pulldown resistor be connected to the decoupled unused input. The slight loss of input sensitivity resulting from this technique does not seriously affect the operation of the device.

The input waveform will normally be sinusoidal but below 40MHz, correct operation depends on the slew rate of the input signal. A slew rate of 100V/μs will enable the device to operate down to DC.

The output stage will drive three TTL gates without the addition of a pull-up resistor. Using a pull-up resistor of 3.3kΩ to a +10V will allow the output to drive a CMOS counter at a frequency of up to 5MHz.

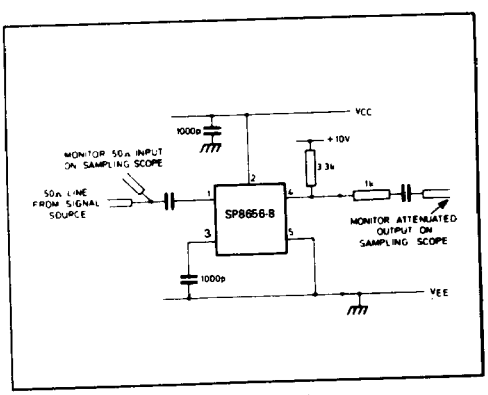

Fig. 3 Test circuit