PLESSEY
Semiconductors

T-45-19-09

SP8660A & B

150MHz ÷ 10

The SP8660A/B is a low power emitter coupled logic counter with an open collector output capable of driving TTL or CMOS. The device is available in two temperature ranges: -55°C to +125°C (A grade) or -30°C to +70°C (B grade). It has internally biased inputs.

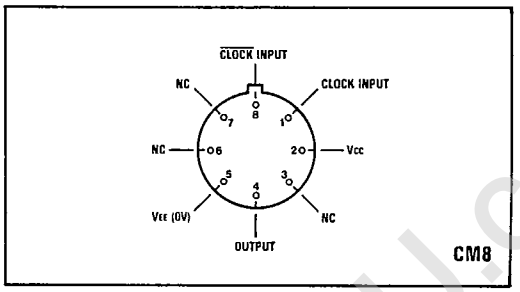

Fig.1 Pin connections - bottom view

FEATURES

- AC Coupled Inputs
- Low Power Consumption
- Open Collector Output CMOS and TTL Compatible

QUICK REFERENCE DATA

- Supply Voltage: 5.0V
- Power Consumption: 50mW
- Temperature Range:
  - -55°C to +125°C (SP8660A)
  - -30°C to +70°C (SP8660B)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Open collector output voltage	12V
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Output sink current	10mA
Max. clock I/P voltage	2.5V p-p

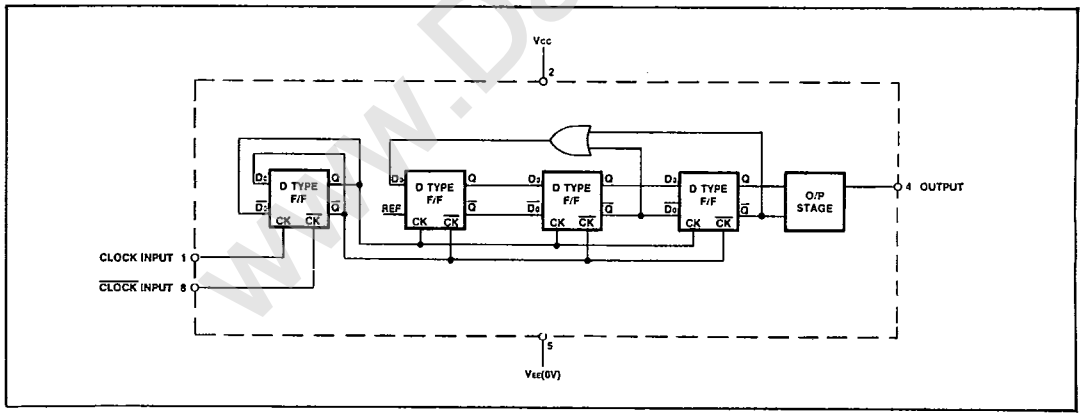

Fig.2 Functional diagram

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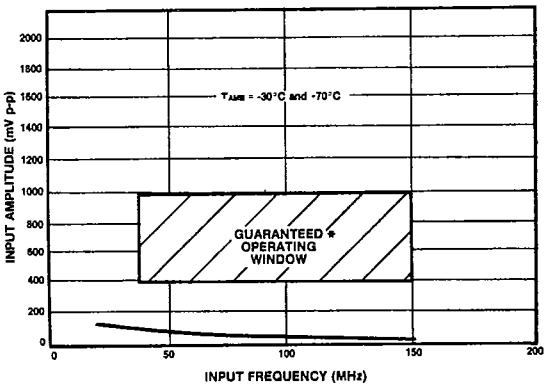
ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 5.0V ± 0.25V V_{EE} = 0V
Temperature: A grade T_{amb} = -55°C to +125°C
B grade T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	150		MHz	Input =400 - 800mV	
Minimum frequency (sinewave input)	f_{min}		40	MHz	Input =400 - 800mV	
Power supply current	I_{EE}		13	mA	V_{CC}= 5.25V	
Output high voltage	V_{OH}	7.5		V	V_{CC}= 5V	
					Pin 4 = 1.5kΩ to 10V	Note 4
Output low voltage	V_{OL}		400	mV	V_{CC} = 5V	
					Pin 4 = 1.5kΩ to 10V	

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The dynamic test circuit is shown in Fig.5.
3. Above characteristics are not tested at 25°C (tested at low and high temperature only).
4. $C_{load} \leq 5pF$.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristic of SP8660A

OPERATING NOTES

1. The clock inputs (pin 1 and 8) should be capacitively coupled to the signal source. When driven single-ended, the input signal path is completed by connecting a capacitor from the unused input to ground.
2. In the absence of a signal the devices will self-oscillate. This can be prevented by connecting a 39k resistor from either input to ground. If the device is driven single ended, it is recommended that the pulldown resistor be connected to the decoupled unused input. There will be a loss in sensitivity of approximately 200mV.
3. The device will operate down to DC but the input slew rate must be better than 100V/µs.
4. The open collector output will drive 3 TTL loads, and thus requires a suitable resistor to Vcc to maintain noise immunity. In order to ensure noise immunity on transitions, this resistor should not exceed 4.7k. For interfacing to CMOS, the open collector may be restored to a +10V line via a 3.3k resistor. The output sink current must not exceed 10mA, and the use of too low a value of resistor may lead to a loss of noise immunity, especially at low temperatures.
5. Input impedance is a function of frequency. See Fig. 4.
6. The rise time of the open collector output waveform is directly proportional to the load capacitance and load resistor value. Therefore the load capacitance should be minimised and the load resistor kept to a minimum compatible with system power requirements. In the test configuration of Fig. 5, the output rise time is approximately 20ns and fall time is 10ns typically.

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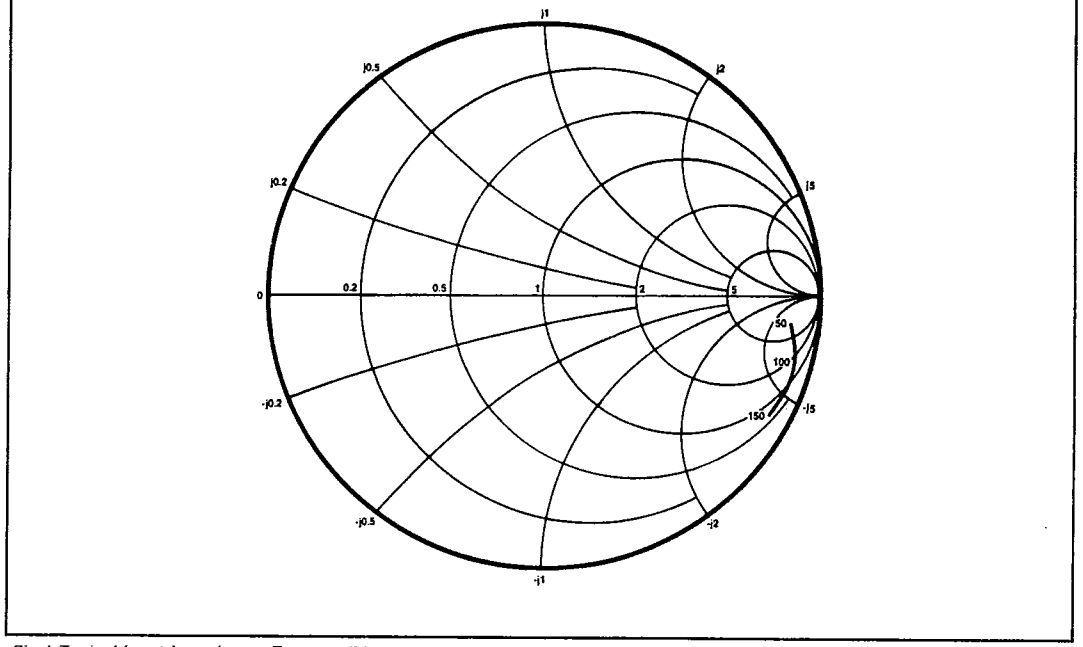

Fig.4 Typical input impedance. Test conditions: supply voltage 5.0V, ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 ohms.

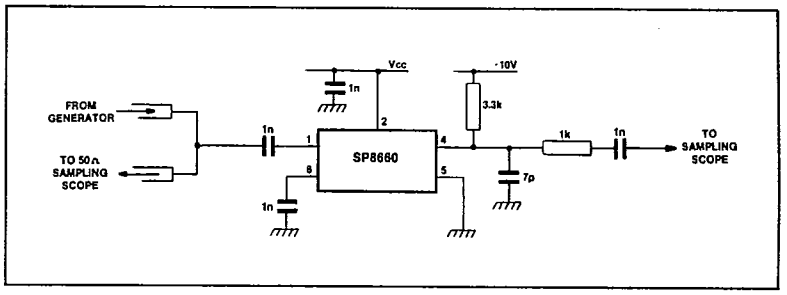

Fig.5 Test circuit

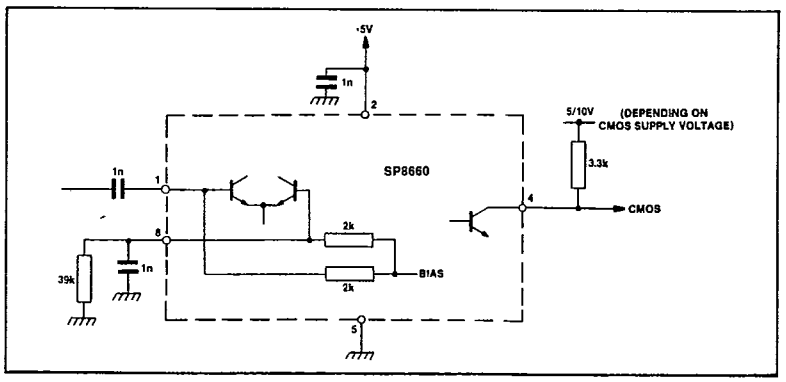

Fig.6 Typical application showing interfacing

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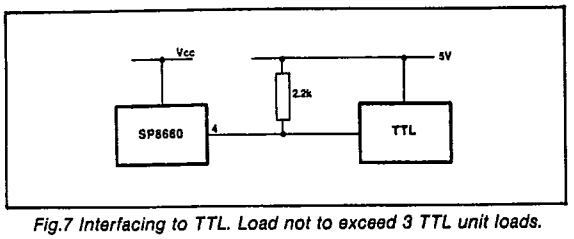

Fig.7 Interfacing to TTL. Load not to exceed 3 TTL unit loads.