SP8685

500MHz÷10/11

The SP8685 is an ECL variable modulus divider, with ECL10K compatible outputs. It divides by 10 when either of the ECL control inputs, PE1 or PE2, is in the high state and by 11 when both are low (or open circuit).

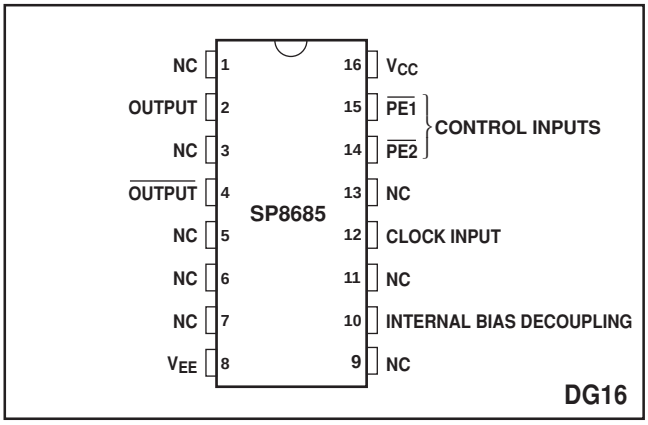


Fig. 1 Pin connections - top view

FEATURES

- Divides by 10 or 11
- AC-Coupled Input (Internal Bias)
- ECL Compatible Output

QUICK REFERENCE DATA

- Supply Voltage: −5·2V
- Power Consumption: 300mW
- Temperature Range:

  −55°C to +125°C (A Grade)
  −30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	−8V
Output current	20mA
Storage temperature range	−65°C to +150°C
Max. junction temperature	+175°C
Max. clock input voltage	2·5V p-p

ORDERING INFORMATION

SP8685 A DG
SP8685 B DG
SP8685 AC DG
SP8685 NA 1C

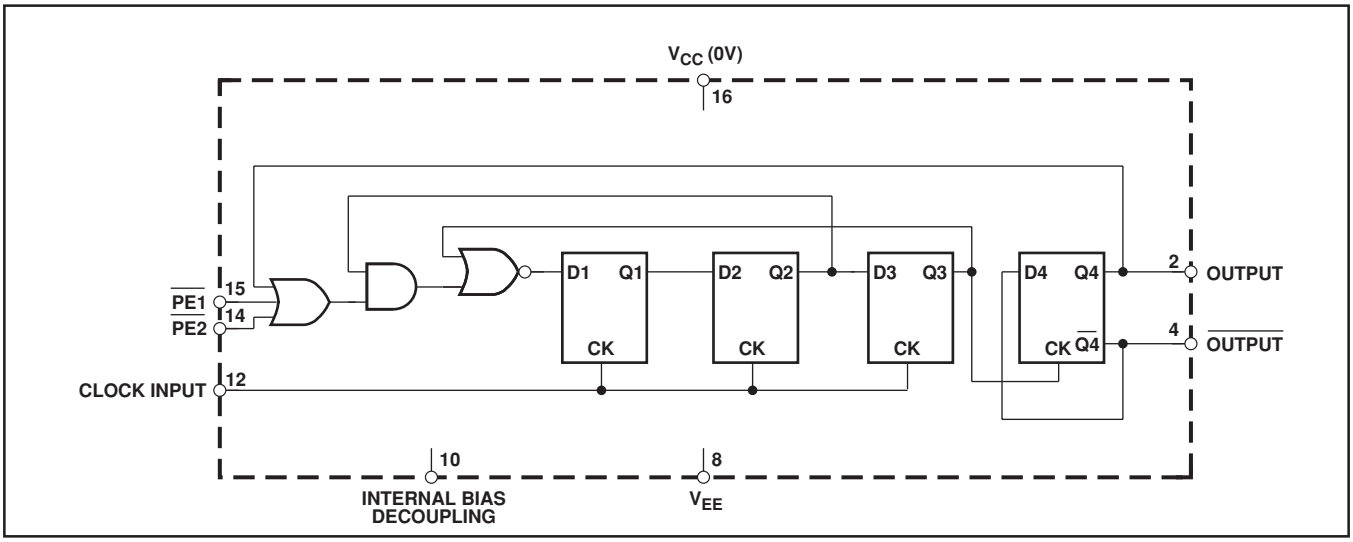


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range

Supply voltage, V_{CC} = 0V, V_{EE} = −5·2V ± 0·25V

Temperature, T_{AMB} = −55°C to +125°C (A Grade), −30°C to +70°C (B Grade)

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{MAX}	500		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{MIN}		50	MHz	Input = 400-800mV p-p	
Power supply current	I_{EE}		70	mA	V_{EE} = −5·2V	
Output high voltage	V_{OH}	−0·87	−0·7	V	V_{EE} = −5·2V (25°C)	
Output low voltage	V_{OL}	−1·8	−1·5	V	V_{EE} = −5·2V (25°C)	
PE input high voltage	V_{INH}	−0·93		V	V_{EE} = −5·2V (25°C)	
PE input low voltage	V_{INL}		−1·62	V	V_{EE} = −5·2V (25°C)	
Clock to output delay	t_p		6	ns		5
Set-up time	t_s	2		ns		5
Release time	t_r	2		ns		5

NOTES

1. The temperature coefficients of V_{OH} = +1·63mV/°C, V_{OL} = +0·94mV/°C and of V_{IN} = +1·22mV/°C.
2. The test configuration for dynamic testing is shown in Fig.6.
3. The set-up time t_s is defined as the minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure that the ÷10 mode is obtained.
4. The release time t_r is defined as the minimum time that can elapse between H→L transition of control input and the next L→H clock pulse transition to ensure that the ÷11 mode is obtained.
5. Guaranteed but not tested.

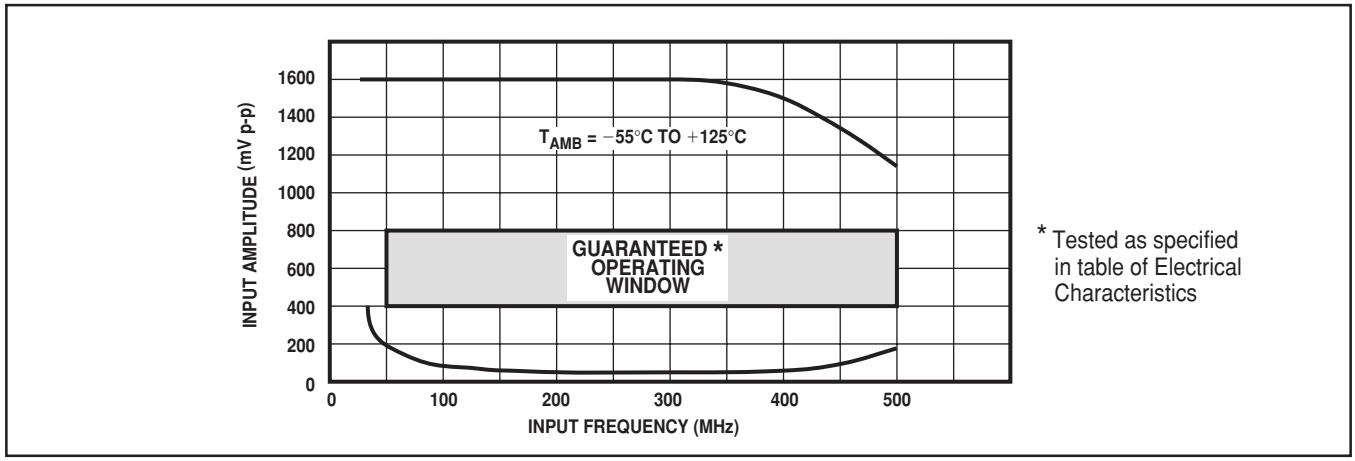
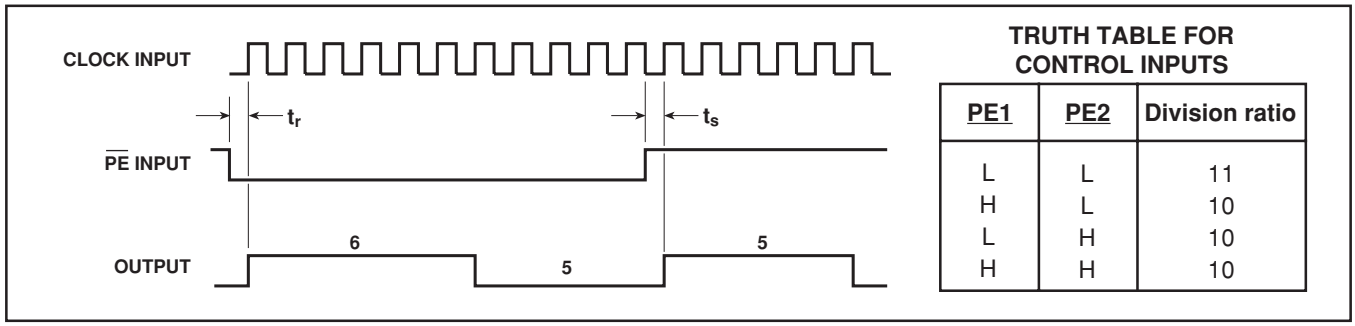


Fig. 3 Typical input characteristic of SP8685A



TRUTH TABLE FOR CONTROL INPUTS

PE1	PE2	Division ratio
L	L	11
H	L	10
L	H	10
H	H	10

Fig. 4 Timing diagram

OPERATING NOTES

1. The clock input is biased internally and is coupled to the signal source with a suitable capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected from pin 10 to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable, it may be prevented by connecting a 15kΩ resistor from the clock input (pin 12) to V_{EE}. This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/μs.
4. The outputs are compatible with ECLII but can be interfaced to ECL10K as shown in Fig. 7.
5. The PE inputs are ECLIII/10K compatible and include 4·3kΩ pulldown resistors. Unused inputs can therefore be left open.
6. Input impedance is a function of frequency, See Fig. 5.
7. All components should be suitable for the frequency in use.

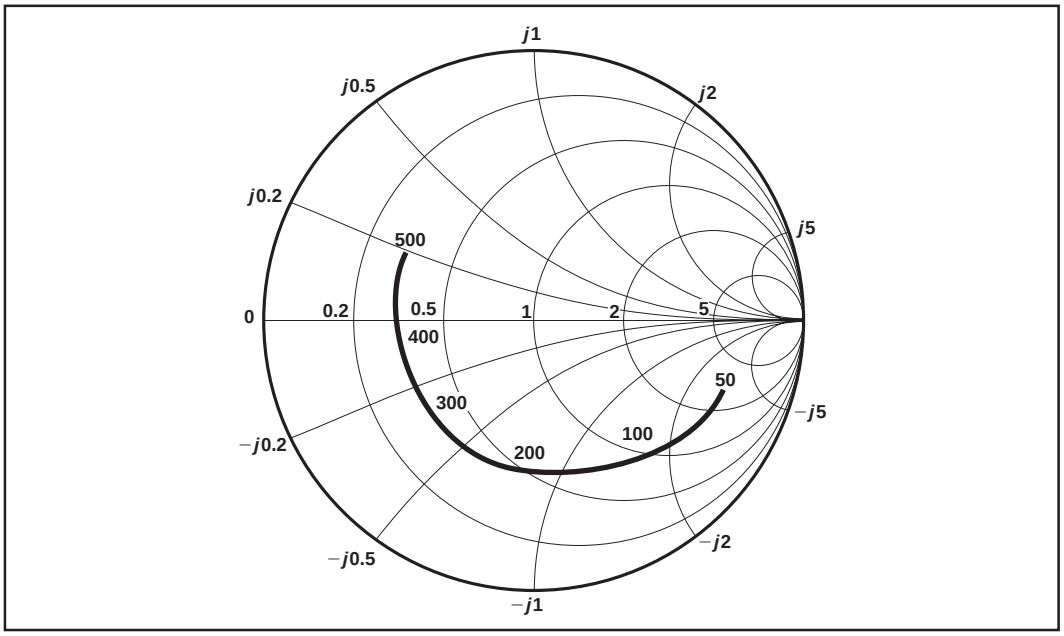


Fig. 5 Typical input impedance. Test conditions: Supply Voltage = −5·2V, Ambient Temperature = 25°C. Frequencies in MHz, impedances normalised to 50Ω.

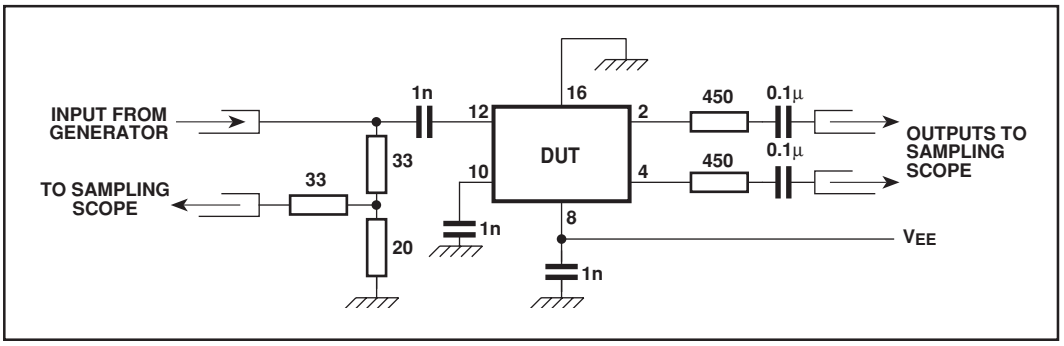


Fig. 6 Test circuit

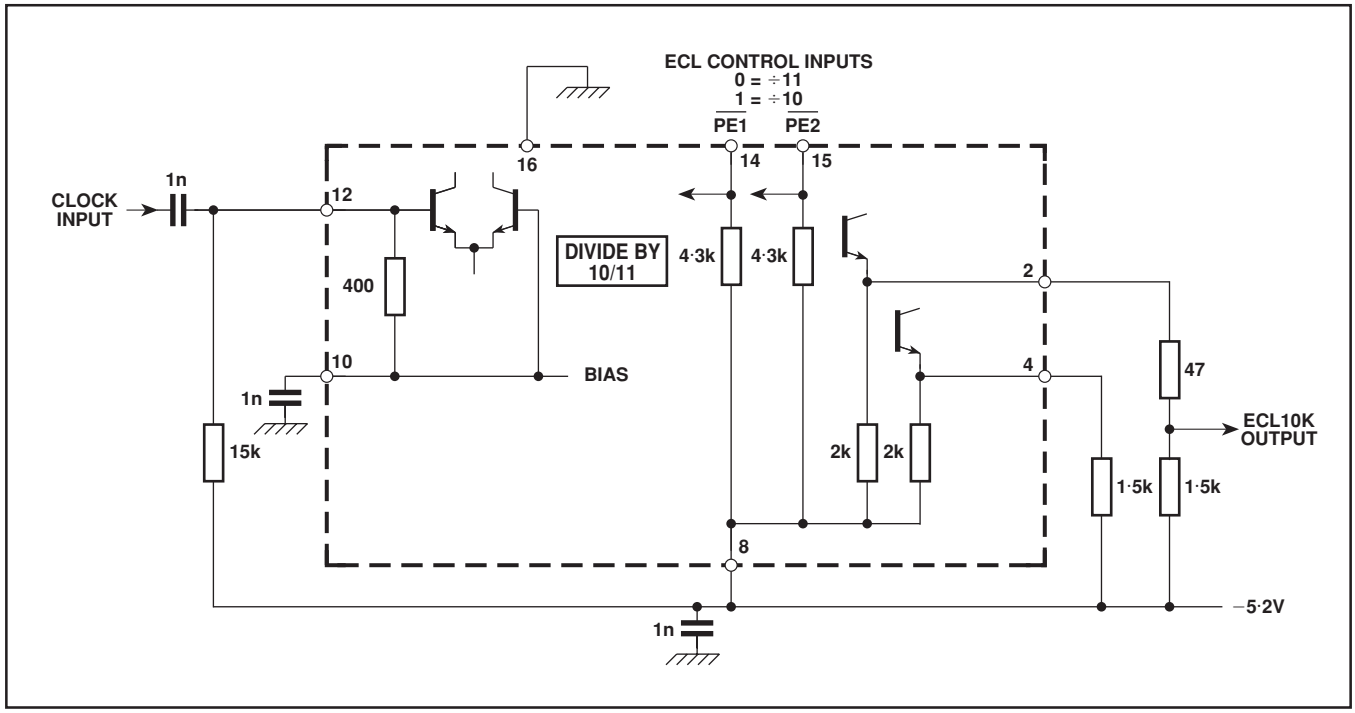
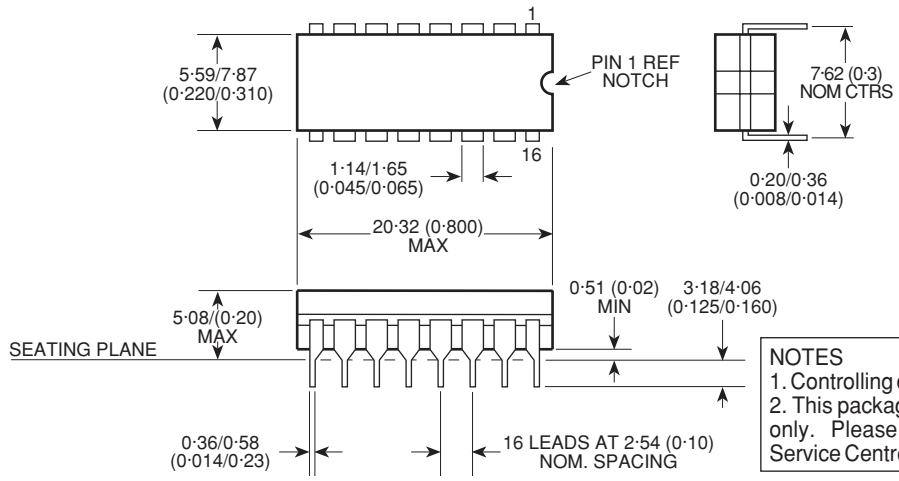


Fig. 7 Typical application showing interfacing

NOTES

PACKAGE DETAILS

Dimensions are shown thus: mm (in).



NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

16-LEAD CERAMIC DIL – DG16

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