GEC PLESSEY
SEMICONDUCTORS

ADVANCE INFORMATION

DS3647-1·2

SP8690 200MHz÷10/11
SP8691 200MHz÷8/9

The SP8690 and SP8691 are low power ECL variable modulus dividers, with both ECL10K and TTL/CMOS compatible outputs. They divide by the lower division ratio when either of the ECL control inputs, $\overline{PE1}$ or $\overline{PE2}$, is in the high state and by the higher ratio when both are low (or open circuit).

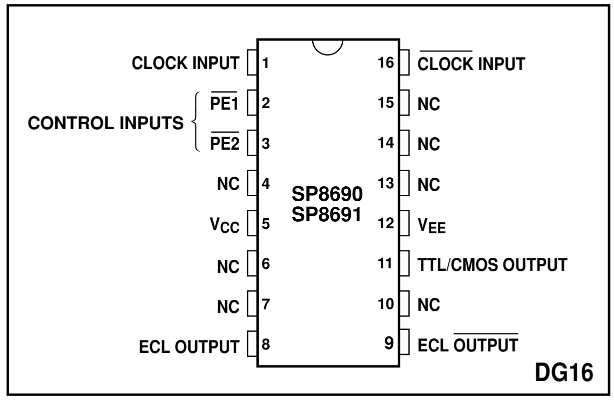


Fig. 1 Pin connections - top view

FEATURES

- ECL and TTL/CMOS Compatible Outputs
- AC-Coupled Input
- Control Inputs ECL Compatible

QUICK REFERENCE DATA

- Supply Voltage: −5·2V±0·25V (ECL), 5V±0·25V (TTL)
- Power Consumption: 70mW (Typ.)
- Temperature Range:
  - −55°C to +125°C (A Grade)
  - −30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage, $\lvert V_{CC} - V_{EE} \rvert$	8V
ECL output current	10mA
Storage temperature range	−65°C to +150°C
Max. junction temperature	+175°C
TTL output voltage	+12V
Input voltage	2·5V p-p
Max. open collector current	15mA

ORDERING INFORMATION

SP8690 A DG
SP8690 B DG
SP8691 A DG
5962-87678 (SMD) (SP8690)

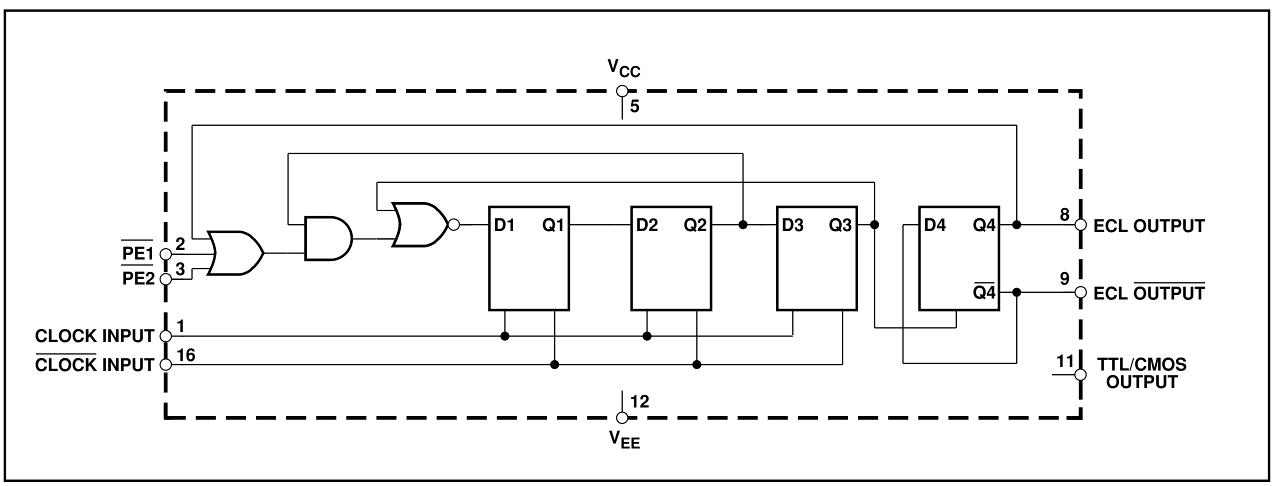


Fig. 2 Functional diagram (SP8690)

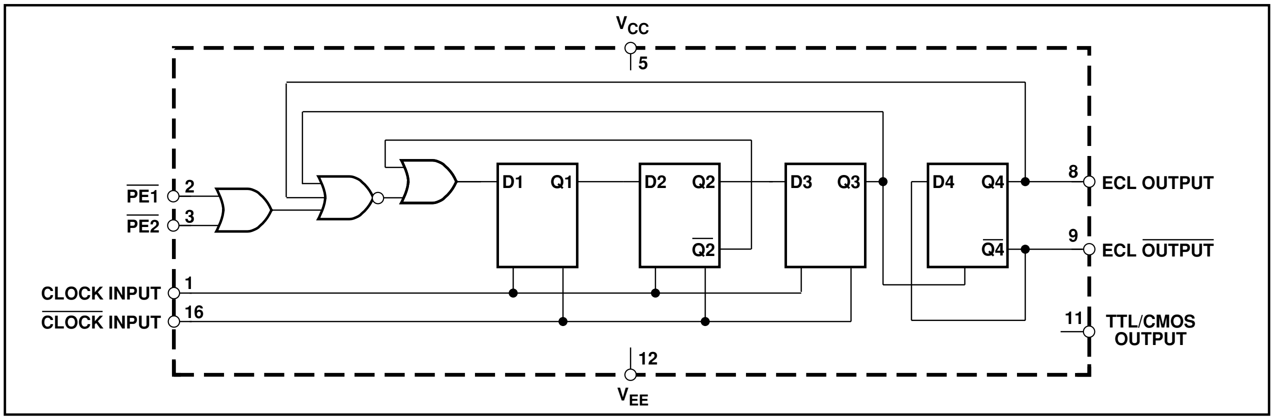


Fig. 3 Functional diagram (SP8691)

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range

ECL OPERATION

Supply voltage, V_{CC} = 0V, V_{EE} = −5·2V ± 0·25V
Temperature, T_{AMB} = −55°C to +125°C (A Grade), −30°C to +70°C (B Grade)

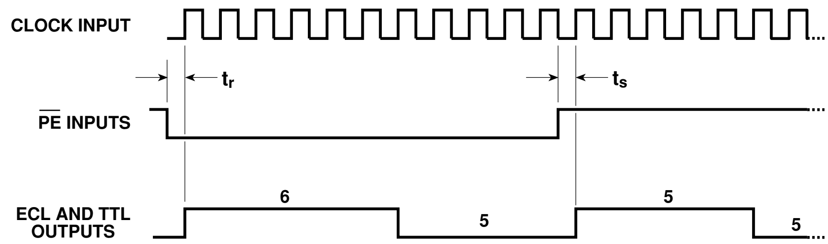
Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{MAX}	200		MHz	Input = 400-800mV p-p	5
Minimum frequency (sinewave input)	f_{MIN}		40	MHz	Input = 400-800mV p-p	5
Power supply current	I_{EE}		21	mA	V_{EE} = −5·0V	5
ECL output high voltage	V_{OH}	−0·85	−0·7	V	V_{EE} = −5·2V (25°C)	
ECL output low voltage	V_{OL}	−1·8	−1·5	V	V_{EE} = −5·2V (25°C)	
PE input high voltage	V_{INH}	−0·93		V	V_{EE} = −5·2V (25°C)	
PE input low voltage	V_{INL}		−1·62	V	V_{EE} = −5·2V (25°C)	
Clock to ECL output delay	t_p		9	ns		6
Set-up time	t_s	3		ns		3, 6
Release time	t_r	8		ns		4, 6

TTL OPERATION

Supply voltage, V_{CC} = 5V ± 0·25V, V_{EE} = 0V
Temperature, T_{AMB} = −55°C to +125°C (A Grade), −30°C to +70°C (B Grade)

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{MAX}	200		MHz	Input = 400-800mV p-p	5
Minimum frequency (sinewave input)	f_{MIN}		40	MHz	Input = 400-800mV p-p	5
Power supply current	I_{EE}		21	mA	V_{CC} = 5·0V	5
TTL output low voltage	V_{OL}		0·5	V	V_{CC} = 5V, R_L = 560Ω	5, 7
TTL output high voltage	V_{OH}	3·75		V	R_L = 560Ω	5, 7
Clock to TTL output high delay, +ve going	t_{PLH}		32	ns	R_L = 560Ω	6
Clock to TTL output low delay, −ve going	t_{PHL}		18	ns	R_L = 560Ω	6
Set-up time	t_s	3		ns		3, 6
Release time	t_r	8		ns		4, 6

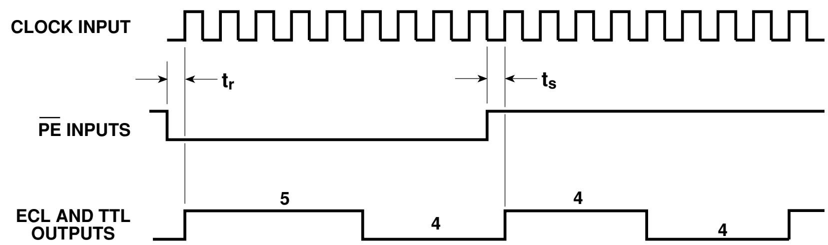
NOTES
1. The temperature coefficients of V_{OH} = +1·63mV/°C, V_{OL} = +0·94mV/°C and of V_{IN} = +1·22mV/°C.
2. The test configuration for dynamic testing is shown in Fig.8
3. The set-up time t_S is defined as the minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure that division by the lower modulus is obtained.
4. The release time t_r is defined as the minimum time that can elapse between H→L transition of control input and the next L→H clock pulse transition to ensure that division by the higher modulus is obtained.
5. SP8690/1B tested at 25°C only.
6. Guaranteed but not tested.
7. The open collector output is not recommended for use at output frequencies above 15MHz. C_{LOAD} ≤ 5pF.



TRUTH TABLE FOR CONTROL INPUTS

PE1	PE2	Division ratio
L	L	11
H	L	10
L	H	10
H	H	10

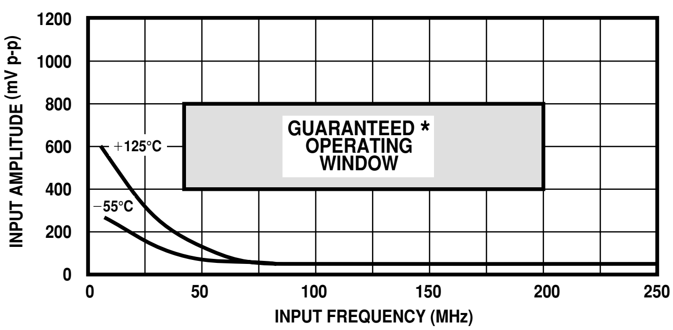
Fig. 4 Timing diagram, SP8690



TRUTH TABLE FOR CONTROL INPUTS

PE1	PE2	Division ratio
L	L	9
H	L	8
L	H	8
H	H	8

Fig. 5 Timing diagram, SP8691



* Tested as specified in table of Electrical Characteristics

Fig. 6 Typical input characteristics, SP8690/1

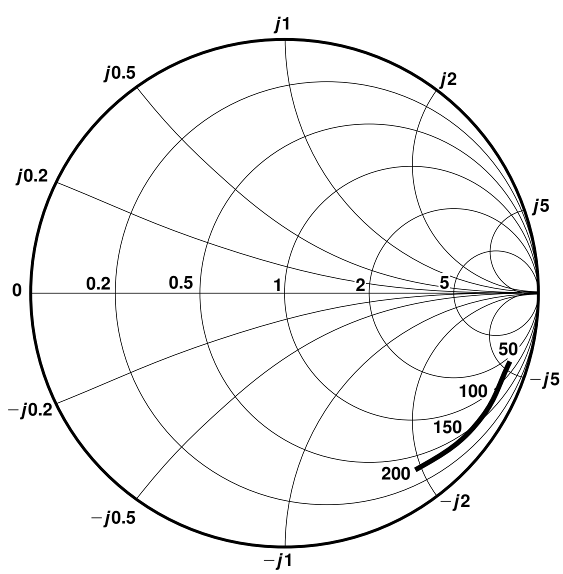


Fig. 7 Typical input impedance. Test conditions: Supply Voltage = 5.0V, Ambient Temperature = 25°C. Frequencies in MHz, impedances normalised to 50Ω.

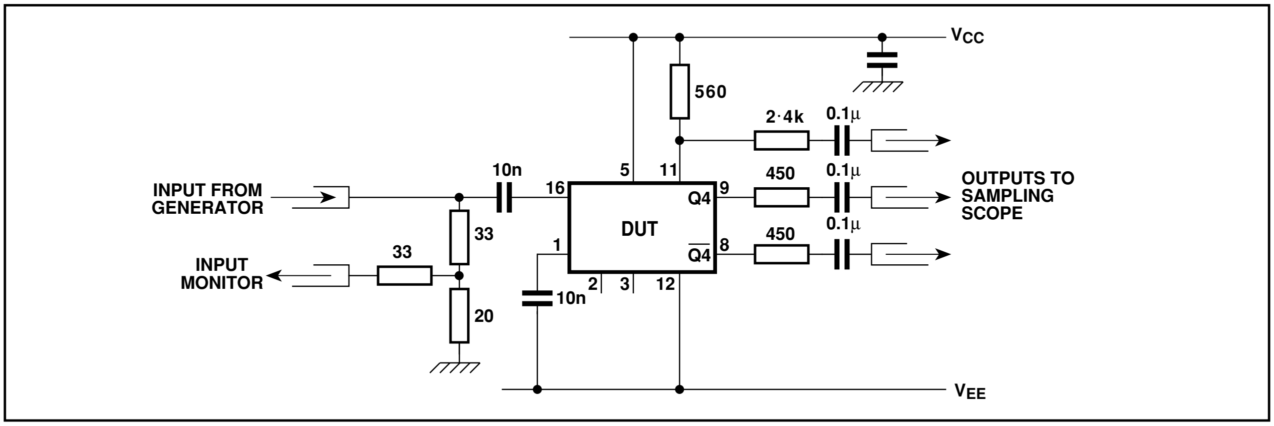


Fig. 8 Test circuit for dynamic measurements

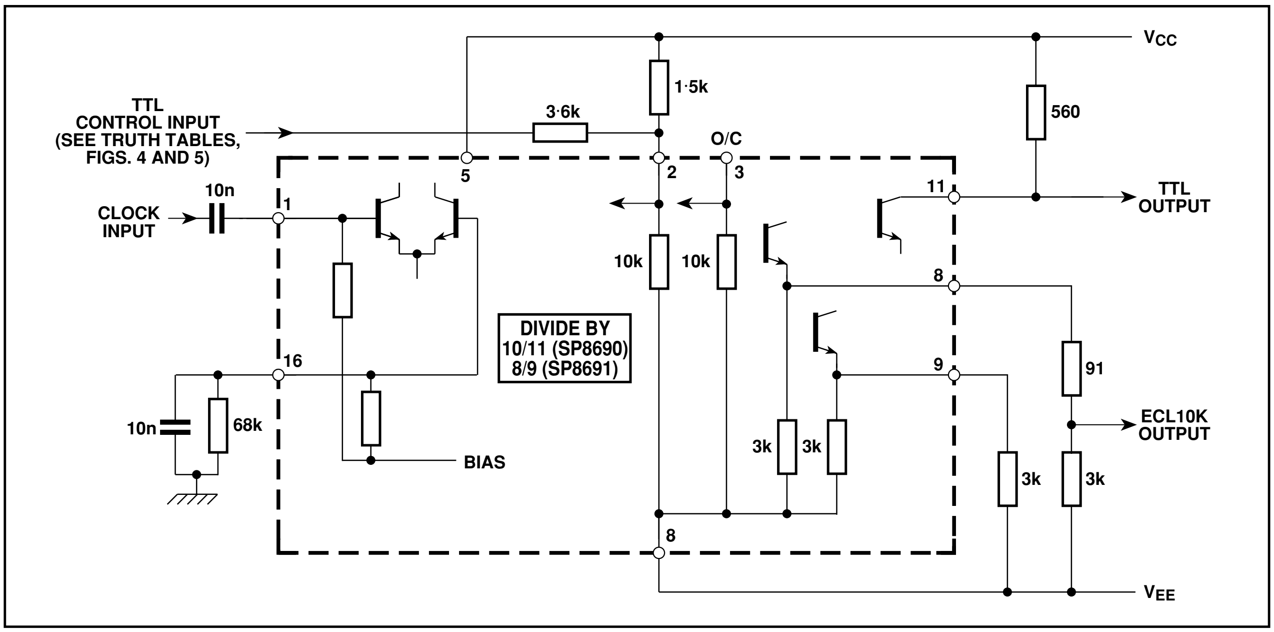


Fig. 9 Typical application showing interfacing.

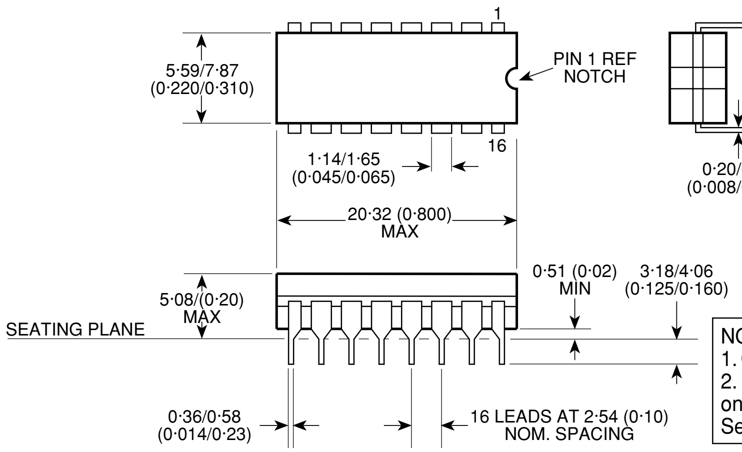
OPERATING NOTES

1. The clock inputs can be single or differentially driven. The clock input is biased internally and is coupled to the signal source with a suitable capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to ground.
2. In the absence of a signal the device will self-oscillate. If this is undesirable, it may be prevented by connecting a 68kΩ resistor from the input to V_{EE} i.e., from pin 1 or pin 16 to pin 12. This reduces the input sensitiviy by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/µs.
4. The Q_4 and $\overline{Q}_4$ outputs are compatible with ECLII but can be interfaced to ECL10K as shown in Fig. 9.
5. The PE inputs are ECLIII/10K compatible and include internal 10kΩpulldown resistors. Unused inputs can therefore be left open circuit.
6. The input impedance of the SP8690/1 varies as a function of frequency. See Fig. 7.
7. The TTL/CMOS output is a free collector and the high state output voltage will depend on the supply that the collector load is taken to. This should not exceed 12V.
8. The rise/fall time of the open collector output waveform is directly proportional to load capacitance and load resistor value. Therefore, load capacitance should be minimised and the load resistor kept to a minimum consistent with system power requirements. In the test configuration of Fig. 8 the output rise time is approximately 10ns and the fall time

NOTES

PACKAGE DETAILS

Dimensions are shown thus: mm (in).



NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

16-LEAD CERAMIC DIL – DG16

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