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ADVANCE INFORMATION
DS3674-1·2

SP8755

1200MHz÷64

The SP8755 is a divide by 64 prescaler which operates from a standard 5V TTL supply and will drive TTL directly. The SP8755A operates over the full military temperature range (−55°C to +125°C).

FEATURES

- TTL Compatible Output
- AC Coupled Input (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: 5V
- Power Consumption: 270mW
- Temperature Range: −55°C to +125°C (A Grade)
  −30°C to +70°C (B Grade)

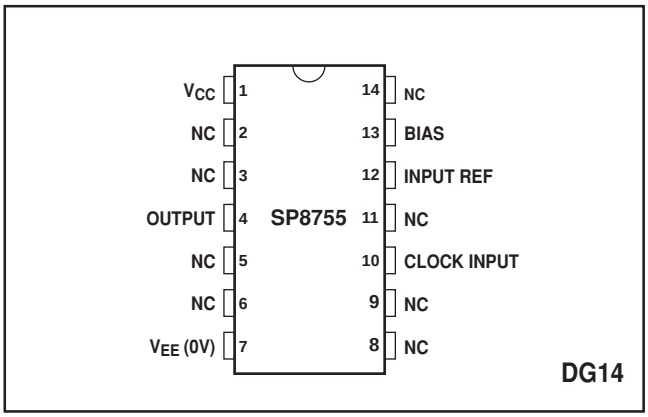


Fig. 1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Output current	±30mA
Storage temperature range	−65°C to +150°C
Max. junction temperature	+175°C
Max. clock input voltage	2·5V p-p

ORDERING INFORMATION

SP8755 A DG
SP8755 B BG
SP8755 NA 1C
5962-88684 (SMD)

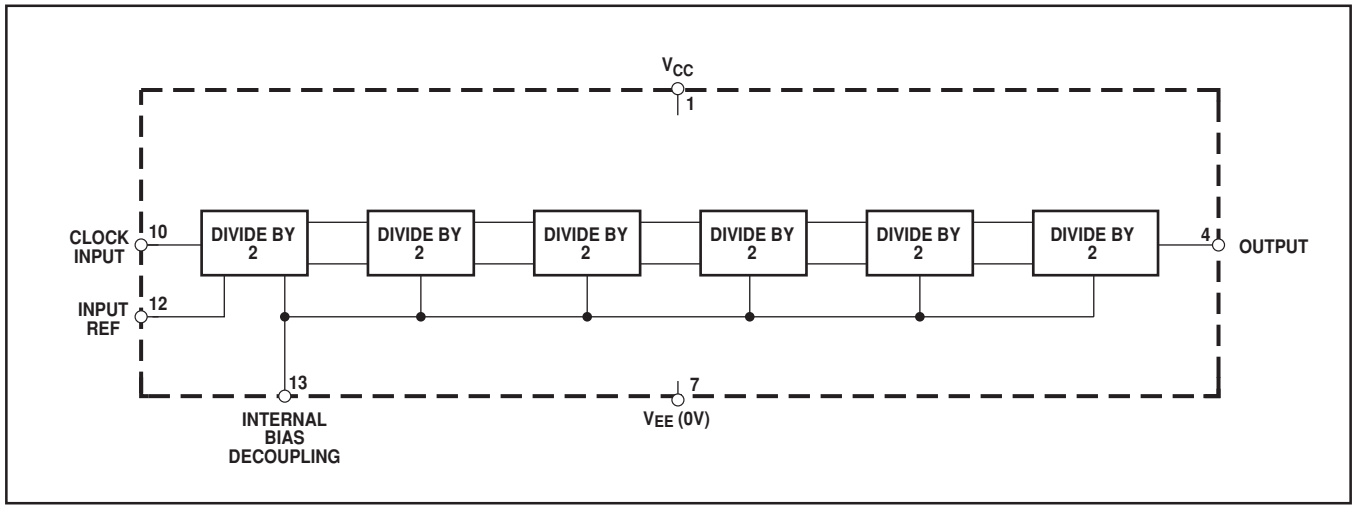


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range
Supply voltage, V_{CC} = 5·0V±0·25V, V_{EE} = 0V
Temperature, T_{AMB} = −55°C to +125°C (A Grade), −30°C to +70°C (B Grade)

Characteristic	Symbol	Value		Units	Grade	Conditions
		Min.	Max.			
Maximum frequency (sinewave input)	f_{MAX}	1·2		GHz	SP8755A	Input = 600-1200mV p-p
	f_{MAX}	1·2		GHz	SP8755B	Input = 400-1200mV p-p
Minimum frequency (sinewave input)	f_{MIN}		100	MHz	Both	Input = 600-1200mV p-p
Power supply current	I_{CC}		75	mA	Both	
Output high voltage	V_{OH}	2·5		V	Both	
Output low voltage	V_{OL}		0·45	V	Both	Sink current = 5mA

NOTES
1. The test configuration for dynamic testing is shown in Fig.5.
2. Above characteristics are not tested at 25°C only (tested ar low and high temperatures only).

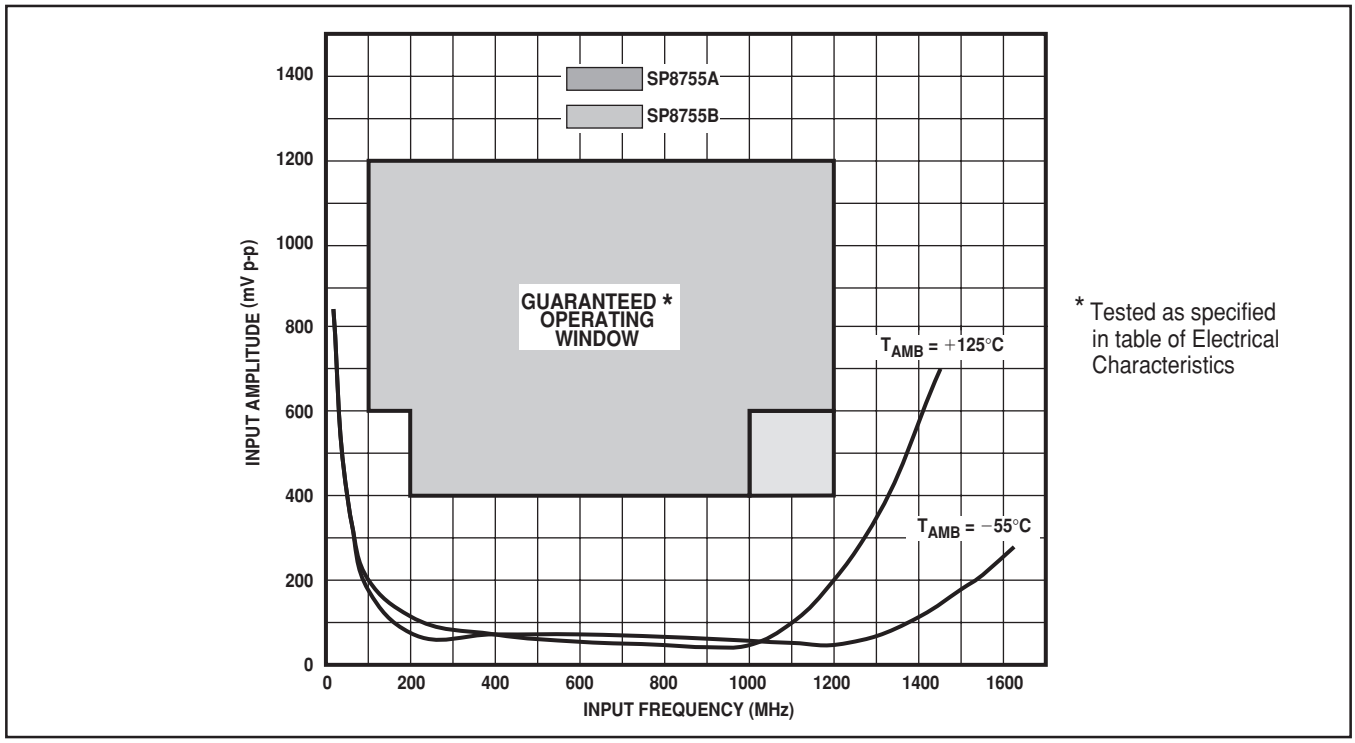


Fig. 3 Typical input characteristic of SP8755A/B

OPERATING NOTES

1.The clock input is biased internally and is connected to the signal source via a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting an 18kΩ resistor between the input and V_{EE} (i.e. from pin 10 to pin 7). This will reduce sensitivity by approximately 100mV.
3. The device will operate down to DC but input slew rate must be better than 100V/μs.
4. The output is a standard totem pole TTL and can therefore be interfaced directly to TTL.

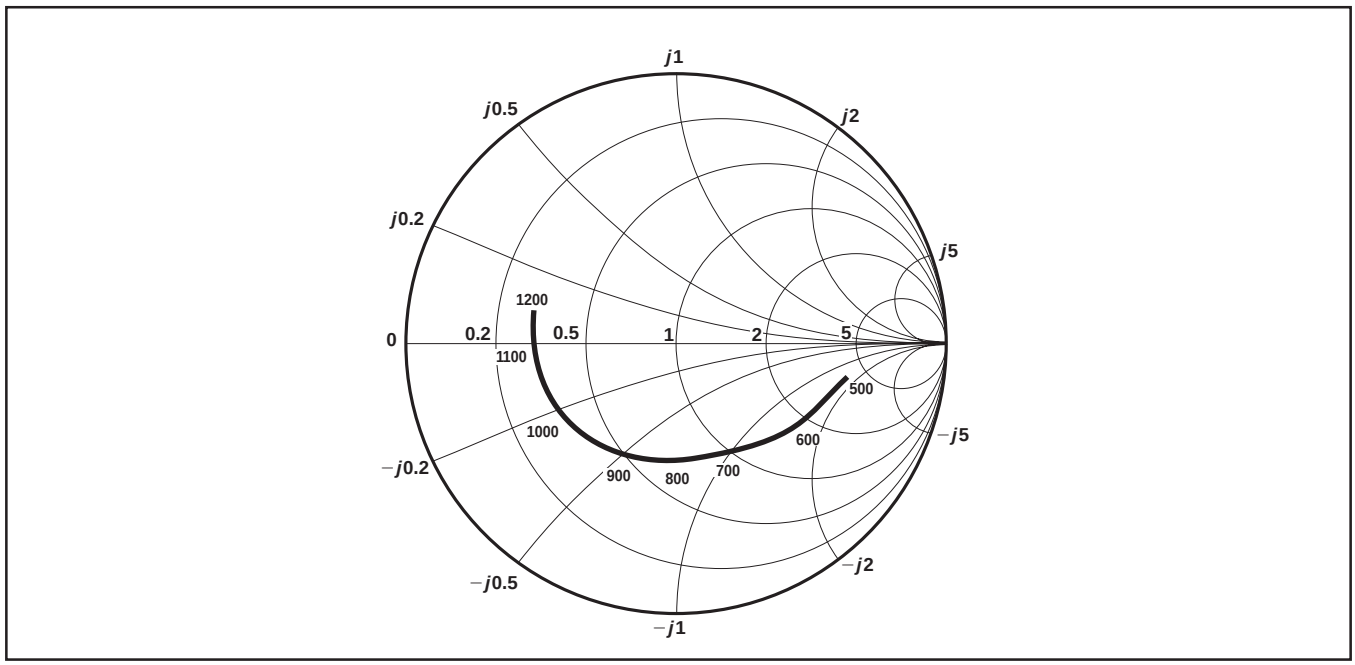


Fig. 4 Typical input impedance. Test conditions: supply voltage = 5·2V, ambient temperature = 25°C, frequencies in MHz, Impedances normalised to 50Ω

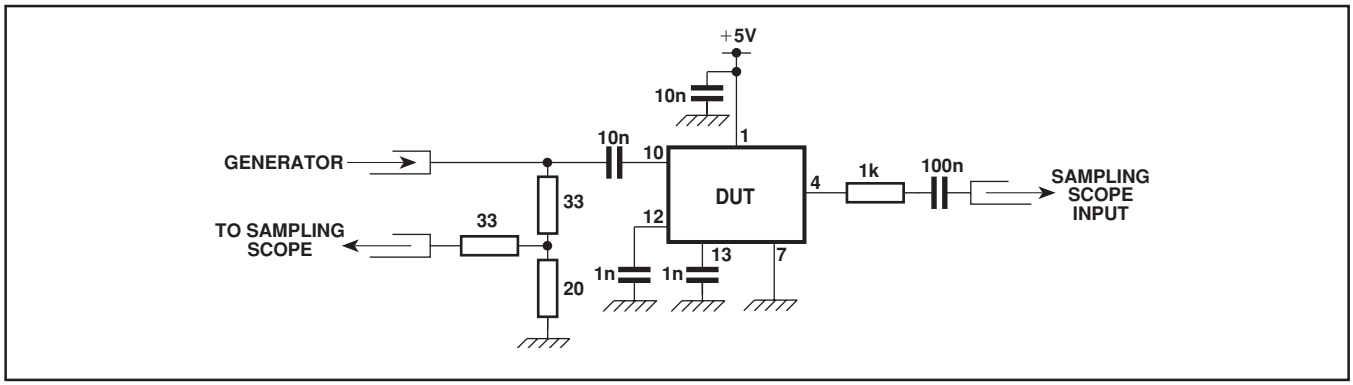


Fig. 5 Test circuit

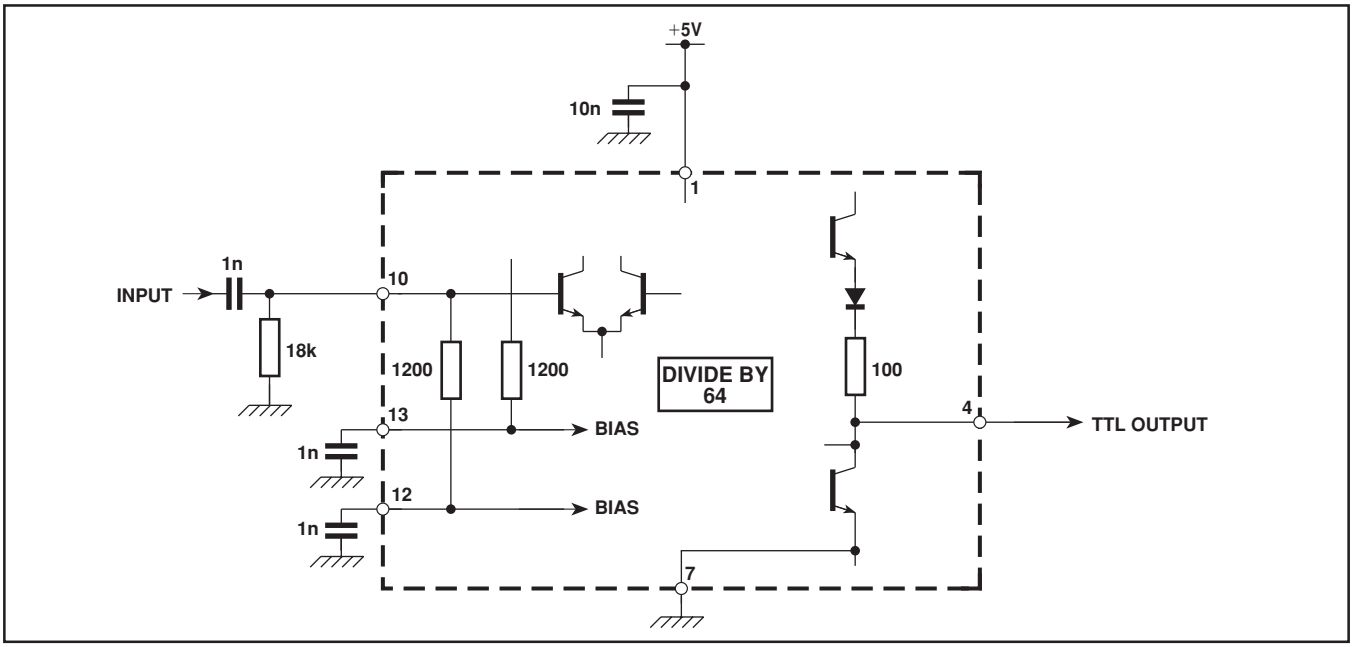
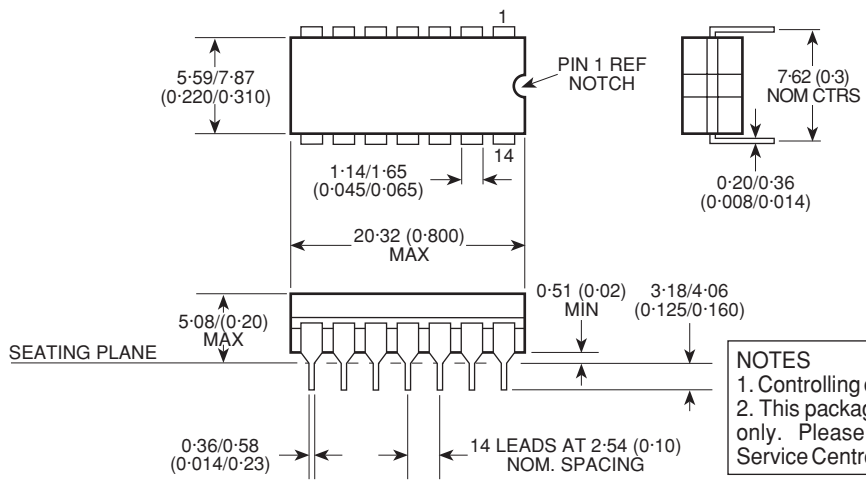


Fig. 6. Typical application circuit showing interfacing

PACKAGE DETAILS

Dimensions are shown thus: mm (in).



NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

14-LEAD CERAMIC DIL – DG14

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