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SP8792 225MHz ÷ 80/81

SP8793 225MHz ÷ 40/41

WITH ON-CHIP VOLTAGE REGULATOR

The SP8792 AND SP8793 are low power programmable ÷80/81 and ÷40/41 counter, temperature range: -40°C to +85°C. They divide by 80(40) when control input is in the high state and by 81(41) when in the low state. An internal voltage regulator allows operation from a wide range of supply voltages.

FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input
- Operation up to 9.5V using Internal Regulator

QUICK REFERENCE DATA

- Supply Voltage 5.2V or 6.8V to 9.5V
- Power consumption: 26mW Typical

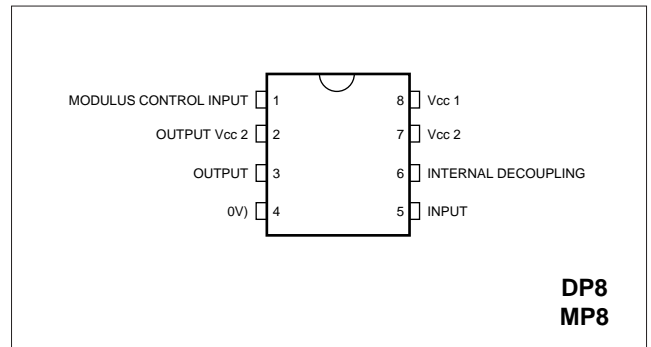


Figure 1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6.0V pins 7 & 8 tied
Supply voltage	13.5V pin 8, pin 7 decoupled
Storage temperature range	-55°C to +125°C
Max. Junction temperature	+175°C
Max. clock input voltage	2.5V p-p
Vcc2 max.	10V

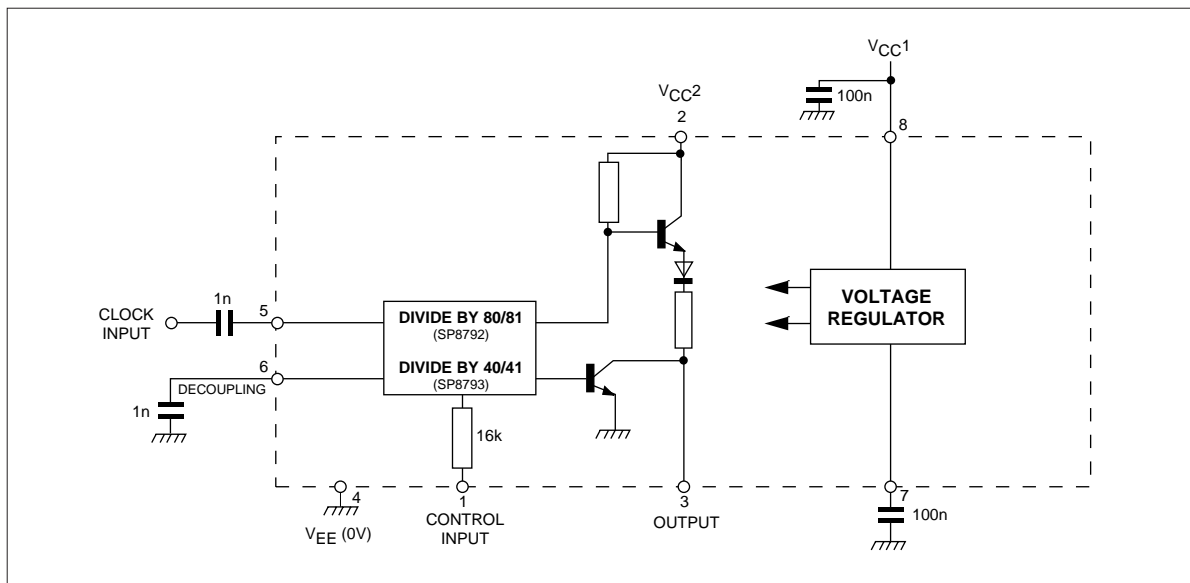


Figure 2 : Functional diagram SP8799

SP8793

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):]

Supply voltage : $V_{CC} = 5.2 \pm 0.25V$ or $6.8V$ to $9.5V$ (see Operating Note 6): $V_{EE} = 0V$

Temperature $T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$

Characteristics	Symbol	Value		Units	Notes	Conditions
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	225		MHz	Note 4	Input = 200-800mV p-p
Minimum frequency (sinewave input)	f_{min}		20	MHz	Note 4	Input = 400-800mV p-p
Power supply current	I_{EE}		7	mA	Note 4	
Control input high voltage	V_{INH}	4		V	Note 4	
Control input low voltage	V_{INL}		2	V	Note 4	
Output high voltage	V_{OH}	2.4		V	Note 4	Pins 2, 7 and 8 linked $V_{CC} = 4.95V$ $I_{OH} = 100\mu A$
Output low voltage	V_{OL}		0.5	V	Note 4	Pin 2 linked to 8 and 7 $I_{OL} = 1.6mA$
Set up time	t_s	14		ns	Note 3	25°C
Release time	t_r	20		ns	Note 3	25°C
Clock to output propagation time	t_p		45	ns	Note 3	25°C

NOTES

1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested onlt at 25°C

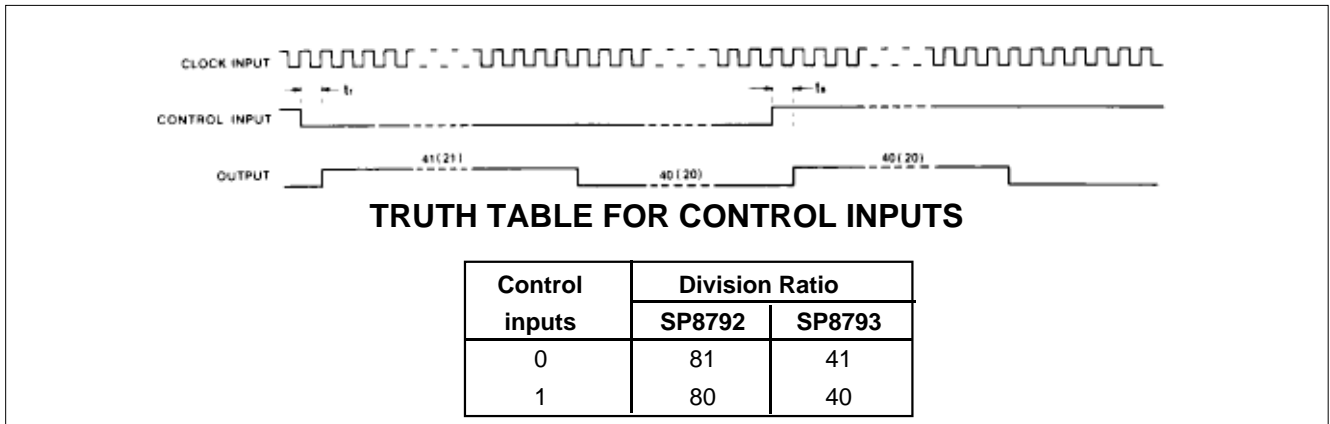
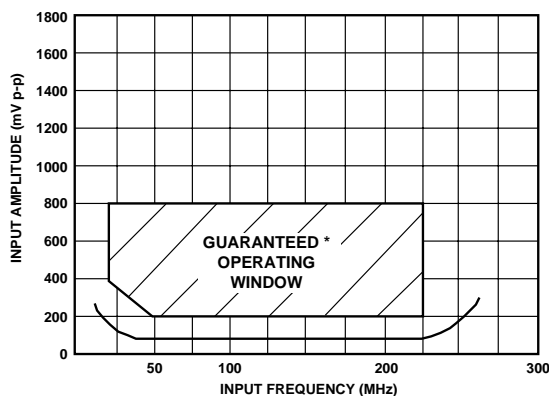


Figure 3 : Timing diagram SP8792/3

NOTES

The set-up time t_s is defined as the minimum time that can elapse between a L → H transition of the control input and the next L → H clock pulse transition to ensure ÷ 80 or 40 mode is selected.

The release time t_r is defined as the minimum time that can elapse between a H → L transition of the control input and the next L → H clock pulse transition to ensure ÷ 81 or 41 mode is selected.



*Tested as specified
in table of
Electrical Characteristics

Figure 4 : Input sensitivity SP8792/SP8793

OPERATING NOTES

1. The clock input (Pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, Pin 6 to ground.
2. The output stage which is normally open collector (Pin 2 open circuit) can be interfaced to CMOS. The open collector can be returned to a +10V line via a 5k resistor but the output sink current should not exceed 2mA. If interfacing to TTL is required then Pins 2 and 7 should be connected together to give a fan-out = 1. This will increase supply current by approximately 2mA.
3. The circuit will operate down to DC but a slew rate of better than 20V/~s is required.
4. The mark space ratio of the output is approximately 1.2:1 at 200MHz.
5. Input impedance is a function of frequency. See Fig.5.
6. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.
7. The internal regulator has its input connected to Pin 8, while the internal reference voltage appears at Pin 7 and should be decoupled. For use from a 5.2V supply, Pins 7 and 8 should be connected together, and 5.2V applied to these pins. For operation from supply voltages in the range +6.8V to +9.5V, Pins 7 and 8 should be separately decoupled, and the supply voltage applied to Pin 8.

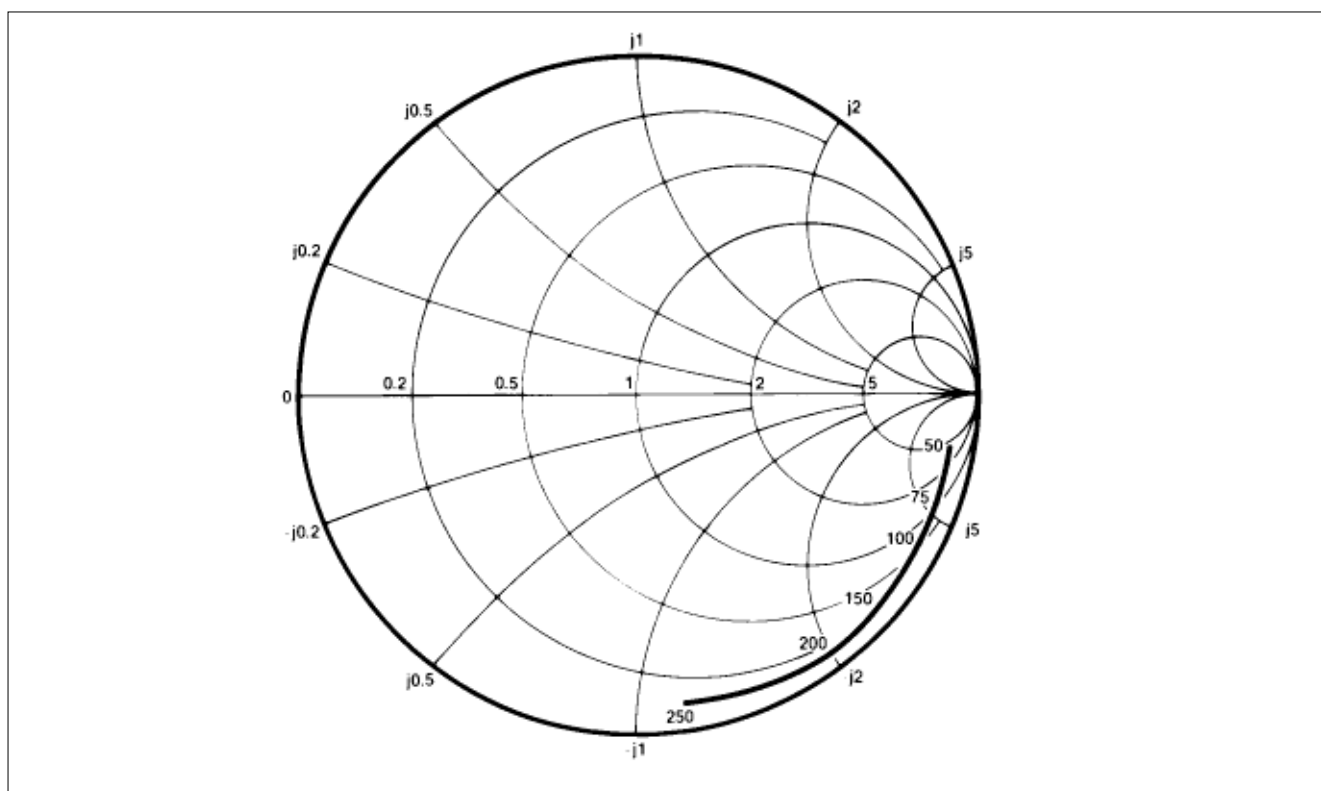


Figure 5 : Typical impedance. Test conditions: supply voltage 5.2V, ambient temperature 25°C, frequencies in MHz, impedance normalised to 50 ohms.

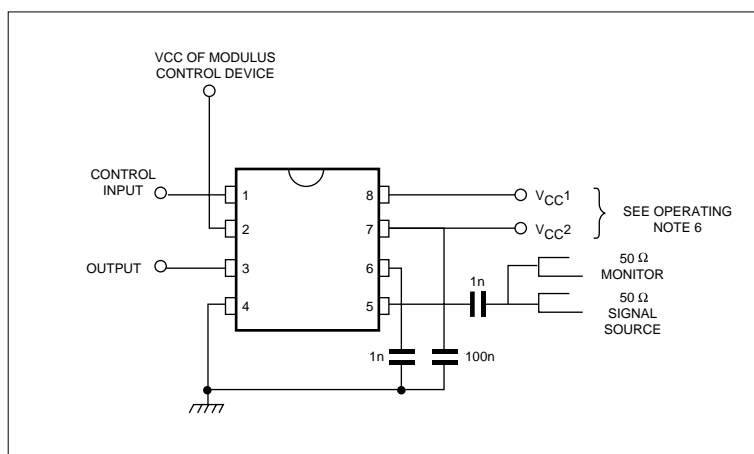


Figure 6 : Toggle frequency test circuit



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