SP8852E

2·7GHz Parallel Load Professional Synthesiser

Preliminary Information

Supersedes January 1996 version, DS4237 - 1.2

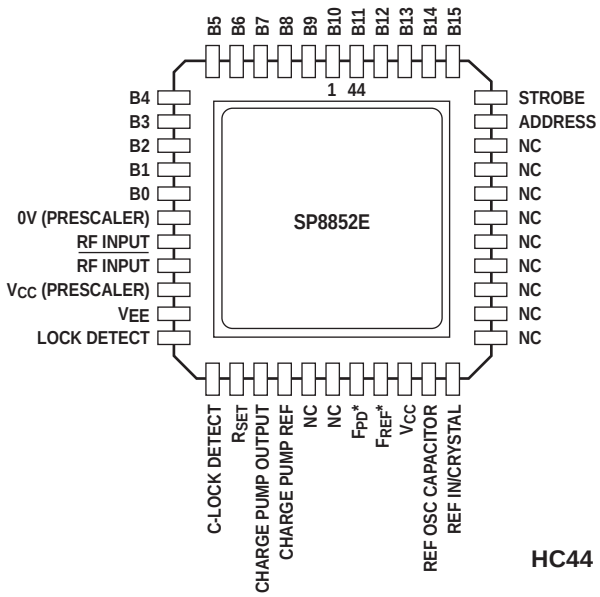
DS4237 - 2.0 June 1998

The SP8852E is one of a family of parallel load synthesisers containing all the elements apart from the loop amplifier to fabricate a PLL synthesis loop. Other parts in the series are the SP8854E which has hard wired reference counter programming and requires only a single 16-bit programming word, and the SP8855E which is fully programmable using hard wired links or switches.

The SP8852E is programmed using a 16-bit parallel data bus. Data can be stored in one of two internal buffers, selected by a single address bit on the input interface. In order to fully program the device, two 16-bit words are required, one to select the RF division ratio (A and M counters) and phase detector gain, and one to set the 10-bit reference divider count, phase detector state and sense. Once the reference divide ratio has been set, frequency changes can be made by a single 16-bit data load entry to the RF divider chain.

FEATURES

- 2·7 GHz Operating Frequency
- Single 5V Supply
- Low Power Consumption <1·3W
- High Comparison Frequency : 20MHz
- High Gain Phase Detector : 1mA/rad
- Zero 'Dead Band' Phase Detector
- Wide Range of RF and Reference Division Ratios
- Programming by Dual Word Data Transfer



*F_{PD} and F_{REF} outputs are reversed by the phase detector sense bit in the F1/F2 programming word, bit 12. The above diagram is correct when bit 12 is high.

Fig. 1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage	−0·3V to +6V
Operating temperature	−55°C to+100°C
Storage temperature	−65°C to +150°C
Prescaler and reference input voltage	2·5Vp-p
Data inputs	V_{CC} +0·3V
	V_{EE} −0·3V
Junction temperature	+175°C

THERMAL DATA

θ_{JC} = 5°C/W

θ_{JA} = 53°C/W

ESD PROTECTION

1000V, human body model

ORDERING INFORMATION

SP8852E KG HCAR Non-standard temperature range, −55°C to +100°C, standard product screening

SP8852E IG HCAR Industrial temperature range, −40°C to +85°C, standard product screening

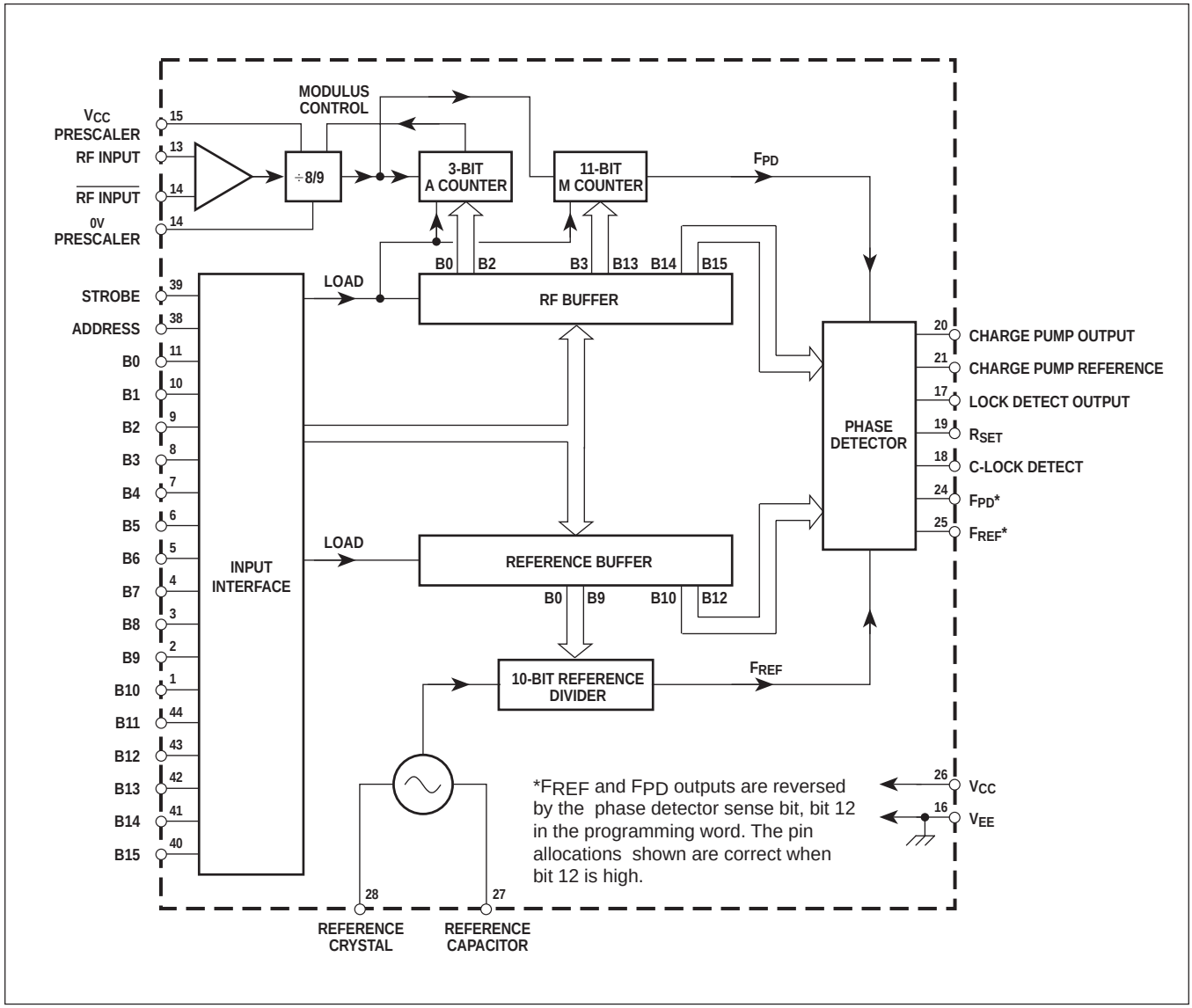


Fig. 2 Block diagram

Pin	Description
1-11, 40-44	These are the inputs to the 16-bit data bus. When pin 38 is high the data goes to the buffers for the A counter, M counter and phase detector gain. When pin 38 is low the data goes to the buffers for the reference counter and the phase detector state (see Table 4). Open circuit = 1 (high) on these pins. Data is transparent from pins to the selected buffers when pin 39 (STROBE) is high and frozen in buffers when pin 39 is low.
13 (RF INPUT) 14 ($\overline{\text{RF INPUT}}$)	Balanced inputs to the RF preamplifier. For single-ended operation the signal is AC-coupled into pin 13 with pin 14 AC-decoupled to ground (or vice-versa). Pins 13 and 14 are internally DC biased.
17 (LOCK DETECT INPUT)	A current sink into this pin is enabled when the lock detect circuit indicates lock. Used to give an external indication of phase lock.
18 (C-LOCK DETECT)	A capacitor connected to this point determines the lock detect integrator time constant and can be used to vary the sensitivity of the phase lock indicator.
19 (R_{SET})	An external resistor from pin 19 to V_{CC} sets the charge pump output current.
20 (CHARGE PUMP OUTPUT)	The phase detector output is a single ended charge pump sourcing or sinking current to the inverting input of an external loop filter. The direction is controlled by bit 12 of the reference word. For bit 12 = 1 and F_{PD} or RF phase leads Ref phase pin 20 will sink current (see Table 3).
21 (CHARGE PUMP REF)	Connected to the non-inverting input of the loop filter to set the optimum DC bias.
22	Not Connected.
23	Not connected.
24 F_{PD} if pin 23 is high F_{REF} if pin 23 is low	RF divider output pulses. F_{PD} = RF input frequency/(M.N+A). Pulse width = 8 RF input cycles (1 cycle of the divide by 8 prescaler output).
25 F_{PD} if pin 23 is low F_{REF} if pin 23 is high	Reference divider output pulses. F_{REF} = reference input frequency/R. Pulse width = high period of Ref input.
27 (Ref. oscillator capacitor)	Leave open circuit if an external reference is used. See Fig. 5 for typical connection for use as an onboard crystal oscillator.
28 (REF IN/XTAL)	This pin is the input buffer amplifier for an external reference signal. This amplifier provides the active element if an onboard crystal oscillator is used.
29-37	Not connected.
38 (ADDRESS)	Controls which buffer the data on the input bus goes to. Pin 38 high sends data to the RF divider group of functions. Pin 38 low sends data to the Ref divider group of functions (see Fig. 6). Open circuit = high.
39 (STROBE)	When pin 39 is high the A, M, and R counters are held in the reset state and the charge pump output is disabled. The data on the input bus is loaded into the buffers selected by the ADDRESS input state (pin 38) when pin 39 goes low. When pin 39 is low the data is fixed in the buffers, the buffers are loaded into the counter and control register, all the counters are active, and the charge pump is enabled. Open circuit = high.

Table 1 Pin descriptions

ELECTRICAL CHARACTERISTICS

The Electrical Characteristics are guaranteed over the following range of operating conditions unless otherwise stated

T_{AMB} = − 55°C to +100°C (KG parts), − 40°C to +85°C (IG parts); V_{CC} = 4·75V to 5·25V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	18, 26		180	240	mA	
RF input sensitivity	13,14	−5		+7	dBm	100MHz to 2·7GHz. See note 3.
RF division ratio	13,14, 24	56		16383		
Reference division ratio	28, 25	1		1023		
Comparison frequency	28, 24, 25			50	MHz	
Reference input frequency	28	10		100	MHz	Ref division ratio >2. See note 1
Reference input voltage	28	0	+6	+10	dBm	
F_{REF}/F_{PD} output voltage high	24, 25		−0·8		V	WRT V_{CC}, 2·2kΩ to 0V
F_{REF}/F_{PD} output voltage low	24, 25		−1·4		V	WRT V_{CC}, 2·2kΩ to 0V
LOCK DETECT output voltage	17		300	500	mV	I_{OUT} = 3mA
CHARGE PUMP current	19, 20, 21	±1·4	±1·5	±1·7	mA	$V_{PIN20} = V_{PIN21}$, I_{PIN19} = 1·6mA, multiplication factor = 1
		±2·0	±2·3	±2·5	mA	$V_{PIN20} = V_{PIN21}$, I_{PIN19} = 1·6mA, multiplication factor = 1·5
		±3·4	±3·8	±4·1	mA	$V_{PIN20} = V_{PIN21}$, I_{PIN19} = 1·6mA, multiplication factor = 2·5
		±5·4	±6·1	±6·5	mA	$V_{PIN20} = V_{PIN21}$, I_{PIN19} = 1·6mA, multiplication factor = 4·0
Input bus logic level high	1-11, 38-44	3·5			V	
Input bus logic level low	1-11, 38-44			1	V	
Input bus current source	1-11, 38-44	−200			µA	V_{IN} = 0V
Input bus current sink	1-11, 38-44			10	µA	$V_{IN} = V_{CC}$
Up/down current matching	20			±5	%	$V_{PIN20} = V_{PIN21}$, I_{PIN19} = 1·6mA
CHARGE PUMP REFERENCE voltage	21			V_{CC}−0·5	V	I_{PIN19} = 1·6mA, current multiplication factor = 1·0
		V_{CC}−1·6			V	I_{PIN19} = 1·6mA, current multiplication factor = 4·0
R_{SET} current	19	0·5		2	mA	Note 2
R_{SET} voltage	19		1·6		V	I_{PIN19} = 1·6mA
C-LOCK DETECT current	18		+10		µA	V_{PIN18} = 4·7V
STROBE pulse width		50			ns	Note 3
Data setup time		100			ns	Note 3

NOTES

1. Lower frequencies may be used provided that slew rates are maintained.
2. Pin 19 current×multiplication factor must be less than 5mA if charge pump accuracy is to be maintained.
3. Guranteed but not tested.

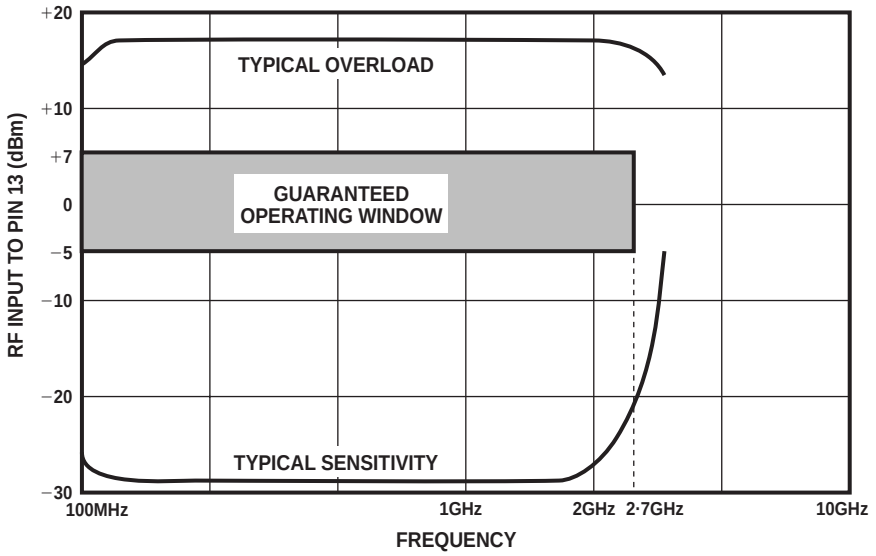


Fig. 3 Input sensitivity

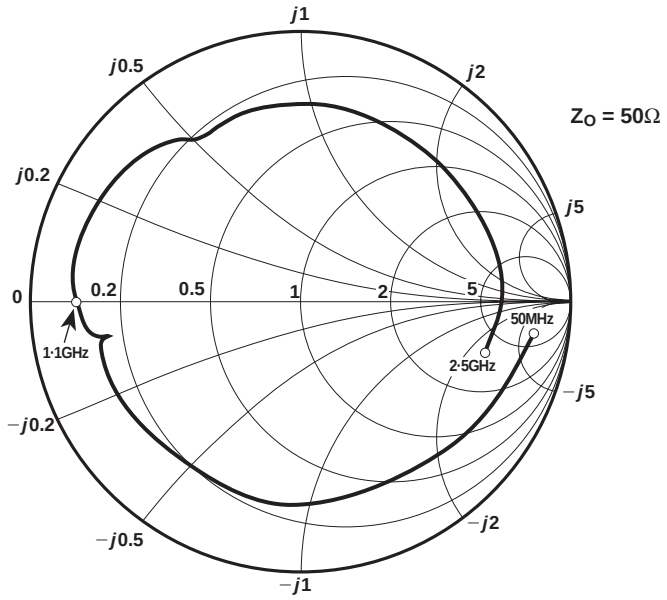


Fig. 4 RF input impedance

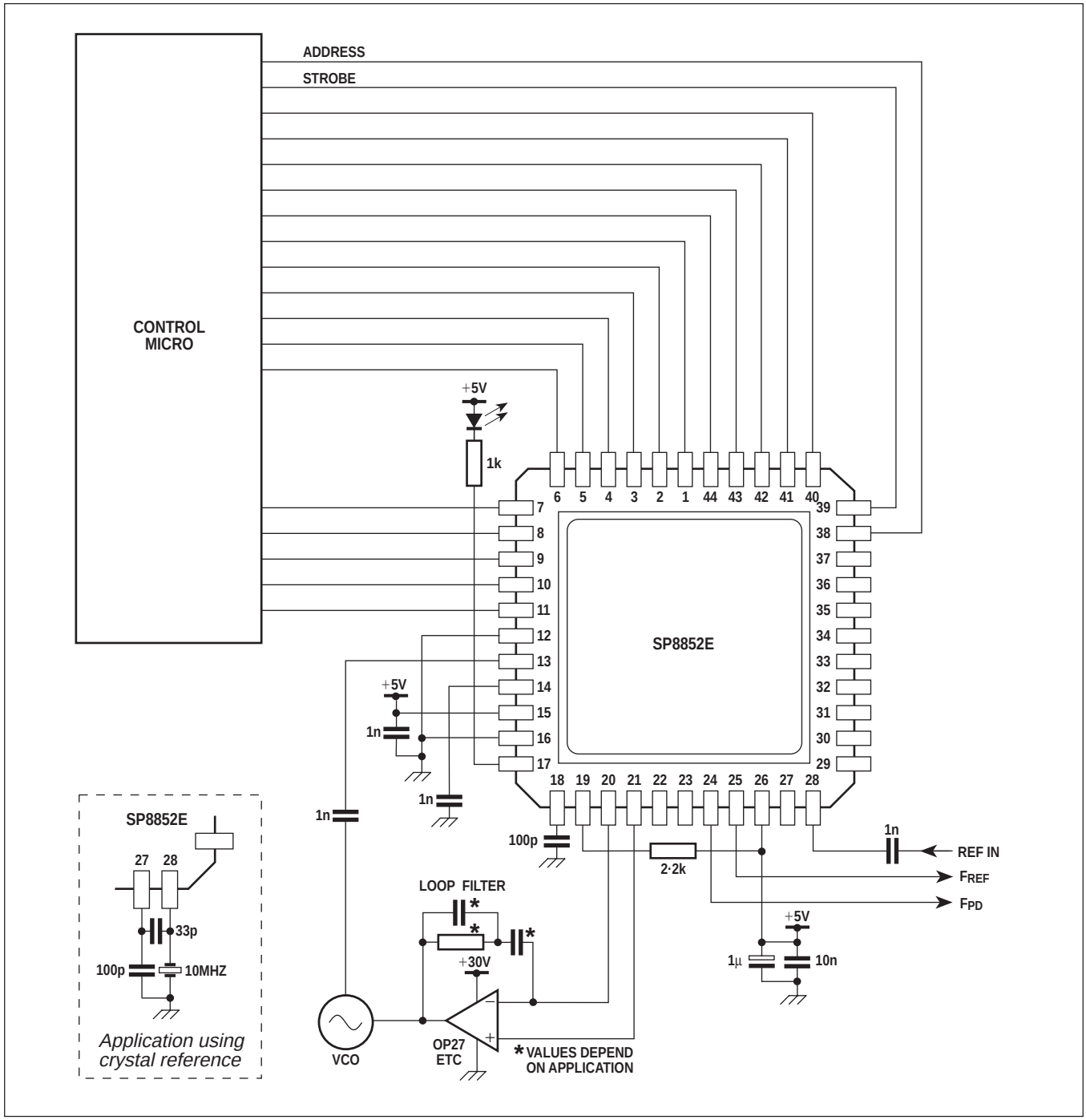


Fig. 5 Typical application diagram

DESCRIPTION

Prescaler and *AM* counter The programmable divider chain is of *A* and *M* counter construction and therefore contains a dual modulus front end prescaler, an *A* counter which controls the dual modulus ratio and an *M* counter which performs the bulk multi-modulus division. A programmable divider of this construction has a division ratio of $MN+A$ and a minimum integer steppable division ratio of $N(N-1)$, where *N* is the prescaler value.

Data Entry and Storage

Data is loaded from the 16-bit bus into one of the internal buffers by applying a positive pulse to the STROBE input. The input bus can be driven from TTL or CMOS logic levels. When STROBE is low, the inputs are isolated and the data can be changed without affecting the programmed state.

The data is loaded into the RF buffer when the address input is high and into the reference buffer when low. When the STROBE input is taken high, the *A* and *M* and reference counters are reset and the input data is applied to the internal storage register. When STROBE is again taken low, the data on the input bus is stored in the selected register and the counters released. The STROBE input is level triggered so that if the data is changed whilst the input is high, the final value before STROBE goes low will be stored.

In order to prevent disturbances on the VCO control voltage when frequency changes are made, the STROBE input disables

the charge pump outputs when high. During this period the VCO control voltage will be maintained by the loop filter components around the loop amplifier, but due to the combined effects of the amplifier input current and charge pump leakage a gradual change will occur. In order to reduce the change, the duration of the strobe pulse should be minimised. Selection of a loop amplifier with low input current will reduce the VCO voltage droop during the strobe pulse and result in minimum reference sidebands from the synthesiser.

Reference Input

The reference source can be either driven from an external sine or square wave source of up to 100MHz or a crystal can be connected as shown in Fig. 5.

Phase Comparator and Charge Pump

The SP8852E has a digital phase/frequency comparator driving a charge pump with programmable current output. The charge pump current level at the minimum gain setting is approximately equal to the current fed into the R_{SET} input, pin 19, and can be increased by programming the bus according to Table 2 by up to 4 times.

Bit 15	Bit 14	Current multiplication factor
0	0	1·0
0	1	1·5
1	0	2·5
1	1	4·0

Table 2

$$\text{Pin 19 current} = \frac{V_{CC} - 1{\cdot}6V}{R_{SET}}$$

$$\text{Phase detector gain} = \frac{I_{PIN19}\,(mA) \times \text{multiplication factor}}{2\pi}\ mA/rad$$

To allow for control direction changes introduced by the design of the PLL, bit 12 on the input bus address 0 can be programmed to reverse the sense of the phase detector by transposing the F_{PD} and F_{REF} connections. In order that any external phase detector will also be reversed by this programming bit, the F_{PD} and F_{REF} outputs are also interchanged by bit 12 as shown in Table 3.

Output for RF phase lag	
Sense bit (bit 12)	**Pin 20**
1	Current source
0	Current sink

Table 3

The F_{PD} and F_{REF} signals to the phase detector are available on pins 24 and 25 and may be used to monitor the frequency input to the phase detector or used in conjunction with an external phase detector. These outputs may be programmed by bits 10 and 11 of word 0 according to Table 4. State 3, where the outputs are disabled by the lock detect circuit, is useful where the user wishes to use an external phase detector. The internal phase/frequency detector may be used to pull the loop into lock and an automatic switch-over to the external phase detector made. When the F_{PD} and F_{REF} outputs are to be used at high frequencies, an external pull down resistor of minimum value 330Ω may be connected to ground to reduce the fall time of the output pulse.

Bit 11	Bit 10	Phase detector state
0	0	Enabled, F_{PD} and F_{REF} off
0	1	Enabled, F_{PD} and F_{REF} on
1	0	Disabled by lock detect, F_{PD} and F_{REF} on
1	1	Disabled, F_{PD} and F_{REF} on

Table 4

The charge pump connections to the loop amplifier consist of the charge pump output and the charge pump reference. The matching of the charge pump up and down currents will only be maintained if the charge pump output is held at a voltage equal to the charge pump reference using an operational amplifier to produce a virtual earth condition at pin 20. The lock detect circuit can drive an LED to give visual indication of phase lock or provide an indication to the control system if a pullup resistor is used in place of the LED. A small capacitor connected form the C-LOCK DETECTOR pin to ground may be used to delay lock detect indication and remove glitches produced by momentary phase coincidence during lock up.

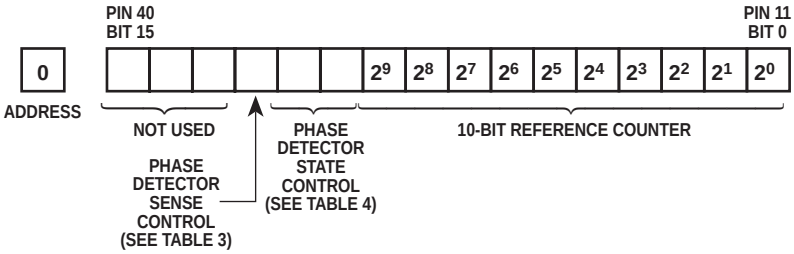


Fig. 6a Reference word bit allocation

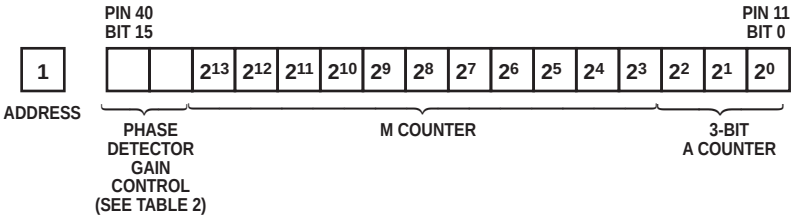


Fig. 6b RF division ratio bit allocation

Fig. 6 Programming data format

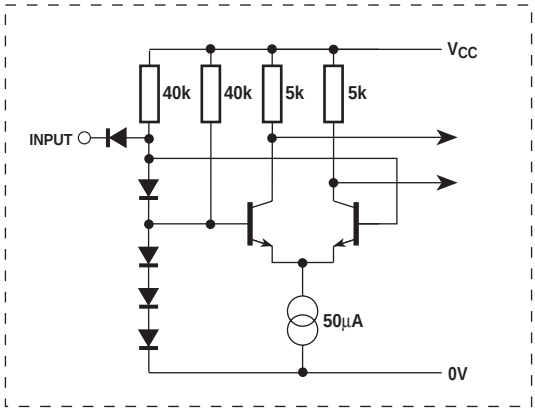


Fig. 7a 16-bit input bus, strobe and address

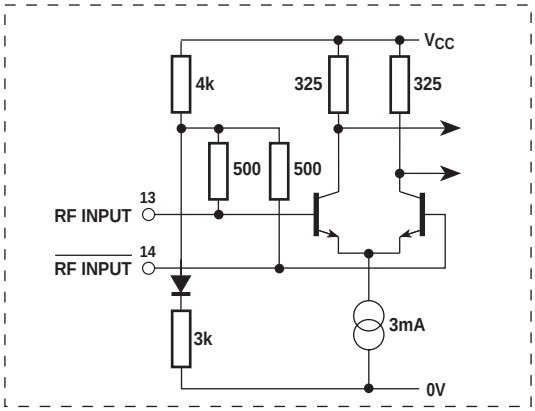


Fig. 7b RF inputs

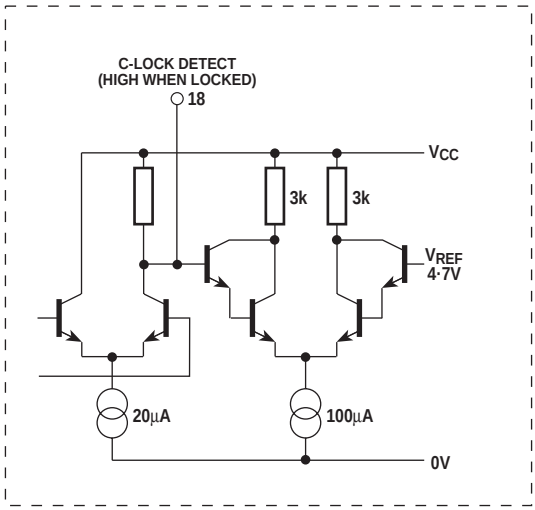


Fig. 7c Lock detect decouple

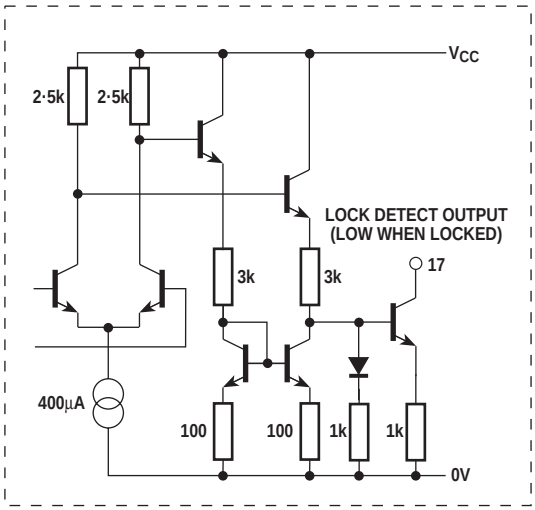


Fig. 7d Lock detect output

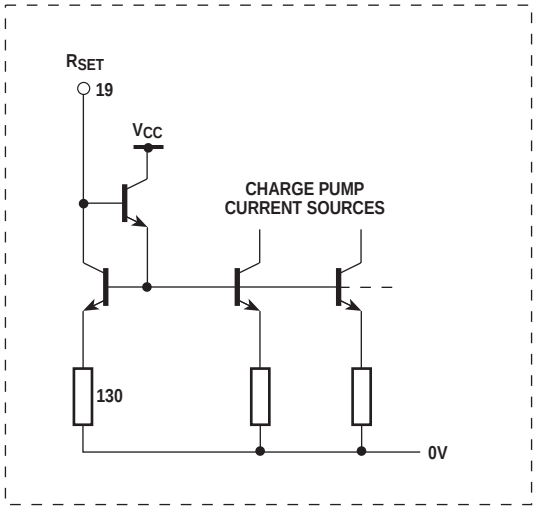


Fig. 7e R_{SET} pin

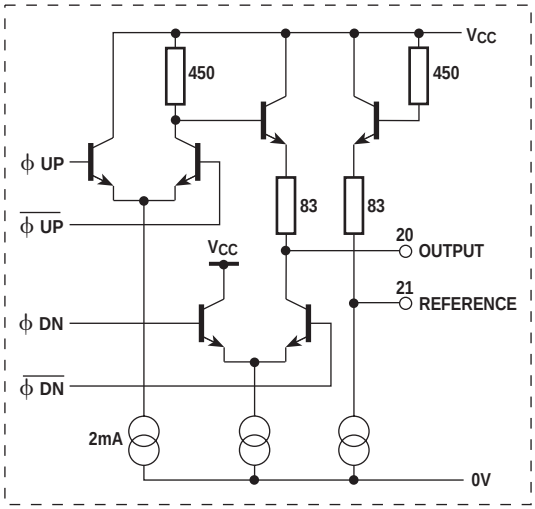


Fig. 7f Charge pump circuit

Fig 7 Interface circuit diagrams

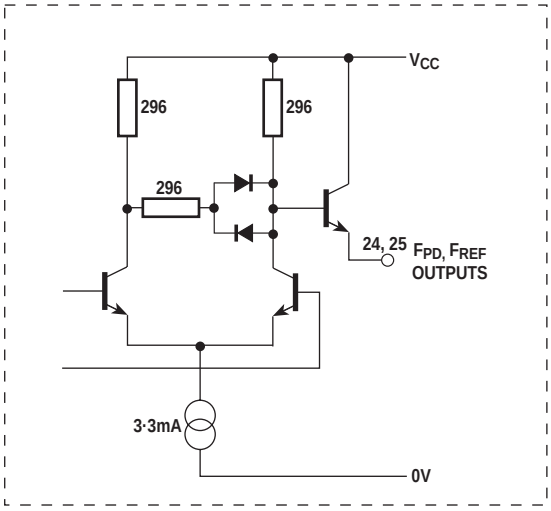


Fig. 7g F_{PD} and F_{REF} outputs

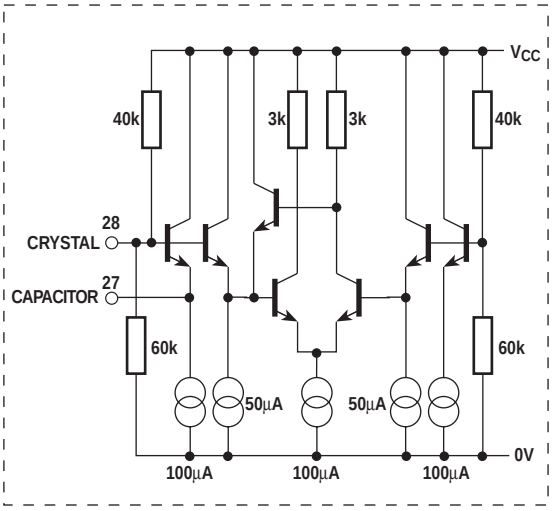


Fig. 7h Reference oscillator

Fig. 7 Interface circuit diagrams (continued)

APPLICATIONS

RF Layout

The SP8852E can operate with input frequencies up to 2·7GHz but to obtain optimum performance, good RF layout practices should be used. A suitable layout technique is to use double sided printed circuit board with through plated holes. Wherever possible the top surface on which the SP8852E is mounted should be left as a continuous sheet of copper to form a low impedance ground plane. The ground pins 12 and 16 should be connected directly to the ground plane.

Pins such as V_{CC} and the unused RF input should be decoupled with chip capacitors mounted as close to the device pin as possible, with a direct connection to the ground plane; suitable values are 10nF for the power supplies and <1nF for the RF input pin (a lower value should be used sufficient to give good decoupling at the RF frequency of operation). A larger decoupling capacitor mounted as close as possible to pin 26 should be used to prevent modulation of V_{CC} by the charge pump pulses. The R_{SET} resistor should also be mounted close to the R_{SET} pin to prevent noise pickup. The capacitor connected from the charge pump output should be a chip component with short connections to the SP8852E. All signals such as the programming inputs, RF IN, REFERENCE IN and the connections to the op-amp are best taken through the pc board adjacent to the SP8852D with through plated holes allowing connections to remote points without fragmenting the ground plane.

Programming Bus

The input pins are designed to be compatible with TTL or CMOS logic with a switching threshold set at about 2·4V by three forward biased base-emitter diodes. The inputs will be taken high by an internal pull up resistor if left open circuit but for best noise immunity it is better to connect unused inputs directly to V_{CC} or ground.

RF Inputs

The prescaler has a differential input amplifier to improve input sensitivity. Generally the input drive will be single ended and the RF signal should be AC coupled to either of the inputs using a chip capacitor.The remaining input should be decoupled to ground, again using a chip capacitor. The inputs can be driven differentially but the input circuit should not provide a DC path between inputs or to ground.

Lock Detect Circuit

The lock detect circuit uses the up and down correction pulses from the phase detector to determine whether the loop is in or out of lock. When the loop is locked, both up and down pulses are very narrow compared to the reference frequency, but the pulse width in the out of lock condition continuously varies, depending on the phase difference between the outputs of the reference and RF counters. The logical AND of the up and down pulses is used to switch a 20mA current sink to pin 18 and a 50kΩ resistor provides a load to V_{CC}. The circuit is shown in Fig. 7c.

When lock is established, the narrow pulses from the phase detector ensure that the current source is off for the majority of the time and so pin 18 will be pulled high by the 50kΩ resistor. A voltage comparator with a switching threshold at about 4·7V monitors the voltage at pin 18 and switches pin 17 low when pin 18 is more positive than the 4·7V threshold.

When the loop is unlocked, the frequency difference at the counter outputs will produce a cyclic change in pulse width from the phase detector outputs with a frequency equal to the difference at the reference and RF counter outputs. A small capacitor connected to pin 18 prevents the indication of false phase lock conditions at pin 17 for momentary phase coincidence. Because of the variable width pulse nature of the signal at pin 18 the calculation of a suitable capacitor value is complex, but if an indication with a delay amounting to several times the expected lock up time is acceptable, the delay will be approximately equal to the time constant of the capacitor on pin 18 and the internal 50kΩ resistor. If a faster indication is required, comparable with the loop lock up time, the capacitor will need to be 2 to 3 times smaller than the time constant calculation suggests. The time to respond to an out of lock condition is 2 to 3 times less than that required to indicate lock.

Charge Pump Circuit

The charge pump circuit converts the variable width up and down pulses from the phase detector into adjustable current pulses which can be directly connected to the loop amplifier. The magnitude of the current and therefore the phase detector gain can be modified when new frequency data is entered to compensate for change in the VCO gain characteristic over

its frequency band. The charge pump pulse current is determined by the current fed into pin 19 and is approximately equal to pin 19 current when the programmed multiplication ratio is 1. The circuit diagram Fig. 7e shows the internal components on pin 19 which mirror the input current into the charge pump. The voltage at pin 19 will be approximately 1·6V above ground due to two V_{BE} drops in the current mirror. This voltage will exhibit a negative temperature coefficient, causing the charge pump current to change with chip temperature by up to 10% over the full military temperature range if the current programming resistor is connected to V_{CC} as shown in the application diagram, Fig. 5. In critical applications where this change in charge pump current would be too large the resistor to pin 19 could be increased in value and connected to a higher supply to reduce the effect of V_{BE} variation on the current level. A suitable resistor connected to a 30V supply would reduce the variation in pin 19 current due to temperature to less than 1·5%. Alternatively a stable current source could be used to set pin 19 current.

The charge pump output on pin 20 will only produce symmetrical up and down currents if the voltage is equal to that on the voltage reference pin 21. In order to ensure that this voltage relationship is maintained, an operational amplifier must be used as shown in the typical application Fig. 5. Using this configuration pin 20 voltage will be forced to be equal to that on pin 21 since the operational amplifier differential input voltage will be no more than a few millivolts (the input offset voltage of the amplifier).

When the synthesiser is first switched on or when a frequency outside the VCO range is programmed, the amplifier output will limit, allowing pin 20 voltage to differ from that on pin 21. As soon as an achievable frequency value is programmed and the amplifier output starts to slew the correct voltage relationship between pin 20 and 21 will be restored. Because of the importance of voltage equality between the charge pump reference and output pins, a resistor should never be connected in series with the operational amplifier inverting input and pin 20, as is the case with a phase detector giving voltage outputs. Any current drawn from the charge pump reference pin should be limited to the few microamps input current of a typical operational amplifier. A resistor between the charge pump reference and the non-inverting input could be added to provide isolation but the value should not be so high that more than a few millivolts drop are produced by the amplifier input current.

When selecting a suitable amplifier for the loop filter, a number of parameters are important; input offset voltage in most designs is only a few millivolts and an offset of 5mV will produce a mismatch in the up and down currents of about 4% with the charge pump multiplication factor set at 1. The mismatch in up and down currents caused by input offset voltage will be reduced in proportion to the charge pump multiplication factor in use.

If the linearity of the phase detector about the normal phase locked operating point is critical, the input offset voltage of most amplifiers can be adjusted to near zero by means of a potentiometer. The charge pump reference voltage on pin 21 is about 1·3V below the positive supply and will change with temperature and with the programmed charge pump multiplication factor. In many cases it is convenient to operate the amplifier with the negative power supply pin connected to 0V as this removes the need for an additional power supply. The amplifier selected must have a common mode range to within 3·4V (minimum charge pump reference voltage) of the negative supply pin to operate correctly without a negative supply. Most popular amplifiers can be operated from a 30V positive supply to give a wide VCO voltage drive range and have adequate common mode range to operate with inputs at +3·4V with respect to the negative supply.

Input bias and offset current levels to most operational amplifiers are unlikely to be high enough to significantly affect the accuracy of the charge pump circuit currents but the bias current can be important in reducing reference side bands and local oscillator drift during frequency changes.

When the loop is locked, the charge pump produces only very narrow pulses of sufficient width to make up for any charge lost from the loop filter components during the reference cycle. The charge lost will be due to leakage from the charge pump output pin and to the amplifier input bias current, the latter usually being more significant. The result of the lost charge is a sawtooth ripple on the VCO control line which frequency modulates the phase locked oscillator at the reference frequency and its harmonics. A similar effect will occur whenever the strobe input is taken high during a programming sequence. In this case the charge pump is disabled when the strobe input is high and any leakage current will cause the oscillator to drift off frequency. To reduce this effect, the duration of the strobe pulse should be minimised.

F_{PD} and F_{REF} Outputs

These outputs provide access to the outputs from the RF and reference dividers and are provided for monitoring purposes during product development or test, and for connection of an external phase detector if required. The output circuit is of ECL type, the circuit diagram being shown in Fig. 7g. The outputs can be enabled or disabled under software control by the address 0 control word but are best left in the disabled state when not required as the fast edge speeds on the output can increase the level of reference sidebands on the synthesised oscillator.

The emitter follower outputs have no internal pulldown resistor to save current and if the outputs are required an external pulldown resistor should be fitted. The value should be kept as high as possible to reduce supply current, about 2·2kΩ being suitable for monitoring with a high impedance oscilloscope probe or for driving an AC-coupled 50Ω load. A minimum value for the pulldown resistor is 330Ω.

When the F_{PD} and F_{REF} outputs are disabled the output level will be at the logic low level of about 3·5V so that the additional supply current due to the load resistors will be present even when the outputs are disabled.

Reference Input

The reference input circuit functions as an input amplifier or crystal oscillator. When an external reference signal is used this is simply AC-coupled to pin 28, the base of the input emitter follower. When a low phase noise synthesiser is required the reference signal is critical since any noise present here will be multiplied by the loop. To obtain the lowest possible phase noise from the SP8852E it is best to use the highest possible reference input frequency and to divide this down internally to obtain the required frequency at the phase detector. The amplitude of the reference input is also important, and a level close to the maximum will give the lowest noise.

When the use of a low reference input frequency say 4 to 10MHz is essential some advantage may be gained by using a limiting amplifier such as a CMOS gate to square up the reference input. In cases where a suitable reference signal is not available, it may be more convenient to use the input buffer as a crystal oscillator in this case the emitter follower input transistor is connected as a Colpitts oscillator with the crystal connected from the base to ground and with the feedback necessary for oscillation provided by a capacitor tap at the emitter. The arrangement is shown inset in Fig. 5.

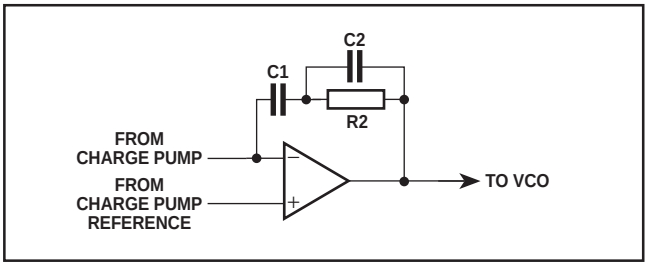


Fig. 8 Third order loop filter circuit diagram

Loop Filter Design

Generally, the third order filter configuration shown in Fig. 8 gives better results than the more commonly used second order because the reference sidebands are reduced. Three equations are required to determine values for the three constants, where

$$\tau_1 = C_1R_1$$
$$\tau_2 = R_2(C_1+C_2)$$
$$\tau_3 = C_2R_2$$

The equations are:

$$\tau_1 = \frac{K_\phi K_0}{\omega_n^2 N}\left[\frac{1+\omega_n^2\tau_2^2}{1+\omega_n^2\tau_3^2}\right]^{\frac{1}{2}} \quad \ldots(1)$$

$$\tau_2 = \frac{1}{\omega_n^2\tau_3^2} \quad \ldots(2)$$

$$\tau_3 = \frac{-\tan\Phi_0 + \frac{1}{\cos\Phi_0}}{\omega_n} \quad \ldots(3)$$

where
K_ϕ is the phase detector gain factor in mA/radian
K_0 is the VCO gain factor in radians/seconds/V
N is the division ratio from VCO to reference frequency
ω_n is the natural loop frequency
Φ_0 is the phase margin, normally set to 45°

Since the phase detector used is linear over a range of 2π radians, the phase detector gain is given by:

$$K_\phi = \frac{\text{Phase comparator current setting}}{2\pi} \text{ mA/radian}$$

These values can now be substituted in equation (1) to obtain a value for C_1 and in equations (2) and (3) to determine values for C_2 and R_2.

Example

Calculate values for a loop with the following parameters:

Frequency to be synthesised	1000MHz
Reference frequency	10MHz
Division ratio	1000MHz/100MHz = 100
K_0 VCO gain factor	2π×10MHz/V
Φ_0 phase margin	45°
Phase comparator current	6·3mA

The phase detector gain factor K_ϕ = 6·3/2π = 1mA/radian

From equation (3):

$$\tau_3 = \frac{-\tan 45° + \frac{1}{\cos 45°}}{100\text{kHz}\times 2\pi}$$
$$= \frac{0{\cdot}4142}{628319}$$
$$\therefore \tau_3 = \mathbf{659\times 10^{-9}}$$

From equation (2):

$$\tau_2 = \frac{1}{(100\text{kHz}\times 2\pi)^2\times 659\times 10^{-9}}$$
$$\therefore \tau_2 = \mathbf{3{\cdot}844\times 10^{-6}}$$

Using these values in equation (1):

$$\tau_1 = \frac{1\times 10^{-3}\times 2\pi\times 10\text{MHz/V}}{100\times(100\text{kHz}\times 2\pi)^2}\times[A]^{\frac{1}{2}}$$

$$\text{where A} = \left[\frac{1+\omega_n^2\tau_2^2}{1+\omega_n^2\tau_3^2}\right]$$
$$= \frac{1+(100\text{kHz}\times 2\pi)^2\times(3{\cdot}844\times 10^{-6})^2}{1+(100\text{kHz}\times 2\pi)^2\times(659\times 10^{-9})^2}$$
$$\tau_1 = \frac{62832}{39{\cdot}48\times 10^{-12}}\left[\frac{6{\cdot}833}{1{\cdot}1714}\right]^{\frac{1}{2}}$$
$$= 1{\cdot}59\times 10^{-9}\times 2{\cdot}415$$
$$\therefore \tau_1 = \mathbf{3{\cdot}84\times 10^{-9}}$$

Now, $\tau_1 = C_1 \therefore C_1 = \mathbf{3{\cdot}84nF}$

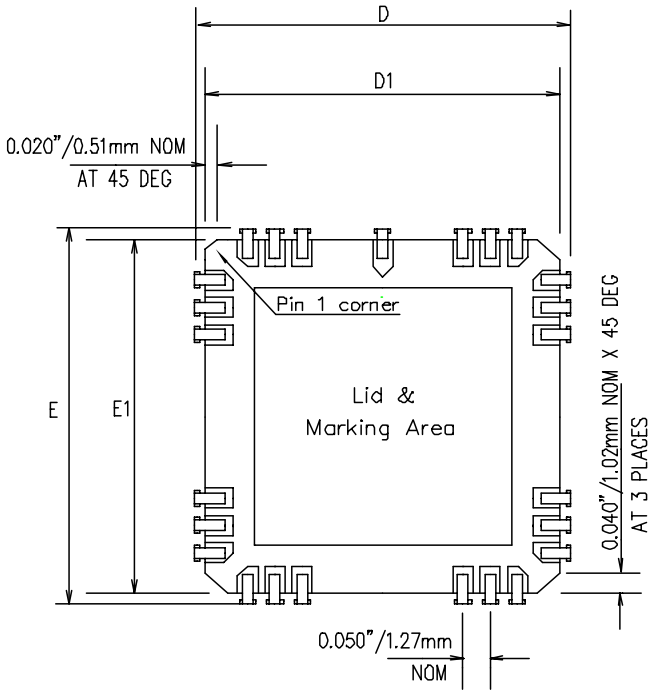
$$\tau_2 = R_2(C_1+C_2)$$
$$\tau_2 = C_2R_2$$

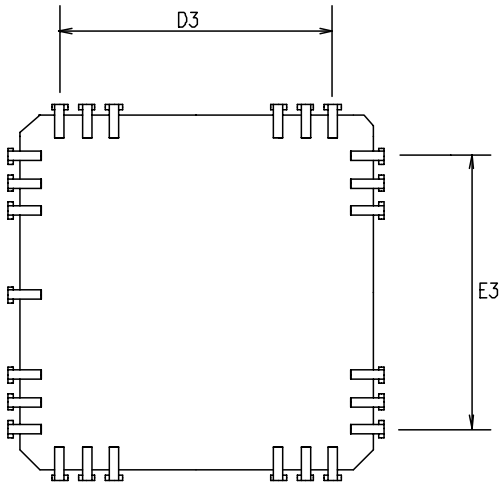
Substituting for C2:

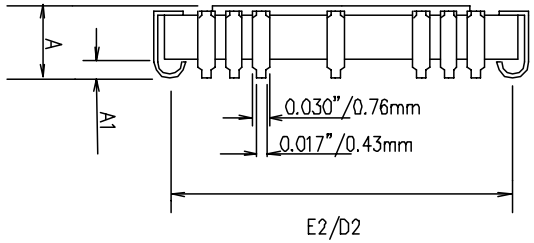
$$\tau_2 = R_2\left[C_1+\frac{\tau_3}{R_2}\right]$$

$$\text{or, } R_2 = \frac{\tau_2-\tau_3}{C_1}$$
$$= \frac{3{\cdot}844\times 10^{-6}-659\times 10^{-9}}{0{\cdot}0153\times 10^{-6}}$$
$$\therefore R_2 = \mathbf{829{\cdot}4\Omega}$$

$$\tau_3 = C_2R_2 = \frac{\tau_3}{R_2}$$
$$= \frac{659\times 10^{-9}}{829{\cdot}4}$$
$$\therefore C_2 = \mathbf{0{\cdot}794nF}$$







Symbol	Altern. Dimensions in millimetres			Control Dimensions in inches		
	MIN	Nominal	MAX	MIN	Nominal	MAX
A	3.05		3.43	0.120		0.135
A1		0.89			0.035	
D	17.27		17.78	0.680		0.700
D1	16.33		16.81	0.643		0.662
D2	15.49		16.51	0.610		0.650
D3	12.45		12.95	0.490		0.510
E	17.27		17.78	0.680		0.700
E1	16.33		16.81	0.643		0.662
E2	15.49		16.51	0.610		0.650
E3	12.45		12.95	0.490		0.510
	Pin features					
N	44					
ND	11					
NE	11					
NOTE	SQUARE					

This drawing supersedes 418/ED/51129/002(Swindon) and TD/D 862(Oldham)

ISSUE	1	2			
ACN	203113	207311			
DATE	9SEP97	19AUG99			
APPRD.					

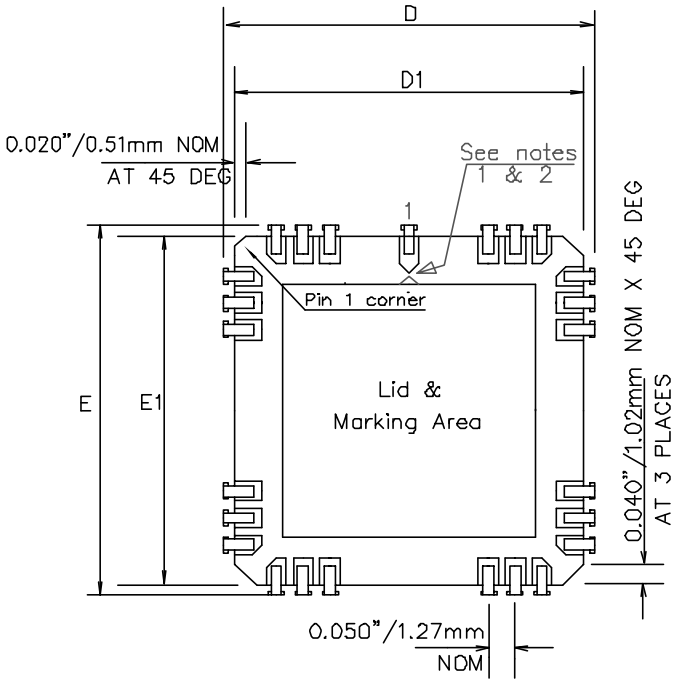
ORIGINATING SITE: SWINDON

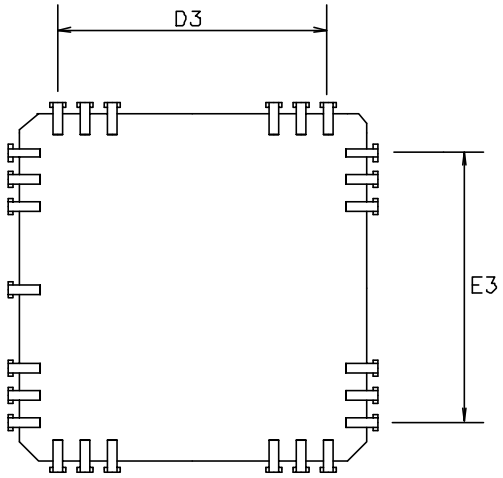
Title:

Outline Drawing for 44 'J' LDCC (HC)

Drawing Number

GPD00442





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	Pin features					
N	44					
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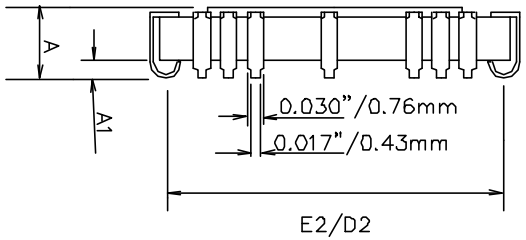
NOTE	SQUARE					



NOTES:

1. Pin 1 will always be in the postion shown relative to the 'Pin 1 Corner'.
2. Pin 1 indicator may be any shape or may not exist at all.

This drawing supersedes 418/ED/51129/002 (Swindon)

ISSUE	1	2	3	4
ACN	203113	207311	212484	213563
DATE	9Sep97	19Aug99	5Apr02	14Oct02
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

HC / J

Package Code QF

Package Outline for
44 lead J-LDCC

GPD00442

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