

# 4V Drive Nch+Pch MOSFET

## SP8M21

●Structure

Silicon N-channel MOSFET /  
Silicon P-channel MOSFET

●Features

- 1) Low on-resistance.
- 2) Built-in G-S protection diode.
- 3) Small and surface mount package (SOP8).

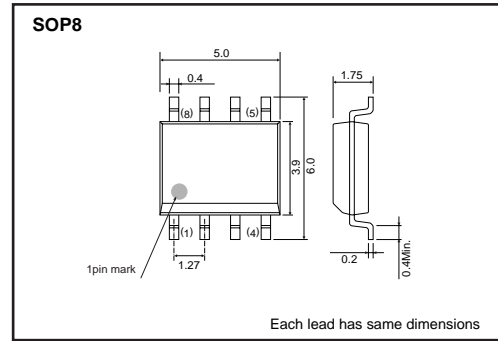
●Applications

Switching

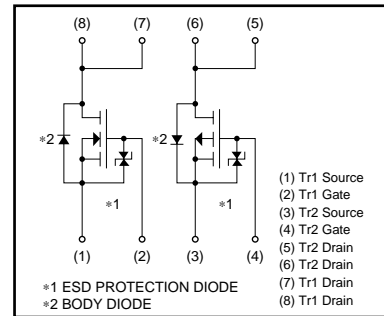
●Package specifications

Type	Package	Taping
	Code	TB
	Basic ordering unit (pieces)	2500
SP8M21		○

●Dimensions (Unit : mm)



●Inner circuit



●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits		Unit
		Tr1 : N-ch	Tr2 : P-ch	
Drain-source voltage	$V_{DSS}$	45	-45	V
Gate-source voltage	$V_{GSS}$	20	-20	V
Drain current	Continuous	$I_D$	$\pm 6.0$	A
	Pulsed	$I_{DP}^{*1}$	$\pm 24$	A
Source current (Body diode)	Continuous	$I_S$	1.0	A
	Pulsed	$I_{SP}^{*1}$	24	A
Total power dissipation	$P_D^{*2}$	2.0		W / TOTAL
		1.4		W / ELEMENT
Channel temperature	$T_{ch}$	150		°C
Storage temperature	$T_{stg}$	-55 to +150		°C

\*1  $P_w \leq 10\mu s$ , Duty cycle  $\leq 1\%$   
\*2 Mounted on a ceramic board.

## Transistors

## N-ch

## ●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I <sub>GSS</sub>	–	–	10	μA	V <sub>GS</sub> =20V, V <sub>DS</sub> =0V
Drain-source breakdown voltage	V <sub>(BR) DSS</sub>	45	–	–	V	I <sub>D</sub> = 1mA, V <sub>GS</sub> =0V
Zero gate voltage drain current	I <sub>DSS</sub>	–	–	1	μA	V <sub>DS</sub> = 45V, V <sub>GS</sub> =0V
Gate threshold voltage	V <sub>GS(th)</sub>	1.0	–	2.5	V	V <sub>DS</sub> = 10V, I <sub>D</sub> = 1mA
Static drain-source on-state resistance	R <sub>DS(on)</sub> *	–	18	25	mΩ	I <sub>D</sub> = 6.0A, V <sub>GS</sub> = 10V
		–	24	34	mΩ	I <sub>D</sub> = 6.0A, V <sub>GS</sub> = 4.5V
		–	26	37	mΩ	I <sub>D</sub> = 6.0A, V <sub>GS</sub> = 4.0V
Forward transfer admittance	Y <sub>fs</sub>  *	6.0	–	–	S	V <sub>DS</sub> = 10V, I <sub>D</sub> = 6.0A
Input capacitance	C <sub>iss</sub>	–	1400	–	pF	V <sub>DS</sub> = 10V
Output capacitance	C <sub>oss</sub>	–	310	–	pF	V <sub>GS</sub> =0V
Reverse transfer capacitance	C <sub>rss</sub>	–	175	–	pF	f=1MHz
Turn-on delay time	t <sub>d(on)</sub> *	–	19	–	ns	V <sub>DD</sub> ≐ 25V
Rise time	t <sub>r</sub> *	–	30	–	ns	I <sub>D</sub> = 3.0A
Turn-off delay time	t <sub>d(off)</sub> *	–	72	–	ns	V <sub>GS</sub> = 10V
Fall time	t <sub>f</sub> *	–	27	–	ns	R <sub>L</sub> = 8Ω
Total gate charge	Q <sub>g</sub> *	–	15.4	21.6	nC	R <sub>G</sub> =10Ω
Gate-source charge	Q <sub>gs</sub> *	–	3.7	–	nC	V <sub>DD</sub> ≐ 25V, V <sub>GS</sub> = 5V
Gate-drain charge	Q <sub>gd</sub> *	–	6.5	–	nC	I <sub>D</sub> = 6.0A
						R <sub>L</sub> = 4Ω, R <sub>G</sub> = 10Ω

\*Pulsed

## ●Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V <sub>SD</sub> *	–	–	1.2	V	I <sub>S</sub> = 6.0A, V <sub>GS</sub> =0V

\*Pulsed

## Transistors

## P-ch

## ●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I <sub>GSS</sub>	–	–	–10	μA	V <sub>GS</sub> = –20V, V <sub>DS</sub> =0V
Drain-source breakdown voltage	V <sub>(BR) DSS</sub>	–45	–	–	V	I <sub>D</sub> = –1mA, V <sub>GS</sub> =0V
Zero gate voltage drain current	I <sub>DSS</sub>	–	–	–1	μA	V <sub>DS</sub> = –45V, V <sub>GS</sub> =0V
Gate threshold voltage	V <sub>GS(th)</sub>	–1.0	–	–2.5	V	V <sub>DS</sub> = –10V, I <sub>D</sub> = –1mA
Static drain-source on-state resistance	R <sub>DS(on)</sub> *	–	33	46	mΩ	I <sub>D</sub> = –4.0A, V <sub>GS</sub> = –10V
		–	43	60	mΩ	I <sub>D</sub> = –4.0A, V <sub>GS</sub> = –4.5V
		–	47	65	mΩ	I <sub>D</sub> = –4.0A, V <sub>GS</sub> = –4.0V
Forward transfer admittance	Y <sub>fs</sub>  *	6.0	–	–	S	V <sub>DS</sub> = –10V, I <sub>D</sub> = –4.0A
Input capacitance	C <sub>iss</sub>	–	2400	–	pF	V <sub>DS</sub> = –10V
Output capacitance	C <sub>oss</sub>	–	320	–	pF	V <sub>GS</sub> = 0V
Reverse transfer capacitance	C <sub>rss</sub>	–	200	–	pF	f=1MHz
Turn-on delay time	t <sub>d(on)</sub> *	–	23	–	ns	V <sub>DD</sub> ≐ –25V
Rise time	t <sub>r</sub> *	–	23	–	ns	I <sub>D</sub> = –2.0A
Turn-off delay time	t <sub>d(off)</sub> *	–	90	–	ns	V <sub>GS</sub> = –10V
Fall time	t <sub>f</sub> *	–	22	–	ns	R <sub>L</sub> = 12.5Ω
Total gate charge	Q <sub>g</sub> *	–	20.0	28.0	nC	R <sub>G</sub> = 10Ω
Gate-source charge	Q <sub>gs</sub> *	–	6.5	–	nC	V <sub>DD</sub> ≐ –25V, V <sub>GS</sub> = –5V
Gate-drain charge	Q <sub>gd</sub> *	–	7.5	–	nC	I <sub>D</sub> = –4.0A
						R <sub>L</sub> = 6Ω, R <sub>G</sub> = 10Ω

\*Pulsed

## ●Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V <sub>SD</sub> *	–	–	–1.2	V	I <sub>S</sub> = –4.0A, V <sub>GS</sub> =0V

\*Pulsed

Transistors

N-ch

●Electrical characteristic curves

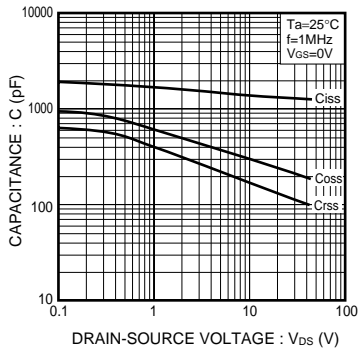


Fig.1 Typical Capacitance vs. Drain-Source Voltage

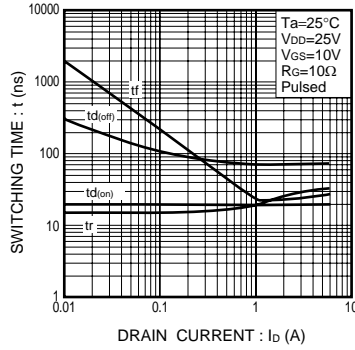


Fig.2 Switching Characteristics

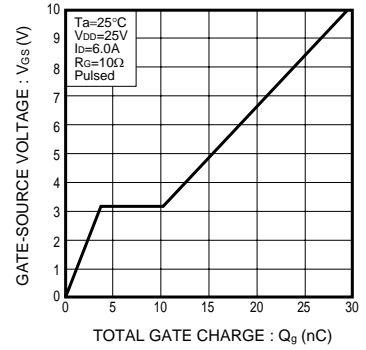


Fig.3 Dynamic Input Characteristics

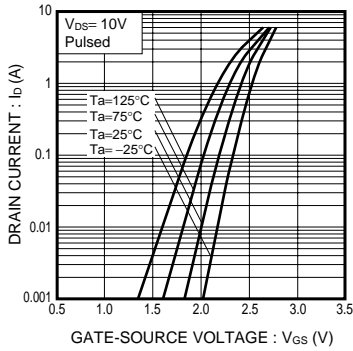


Fig.4 Typical Transfer Characteristics

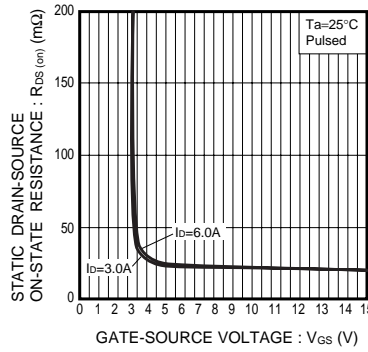


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

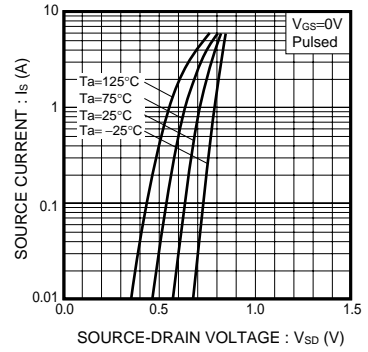


Fig.6 Source Current vs. Source-Drain Voltage

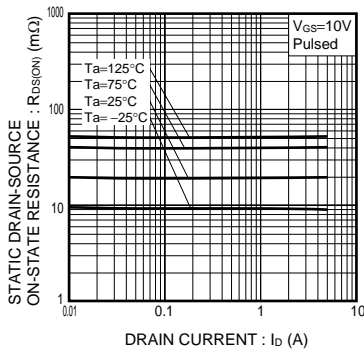


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current ( I )

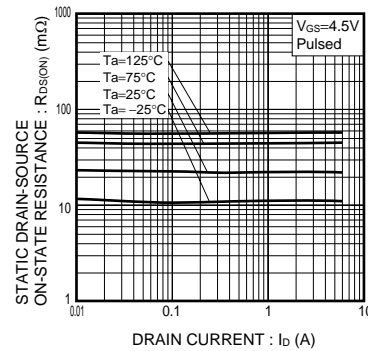


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current ( II )

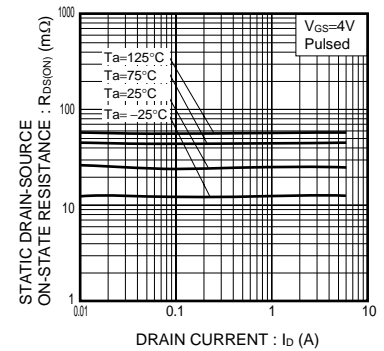


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current ( III )

Transistors

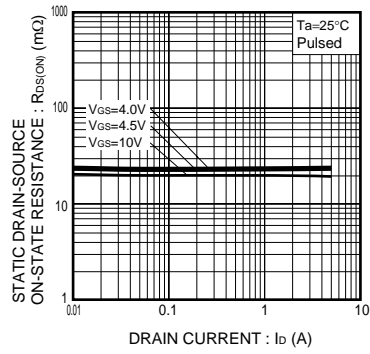


Fig.10 Static Drain-Source On-State Resistance vs. Drain Current (IV)

Transistors

P-ch

●Electrical characteristic curves

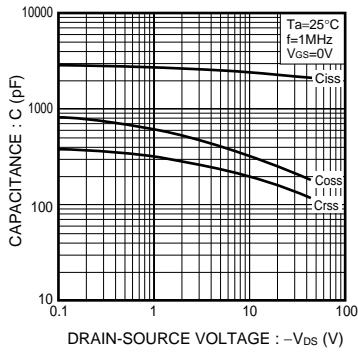


Fig.1 Typical Capacitance vs. Drain-Source Voltage

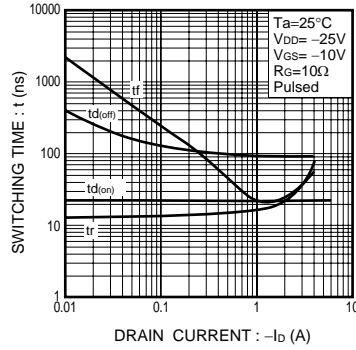


Fig.2 Switching Characteristics

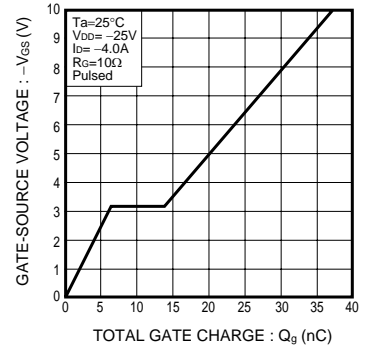


Fig.3 Dynamic Input Characteristics

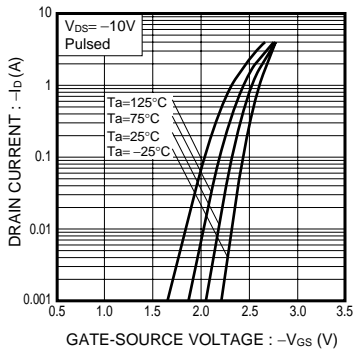


Fig.4 Typical Transfer Characteristics

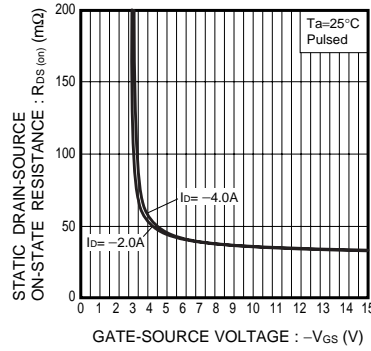


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

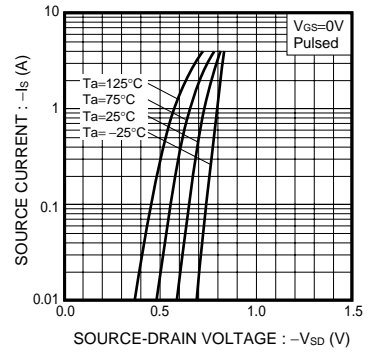


Fig.6 Source Current vs. Source-Drain Voltage

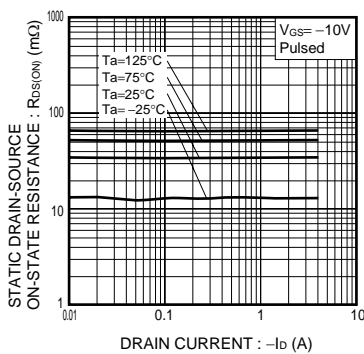


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current ( I )

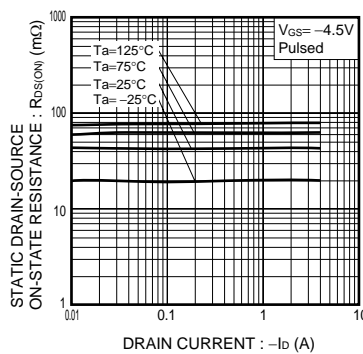


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current ( II )

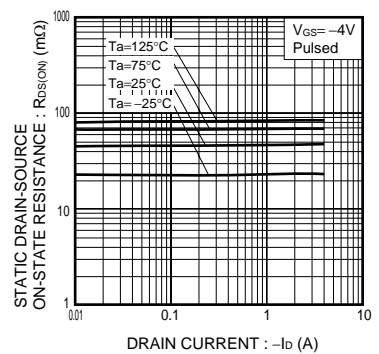


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current ( III )

Transistors

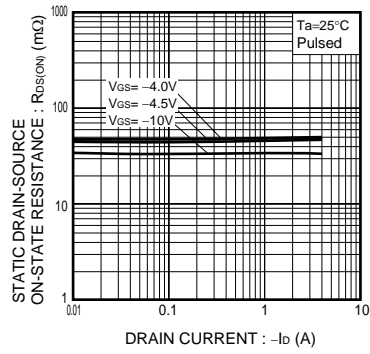


Fig.10 Static Drain-Source On-State Resistance vs. Drain Current (IV)

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