SP9210

128-RGB x 160 Color OLED Column / Row Driver

with Controller

REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
V1.0	Initial Release	20010-06	

CONTENT

1 GENERAL DESCRIPTION

The SP9210 is a low power single chip OLED Display Driver IC with integrated controller in 65K colors. The SP9210's well matched current drivers and user provisions to accommodate specific display panel characteristics ensure uniform luminance and high quality operation

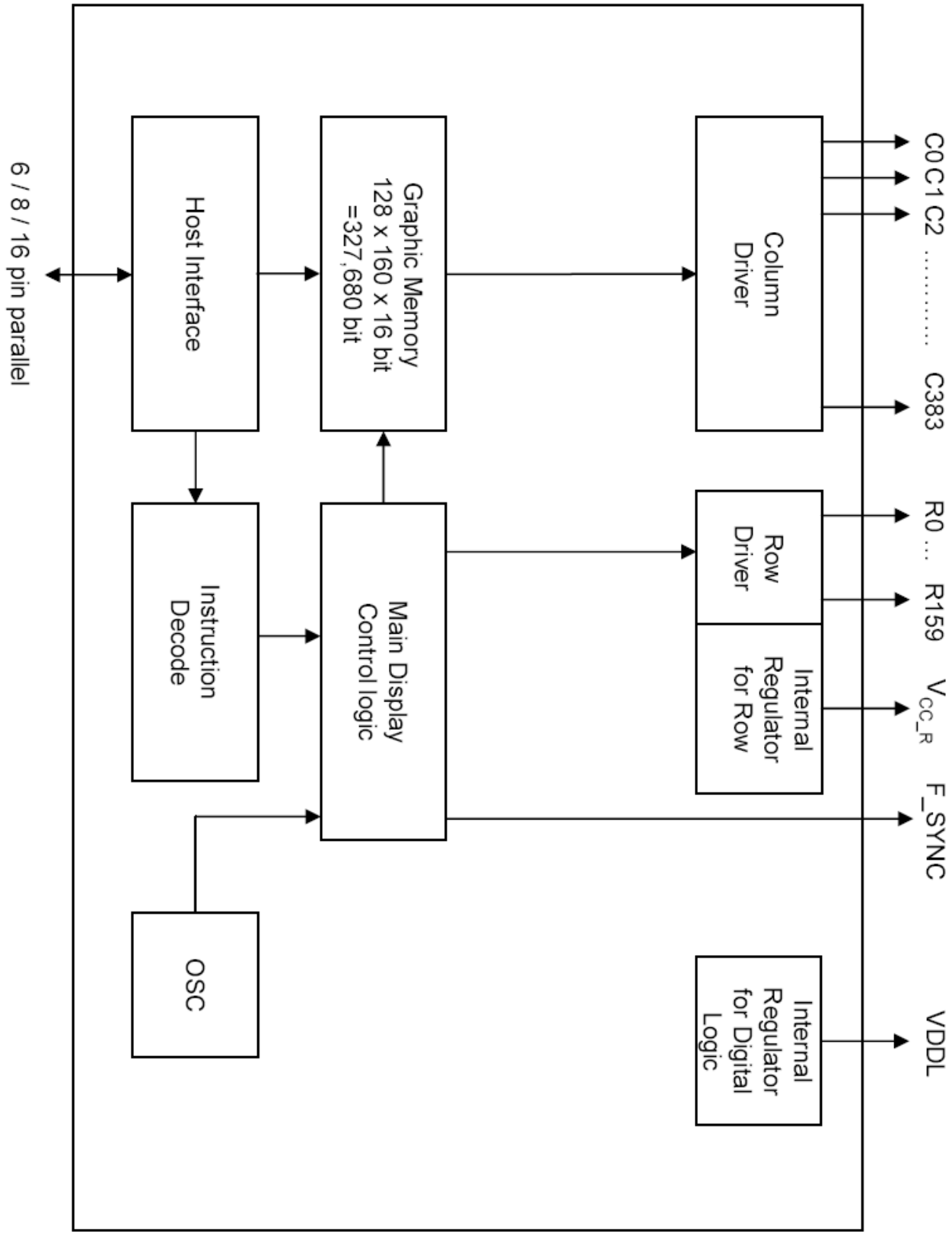
The SP9210 has the maximum resolution of 128[RGB] * 160. The SP9210 is a high-performance device which includes 327K bit graphic RAM[= 128 * 160 * 16 bit], on-chip oscillator and programmable frame frequency adjustment. It has various screen saver functions to extend a panel's life time also.

The SP9210 displays data directly for its internal graphic RAM. Data/Command are sent from general MPU. The SP9210 supports 6 / 8 / 16 bit in parallel interface with 8080 or 6800 series industry standard MPU, serial interface.

2 FEATURES

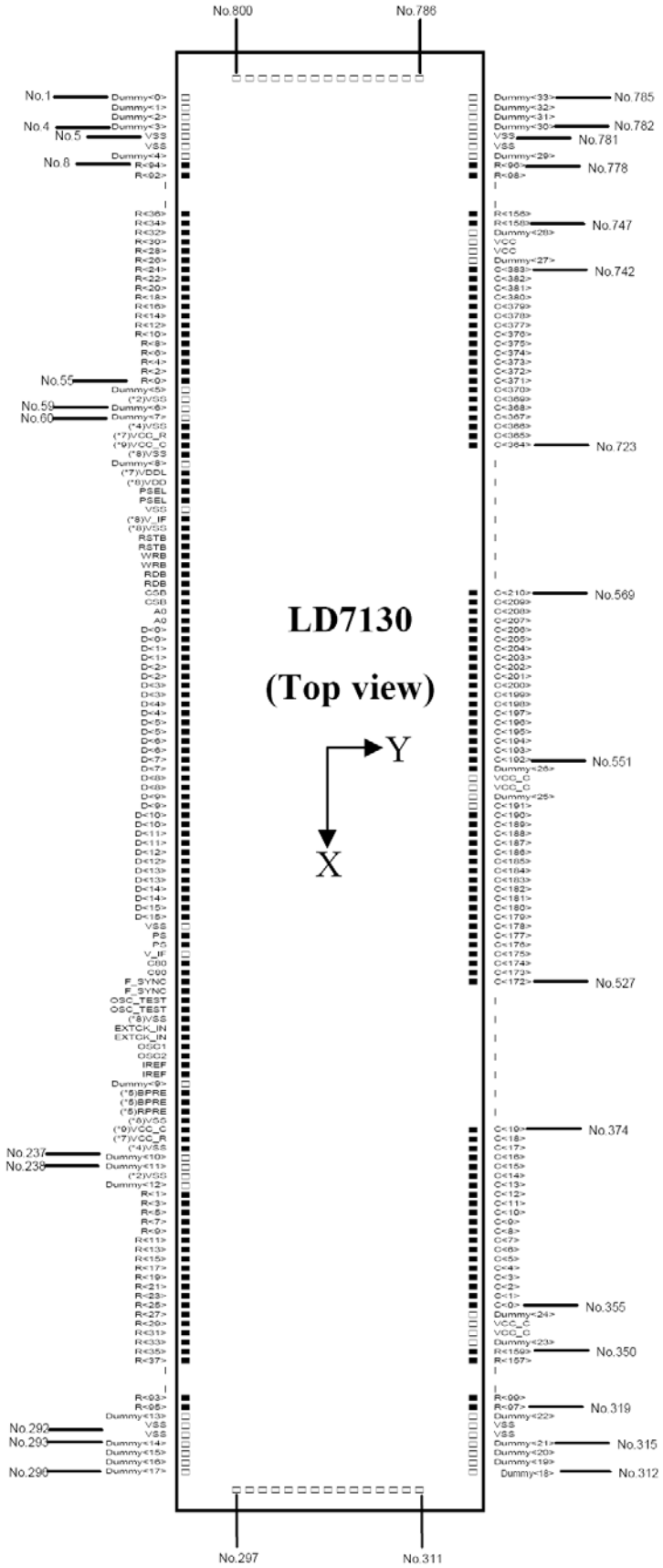
- **128-RGB x 160 65K Color OLED Display Driver IC**
  - Max. resolution of 128 RGB x160
  - Embedded 327K bit of graphic RAM
  - On-chip oscillator
  - Advanced display features
- **For Dot Matrix Display**
  - Column max. source current: 255uA with 1uA step.
  - Row max. sink average current: 50mA
  - Row R_{ON} resistance : 20Ω
- **On-chip Oscillators**
  - Internal RC Oscillation
- **Graphic RAM**
  - 128x160x16bit = 327Kbit
- **Operating Voltage**
  - V_{DD} : 2.4 ~ 3.3V
  - V_{IF} : 1.65 ~ 3.3V for MPU Interface
  - V_{CC_C} : 8.0 ~ 18.0V for Column
  - V_{CC_R} : 8.0 ~ 18.0V for Row
- **Operating Temperature**
  - Wide range of operating temp.: -40 to 85℃
- **Industry Standard Host Bus I/F**
  - 6/8/16 bit I/F :
    8080-series MPU, 6800-series MPU
  - Serial I/F
- **Advanced display features**
  - Adjustable frame frequency.
  - Internal regulator for row.

3 FUNCTIONAL BLOCK DIAGRAM



4 CHIP GENERAL INFORMATION

4.1 Die Pad Floor Plan



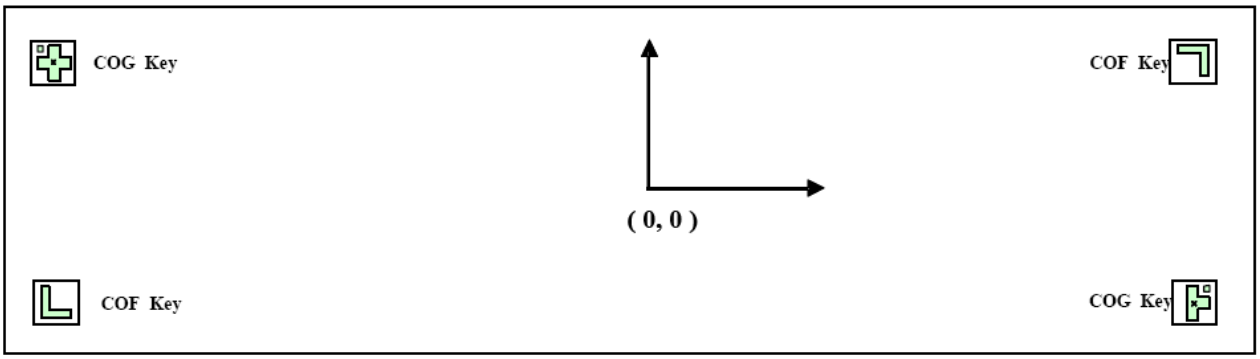
4.2 Chip Spec

Item	SPEC.
Chip Size	14546um * 1072um
Chip Thickness	425 um
Min. Column Pad Pitch	30 um
Min. Row Pad Pitch	30 um
Min. I/O Pad Pitch	60 um
Bump Height	15 um ± 3 um

4.3 Bump Size

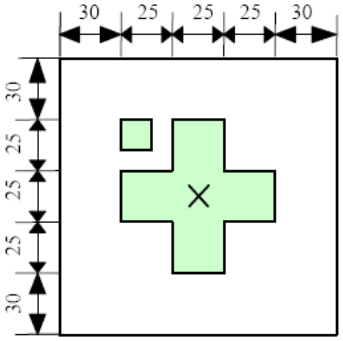
Pad No.	Bump Size
60~237	40um X 91um
5~59, 238~292, 316~781	18um X 108um
1~4, 293~296, 312~315, 782~785	28um X 108um
297~299, 309~311, 786~788, 798~800	96um X 33um
300~308, 789~797	96um X 28um

4.4 Align Key Coordination

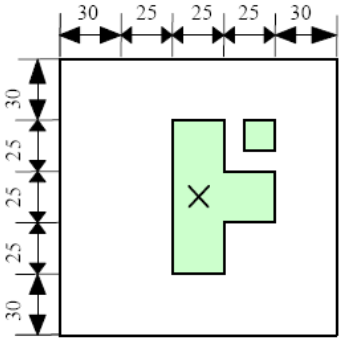


COG Align Key Coordination

(Unit : um)



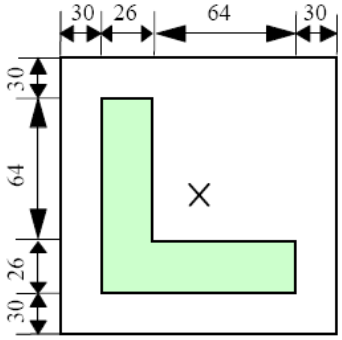
Upper Left (-6999.5, 250.5)



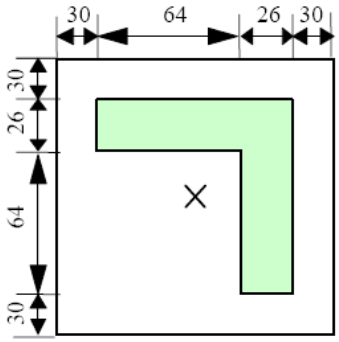
Lower Right (6999.5, -250.5)

COF Align Key Coordination

(Unit : um)



Lower Left (-6992.0, -243.0)



Upper Left (6992, 243.0)

5 PIN DESCRIPTION

Pin Name	Pin Type	Descriptions
V_{DD}	P	This pin is a power supply pin of logic block. It must be connected to the external power source.
V_{DDL}	I/O	This pin is the power output pin of internal logic power regulator. A capacitor is connected between it and GND. If internal logic power regulator is disabled, It must be connected to the external power source.
V_{IF}	P	This pin is a power supply pin of I/O buffer block. It must be connected to the external power source.
GND	P	These pins are Analog/digital block ground pin and also act as ground reference for the logic pins. These pins must be connected to external ground.
PRE R/G/B	I/O	These pins are Pre-Charge supply voltage for Red/Green/Blue.
I_{REF} (Optional)	O	This pin is needed at external resister mode only. This pin is the dot output current reference pin. I_{DOT} is derived from Iref. A resister should be connected between this pin and ground . (Current Setting. Typ Resistance = 39 kΩ) (Current adjustable range ±30%)
C80	I	This pin select MPU type in parallel interface. When this pin is high, it must be 6800-series MPU. When this pin is low, it must be 8080-series MPU.
PS	I	This pin select interface mode. When this pin is high, it must be parallel interface mode. When this pin is low, it must be serial Interface mode.
V_{CC_C}	P	Dot Matrix Power Supply for Column Driver. It is supplied by external high voltage source.
V_{CC_R}	P	This pin is the power output pin of internal row power regulator. A 4.7uF capacitor is recommended to connect between V_{CC_R} and GND. If internal row power regulator is disabled, It must be connected to the external high voltage source.
R[0:159]	O	These pins provide the row switch signals to the OLED panel.
C[0:383]	O	These pins provide the OLED column driving signals.

Pin Name	Pin Type	Descriptions
PSEL	I	This pin enable/disable internal logic power regulator. When this pin is tied with V_{DD} pin, it is the internal logic power regulator enabled.
CSB	I	This pin is the Chip Select input. The chip is enabled only when it is pulled low. (Active Low)
RDB/E	I	When interfacing to a 6800-series MPU, this pin will act as the Enable (E) signal. When connecting to an 8080 MPU, this pin will used as RDB signal.
WRB/RW	I	When interfacing to a 6800-series MPU, this pin will act as the Read/Write (RW) selection signal. Read mode will be carried out when it is pulled high and write mode will be carried out when it is low. When connecting to an 8080 MPU, this pin will used as Write (WDB) signal. Data write operation is initialed when it is pulled low.
RSTB	I	This pin is reset signal input. When it is low, initialization of chip is executed. Keep this pin high during normal operation.
A0	I	This pin is a address pin. When it is pulled low, the input data is treated as command signal, When it is pulled high, the input data is treated as parameter input.
D[15:0]	I/O	These pins are 16-bit bi-directional data bus to be connected to the MPU's data bus. In case of serial I/F, D[1] is serial data and D[0] is serial clock input.
F_SYNC	O	Frame Sync Signal
TEST_1	I	This pin is test signal input. See application guide 10.8. (page 29) This pin should be connected ground in application.

※NOTE :

I : Input

O : Output

I/O : Bi-directional (Input/Output)

P : Power

6 FUNCTIONAL BLOCK DESCRIPTION

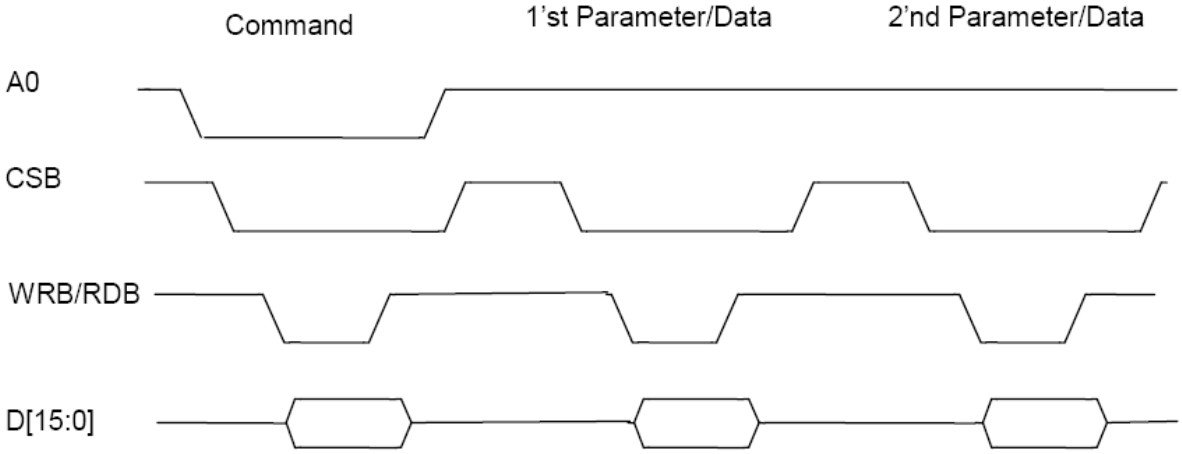
6.1 MPU Interface Selection

MPU Interface mode is determined by C80 and PS pin. When PS pin is high, it means parallel interface mode. When PS pin is low, it means serial interface mode.
When C80 pin is high, it means to use 6800-series MPU interface and when C80 pin is low, it means to use 8080-series MPU interface. Please refer the page 28 and 29 for Application guide.
To change bus type being used “Interface Bus Select(08h)” command, please refer to the Appendix A.

6.1.1 Parallel Interface for 8080-Series MPU

The parallel interface consist of CSB, WRB, RDB, A0 and 16 bi-directional data pins Data[15:0]. A low in A0 pin indicate COMMAND read/write and high in A0 pin indicates Parameter or Data. A rising edge of RDB input serves as a data READ latch signal while CSB is kept low. A rising edge of WRB input serves as a data/command WRITE latch signal while CSB is kept low.

Function	CSB	WRB	RDB	A0	D[15:0]
Write Command	L	↑	H	L	Command
Write Parameter/Data	L	↑	H	H	Parameter or Data
Read Parameter/Data	L	H	↑	H	Parameter or Data



※NOTE :

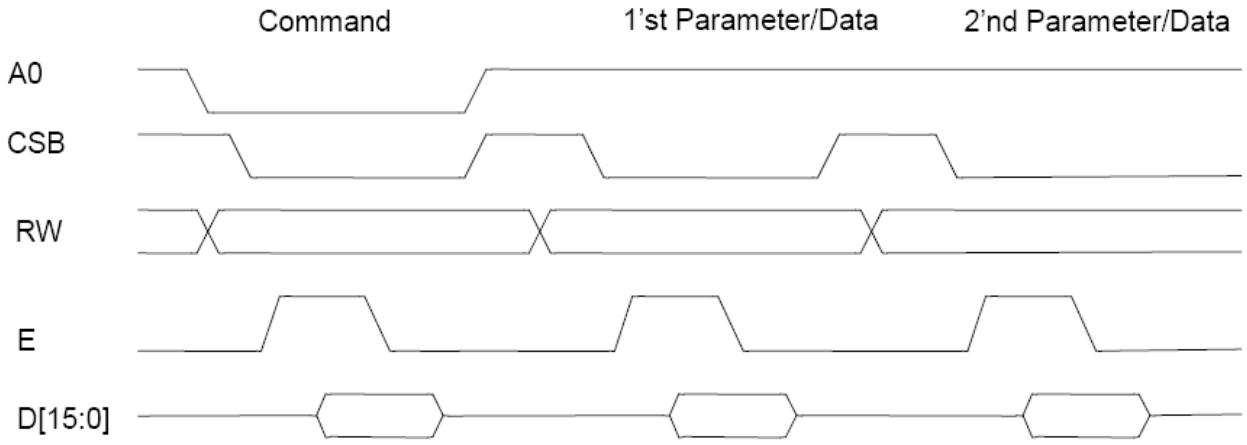
↑ stands for rising edge of signal.

L stands for low in signal.

H stands for high in signal.

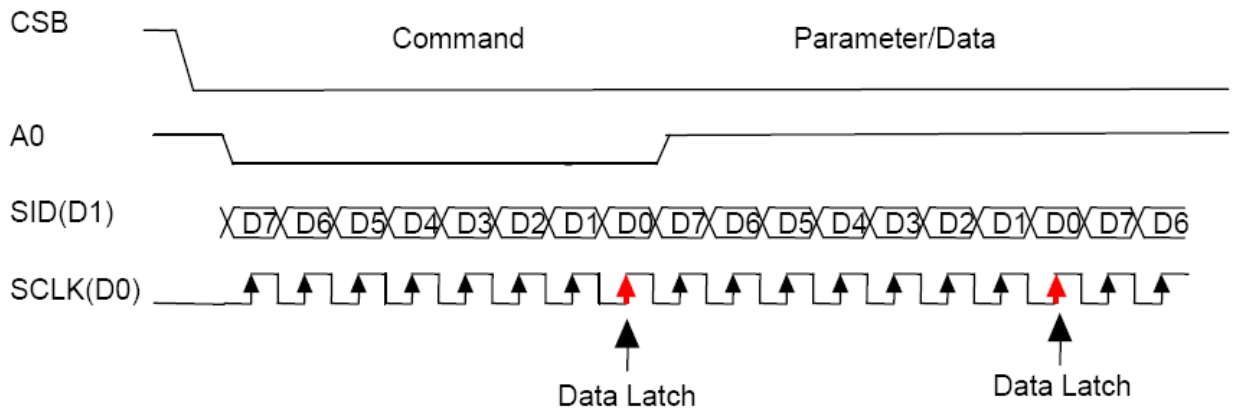
6.1.2 Parallel Interface for 6080-Series MPU

Function	CSB	RW	E	A0	D[15:0]
Write Command	L	L	↓	L	Command
Write Parameter/Data	L	L	↓	H	Parameter or Data
Read Parameter/Data	L	H	↓	H	Parameter or Data



6.1.3 MPU Serial Interface

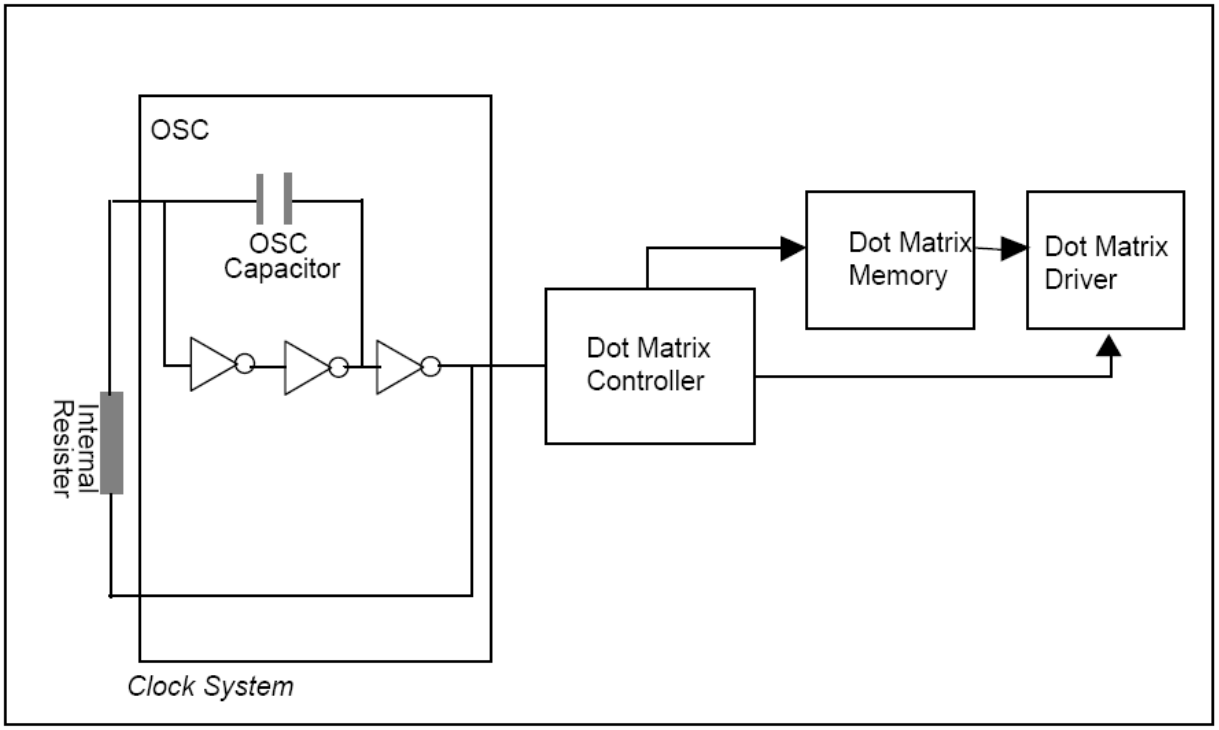
Function	CSB	CLOCK	A0	DATA
Write Command	L	D[0]	L	D[1]
Write Parameter/Data	L	D[0]	H	D[1]



※ Notice
- All command inputs have a priority over previous commands.
- To select Parallel/Serial Interface use PS Input. (H: Parallel L: Serial)
- Serial clock (SCLK) works in the unit of 8 clocks.
- In serial interface, 6 bit or 8 bit bus mode can be selected. (16bit bus mode not allowed)

6.2 Oscillator Circuit

This module consists of On-chip low power RC oscillator circuit for Dot Matrix.
The oscillator is stopped in stand-by mode.
The frame frequency can be changed by command of DFRAME(04h). If the frame frequency is set too low, flickering may occur. On the other hand, higher frame frequency leads to higher power consumption an the whole system.



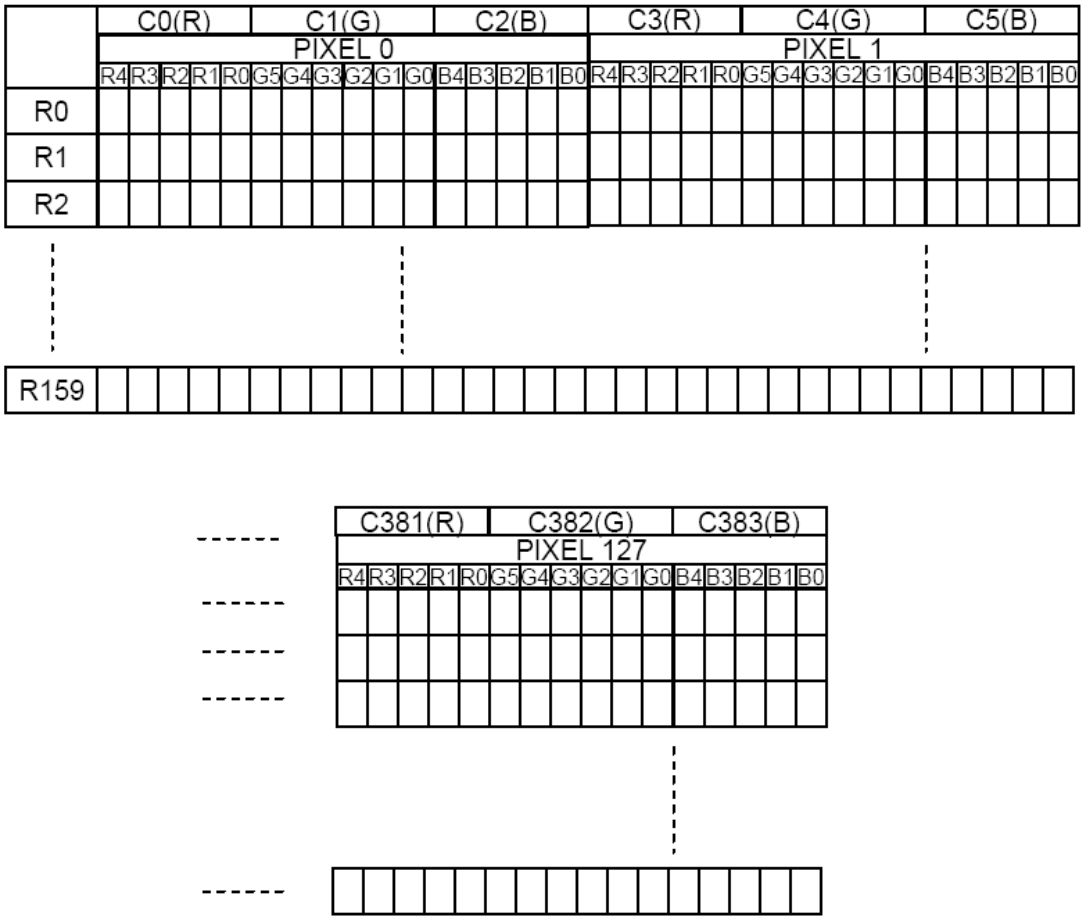
6.3 Reset Circuit

When RSTB input is low, the chip is initialized with following status;

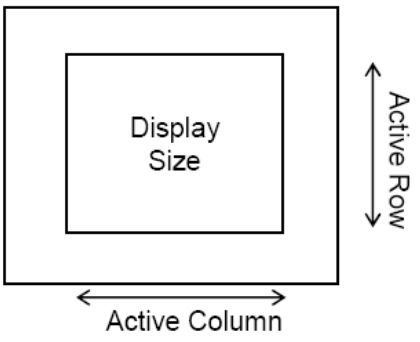
1. Dot matrix display is OFF
2. The OSC is stopped.
3. 128 RGB x 160 Display mode.
4. All registers are set with default value.

6.4 Graphic RAM(GRAM)

The GRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the GRAM is 327,680bits(=128x160x16bits).



6.4.1 Setting The Display Size



※ NOTE :

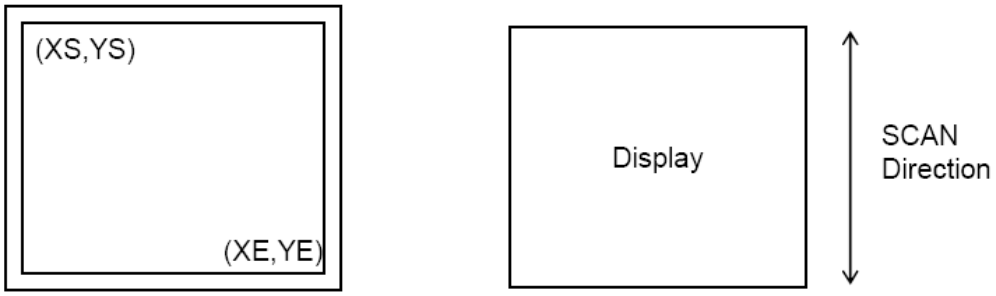
- It is set by "DispSize" command.
- The unselected column outputs are always **Pre-C.**
- The unselected row outputs are always **Vcc**.
- The row is repeated within selected area.
- Frame frequency is set for maximum display area.

6.4.2 Correspondence Bitween Memory and Display

In case of Memory Data Write,

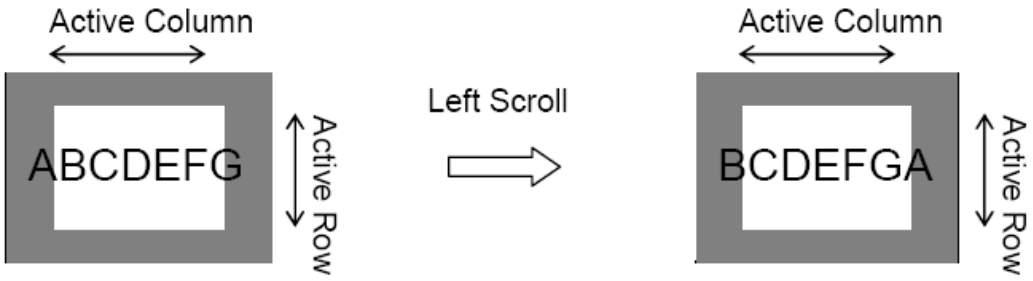
- "Data Writing Box" command indicates memory writing area.
- "Writing direction" command indicates writing direction (auto increment or decrement)

Incase of Display Direction, it is set by DispDirection command. Please refer to the Appendix



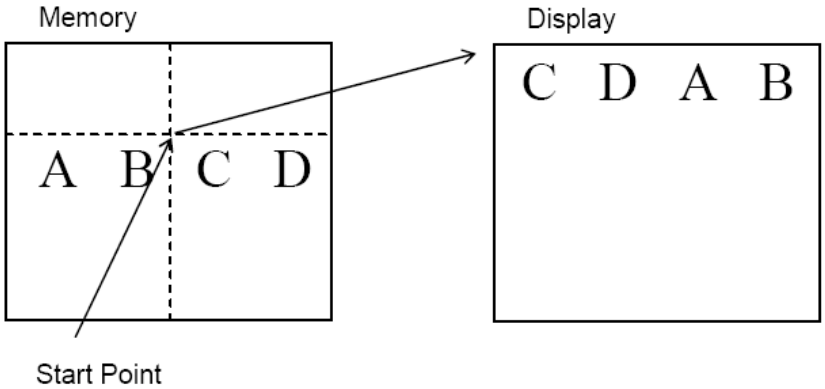
6.4.3 Setting the Scroll Area

Regardless setting display size, whole memory is enable in scroll mode,

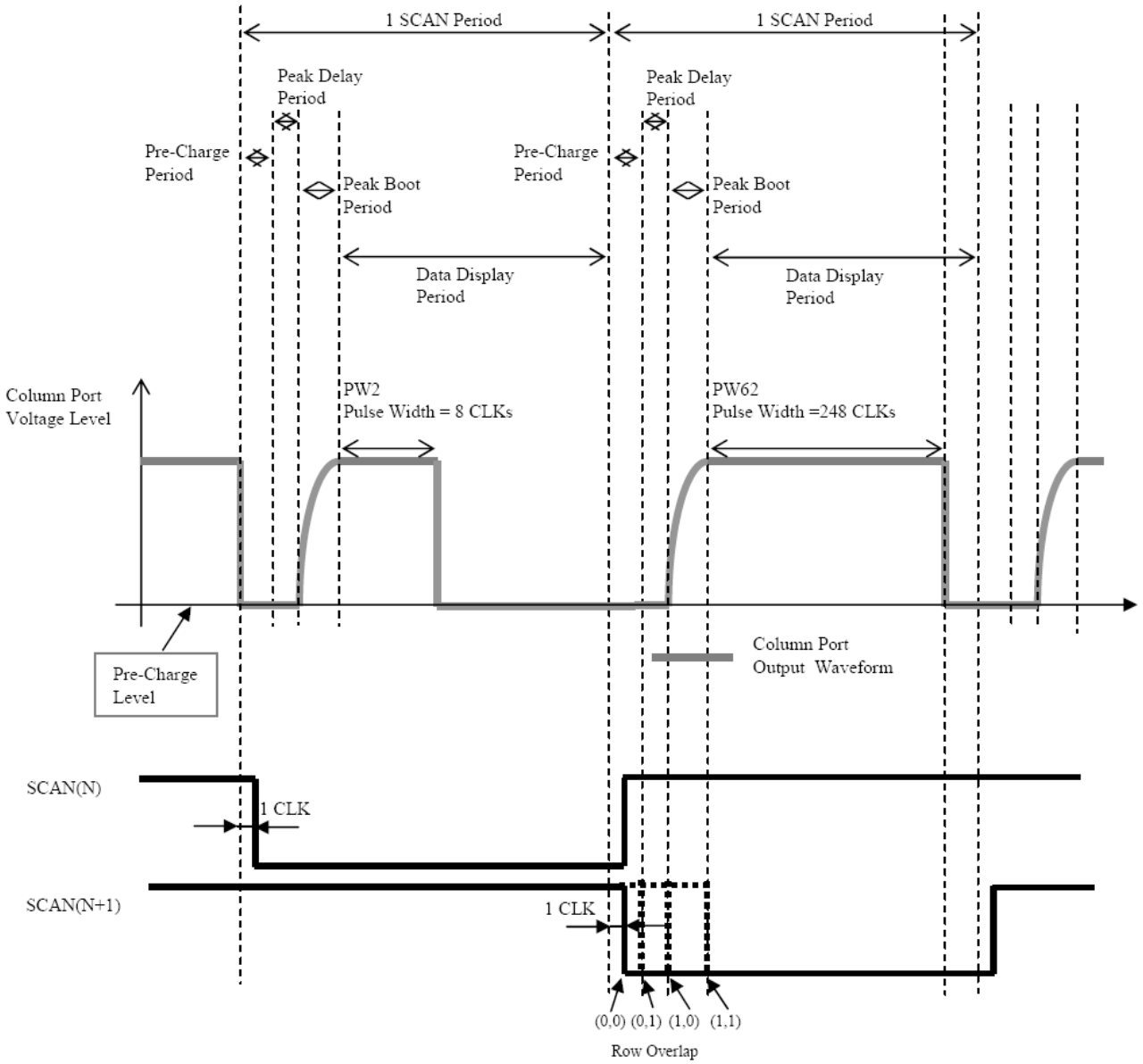


6.4.4 Setting the Memory Reading Start Address

It is set by "DispStart" command and related to the display coordination.



6.5 Column/Scan Driver Output Waveform



Related Command

1. PreC_Width(RGB)
2. PeakDelay
3. PeakWidth(RGB)
4. Dot Data Current(RGB)
5. Dot Peak Current(RGB)
6. Row Overlap

Gray Scale (Pulse Width)	Unit (DCLK)
PW0	0
PW1	4
PW2	8
⋮	⋮
PW62	248
PW63	255

Gamma Correction Table (G)

6.6 Dot Matrix Power Save

FUNCTION	DISPLY OFF	STAND BY ON	SOFT RESET
COMMAND	DISPON/OFF(02h)	STBON/OFF(03h)	SOFTRES(01h)
Description	▪All dot display turn Off.	▪All dot display turn Off. ▪OSC oscillator is stopped	▪ All display turn Off. ▪ All registers are cleared except status/data register. ▪ Stand by mode is ON ▪ OSC oscillator is stopped.

7 MAXIMUM RATINGS

Voltage Referenced to Vss

Content	Parameter	Value	Unit
V_{DD}	Supply Voltage	−0.3～+4.0	V
V_{IF}		−0.3～+4.0	
V_{CC_C}		−0.3～+20.0	
V_{CC_R}		−0.3～+20.0	
V_{IN}	Input Voltage	Vss−0.3～V_{IF}+0.3	
V_{OUT}	Output Voltage	Vss−0.3～V_{IF}+0.3	
T_{OPR}	Operating Temperature	−40.0～+85.0	℃
T_{STG}	Storage temperature	−50.0～+125.0	℃

Maximum ratings are those value beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

8 DC CHARACTERISTICS

CONDITIONS :

Voltage referenced to Vss

V_{DD}= 2.8V, V_{IF}= 2.8V, V_{CC_C}=V_{CC_R}=15V, Ta = 25℃

Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	UNIT
V_{CC_C}	Operating Voltage	-	V_{CC_C}	8.0 *1)	-	18.0	V
V_{CC_R}	Operating Voltage	-	V_{CC_R}	8.0 *1)	-	18.0	V
V_{DD} *9)	Internal Power1	-	V_{DD}	2.4	2.8	3.3	V
V_{IF}	Interface Power	-	V_{IF}	1.65		3.3	V
V_{IH}	High Logic Input Level		Logical Input	0.8*V_{IF}	—	V_{IF}	V
V_{IL}	Low Logic Input Level		Logical Input	0	—	0.2*V_{IF}	V
V_{OH}	High Logic Output Level	Iout=-100uA	Logical Output	0.9*V_{IF}	—	V_{IF}	V
V_{OL}	Low Logic Output Level	Iout=100uA	Logical Output	0	—	0.1*V_{IF}	V
IIL / IIH	Input Leakage Current			—1.0		+1.0	μA
IRVDD	VDDL Power Regulator Output Voltage (Normal Mode)	I_{VDDL}=0.5mA	VDDL	1.55	—	1.65	V
IRVCC	VCC_R Power Regulator Output Voltage	*10) Default I_{VCC_R}=10mA	V_{CC_R}	12.5	13.6	14.7	V
Cptp1	Output Current Pin to Pin Evenness *2)	Iout =100uA	C[0-383]	-2.0	-	+2.0	%
		Iout=50uA	C[0-383]	-2.0	-	+2.0	%
Carea1	Output Current Evenness *3)	Iout =100uA	C[0-383]	-	-	4.5	-
		Iout=50uA	C[0-383]	-	-	2.5	-
Cchip1	Output Current Absolute Correctness *4)	Iout =100uA	C[0:383]	-6.0	-	+6.0	%
		Iout =50uA	C[0:383]	-6.0	-	+6.0	%
Cptp3	Peak boot Pin to Pin Evenness *5)	Ioutpeak=480uA	C[0:383]	—2.0	—	+2.0	%
Calp3	Peak boot Evenness *6)	Ioutpeak=480uA	C[0:383]	—4.0	—	+4.0	%
Cchip3	Peak boot Absolute Correctness *7)	Ioutpeak=480uA	C[0:383]	—6.0	—	+6.0	%
Rrg	ROW - Vss ON Resistance	IOL=50mA	R[0:159]	-	20	40	Ω
Rr	ROW - VH ON Resistance	IOL=1mA	R[0:159]	-	1	3	kΩ

Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	UNIT
Rp	Pre-Charge SW ON Resistance	Each Pin	C[0:383]	—	600	1000	Ω
		Column All Pin Short	C[0:383]	—	—	7	Ω
I_{VIF1}	Stand-by Current		V_{IF}	—	—	5	μA
I_{VDD1}			V_{DD}	—	—	30	μA
I_{VCC_R1}			V_{CC_R}	—	—	5	μA
I_{VCC_C1}			V_{CC_C}	—	—	5	μA
I_{VIF2}	Normal Operation	*8)	V_{IF}	—	—	0.5	mA
I_{VDD2}		*8)	V_{DD}	—	—	1	mA
I_{VCC_R2}		*8)	V_{CC_R}		—	1.0	mA
I_{VCC_C2}		*8)	V_{CC_C}		—	2.0	mA

※NOTE :

*1) Min Vcc : 8V on spec but workable to 5V

*2) In case of Column output

Rm=C3n, Gm=C3n+1, Bm=C3n+2 (n=0 ~ 127)

$$Pn=Rm+Gm+Bm/3=(C3n+C3n+1+C3n+2)/3=\sum_{\ell=0}^{\ell=2} C_{3n+\ell}/3 \quad (n=0 \sim 127)$$

$$Gk\ (Group\ Avg)=\sum_{\ell=0}^{\ell=7} P_{k+\ell}/8 \quad (k=0 \sim 120)$$

P2P : (Pn − Pn+1) / Iavg (n = 0 to 127) Iavg = ∑Pn / 128 (n = 0 to 127)

*3) $Areak=\sum_{\ell=0}^{\ell=7} | P_{k+\ell}-G_k |\ (k=0 \sim 120)$ If $Area_k \leq 4.5$ then Pass

*4) C2C : (Iavg − IREF(SPEC)) / IREF(SPEC)

*5) In case of Column output

(Ik − Ik+3) / Iavg : (k = 0 to 380) & Iavg = Σ(I3k ,I3k+1 ,I3k+2) / 128 : (k = 0 to 127)

*6) (Imax − Iavg) / Iavg , (Imin − Iavg) / Iavg IAVG = Σ(Ik)/384 : (k = 0 to 383)

*7) (IAVG − IREF(SPEC)) / IREF(SPEC)

*8) Idata_period(Column_port) =10μA, Ipeak_period(Column_port) =50μA

All Data on, Frame Frequency 90Hz,

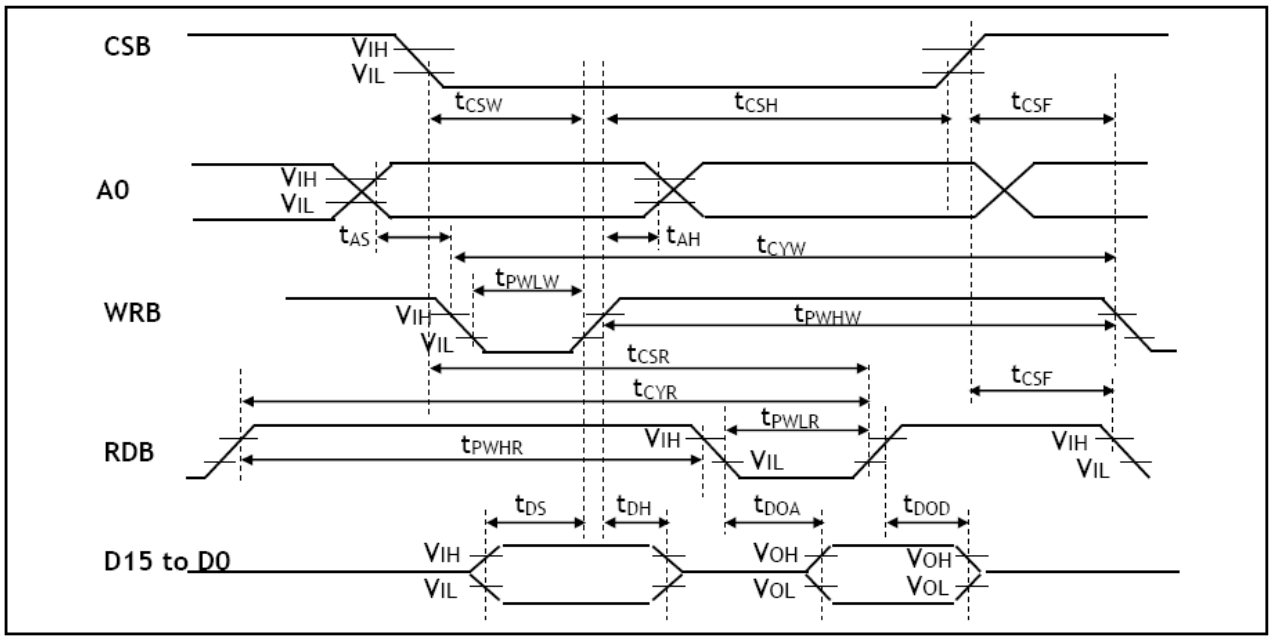
V_{CC_C}=V_{CC_R}=15V, V_{IF}=V_{DD}=2.8V, Output all Open, Display Size full, Others Default

*9) Reference guide => "Internal Regulator for Logic VDD" (Page30)

*10) Default IRVCC Output Voltage = V_{CC_C}*0.76, V_{CC_C}=18V

9 AC CHARACTERISTICS

9.1 Parallel Interface Timing (8080-series MPU)

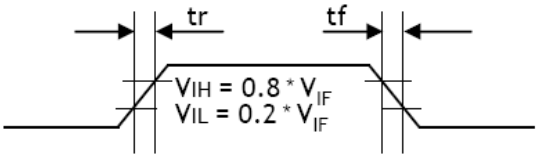


(V_{SS} = 0V, V_{IF} = V_{DD} = 2.8V, Ta = 25℃)

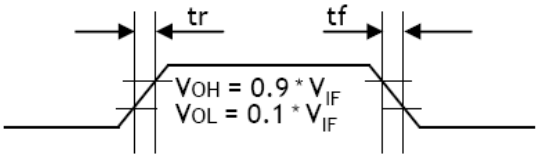
Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	Unit
t_{CSW}, t_{CSR} t_{CSF} t_{CSH}	Chip select setup time Chip select wait time Chip select hold time	-	CSB	40 10 20	- -	- -	ns
t_{AS} t_{AH}	Address setup time Address hold time	-	A0	10 20	- -	- -	ns
t_{CYW} t_{PWHW} t_{PWLW}	Write cycle time Write High Time Write Low Time	-	WRB	100 40 40	-	-	ns
t_{CYR} t_{PWHR} t_{PWLR}	Read cycle time (Data read) Read High (Data read) Read Low (Data read)	-	RDB	500 300 150	-	-	ns
t_{DS} t_{DH}	Data setup time Data hold time	-	D15 to D0	10 20	- -	- -	ns
t_{DOA} t_{DOD}	Data output access time Data output disable time	CL = 30pF		- 10	- -	200 -	ns

NOTE : The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

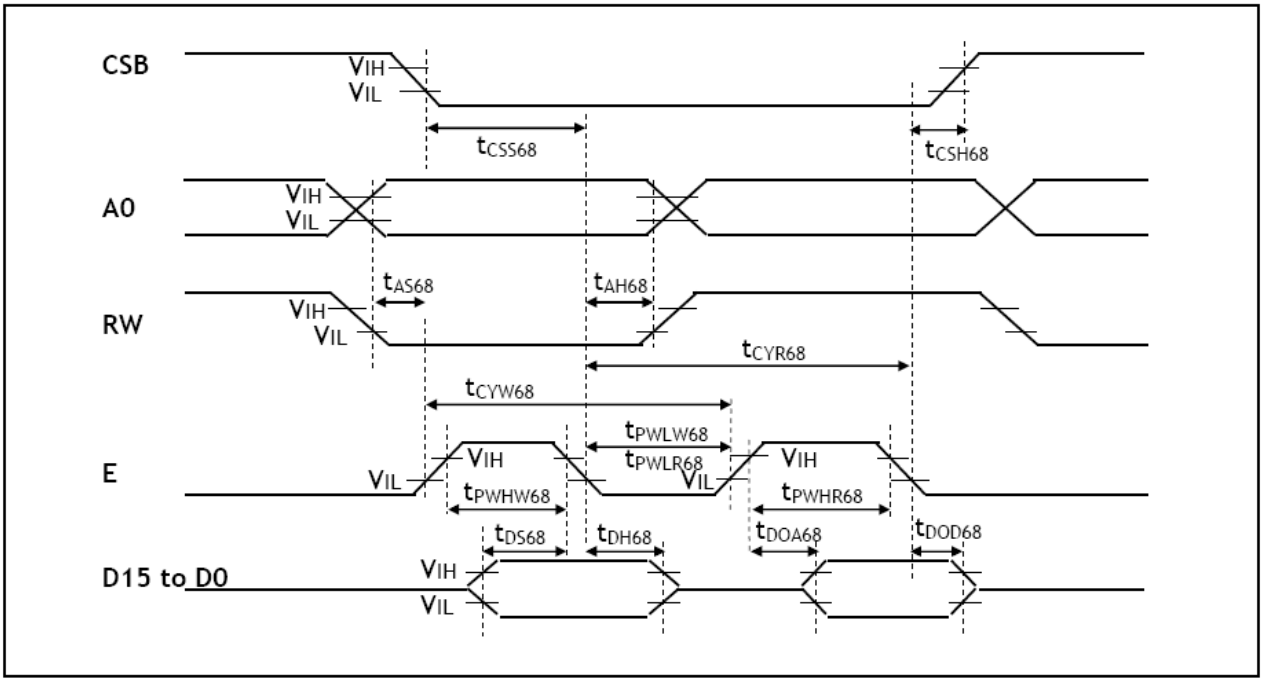
Input Signal Slope



Output Signal Slope



9.2 Paralled Interface Timing(6800-series MPU)

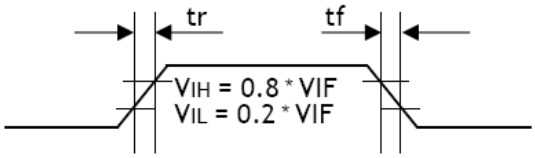


(V_{SS} = 0V, V_{IF} = V_{DD} = 2.8V, Ta = 25℃)

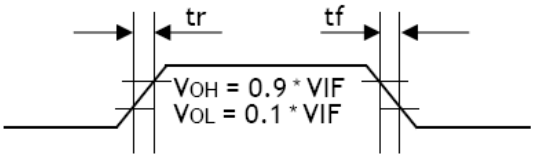
Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	Unit
t_{CSS68} t_{CSH68}	Chip select setup time Chip select hold time	-	CSB	40 20	- -	- -	ns
t_{AS68} t_{AH68}	Address setup time Address hold time	-	A0 RW	10 20	- -	- -	ns
t_{CYW68} t_{PWHW68} t_{PWLW68}	Write cycle time Write High Time Write Low Time	-	E	100 30 40	-	-	ns
t_{CYR68} t_{PWHR68} t_{PWLR68}	Read cycle time (Data read) Read High (Data read) Read Low (Data read)	-	E	500 150 300	-	-	ns
t_{DS68} t_{DH68}	Data setup time Data hold time	-	D15 to D0	10 20	- -	- -	ns
t_{DOA68} t_{DOD68}	Data output access time Data output disable time	CL = 30pF		- 10	- -	200 -	ns

NOTE : The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

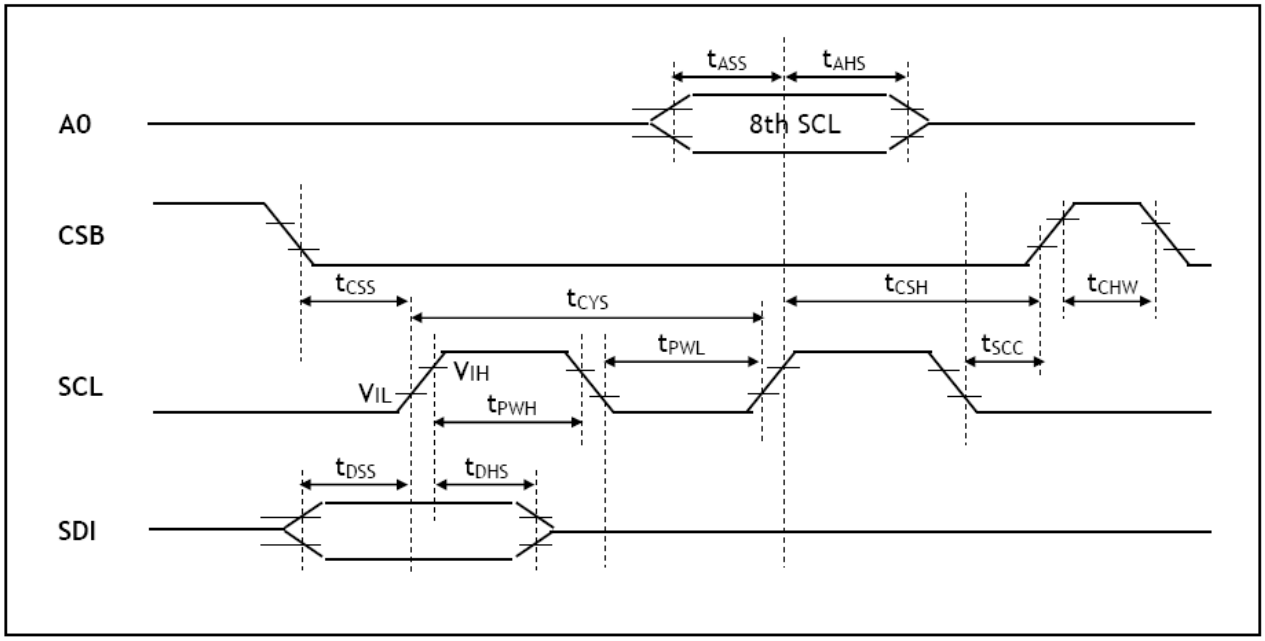
Input Signal Slope



Output Signal Slope



9.3 Serial Interface Timing (write)

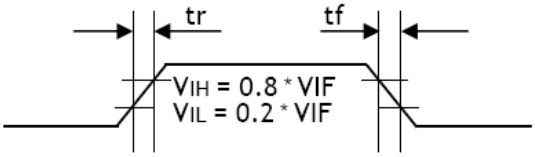


(VSS = 0V, V_{IF} = VDD = 2.8V, Ta = 25℃)

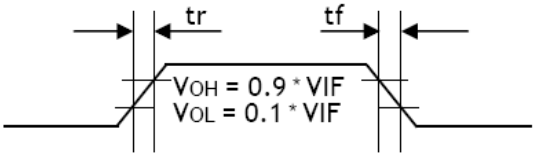
Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	Unit
t_{CYS} t_{PWH} t_{PWL}	Serial clock cycle High pulse Width Low pulse width	-	SCL	50 20 20	- -	- -	ns
t_{ASS} t_{AHS}	A0 setup time A0 hold time		A0	15 25	- -	- -	ns
t_{DSS} t_{DHS}	Data setup time Data hold time		SDI	20 20	- -	- -	ns
t_{CSS} t_{CSH} t_{CSW}	Chip select setup time Chip select hold time Chip select high pulse width	-	CSB	20 50 50	- - -	- - -	ns
t_{SCC}	SCL to Chip select	-	SCL, CSB	15	-	-	ns

NOTE : The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Input Signal Slope



Output Signal Slope



9.4 Driver Timing

CONDITIONS :

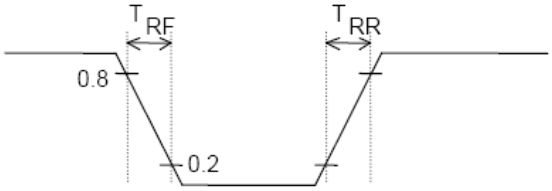
Voltage referenced to Vss

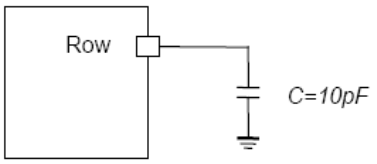
V_{DD}= 2.8V

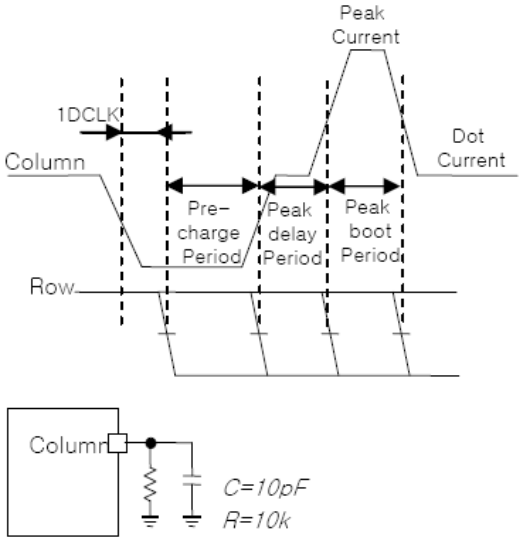
Iout = 100uA

Ta = 25℃t

Item	Signal	Symbol	Min.	Typ.	Max.	Unit
Row Falling Time	R0-R159	T_{RF}	—	—	10	ns
Row Rising Time	R0-R159	T_{RR}	—	—	100	ns







"Row Overlap" command changes Row falling timing.

9.5 Oscillator Frequency

CONDITIONS:

Voltage referenced to Vss

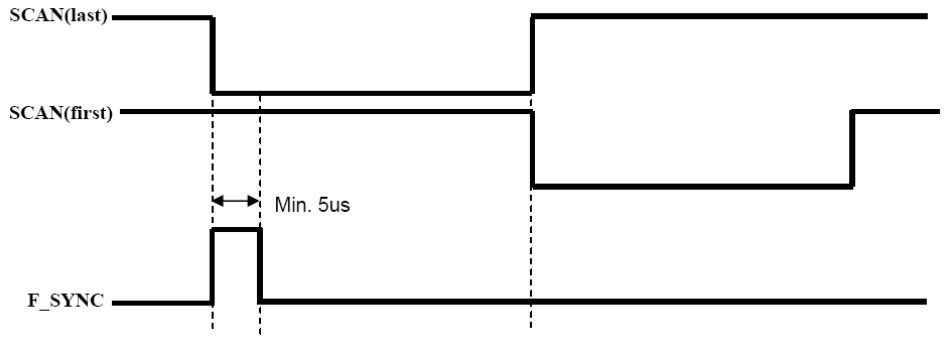
V_{DD}= 2.8V, V_{IF}= 1.6V ~ 3.3V

Ta = 25℃

Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	UNIT
FOSC	Oscillator Frequency For Dot Matrix	Internal Mode		-	4.08 *1)	-	MHz

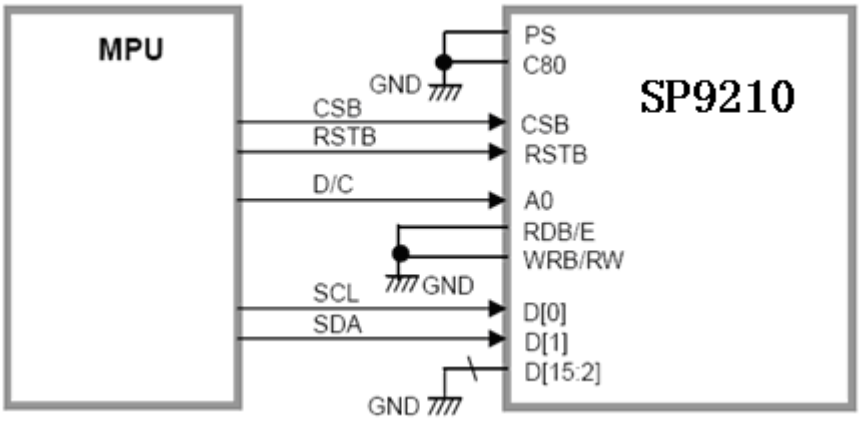
*1) This value is based on 90Hz Frame.

9.6 Frame Sync Signal (F_SYNC)

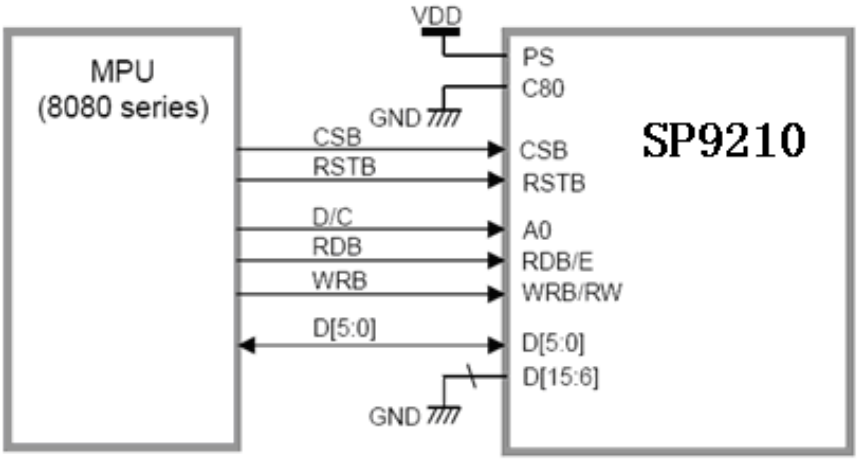


10 APPLICATIONS GUIDE

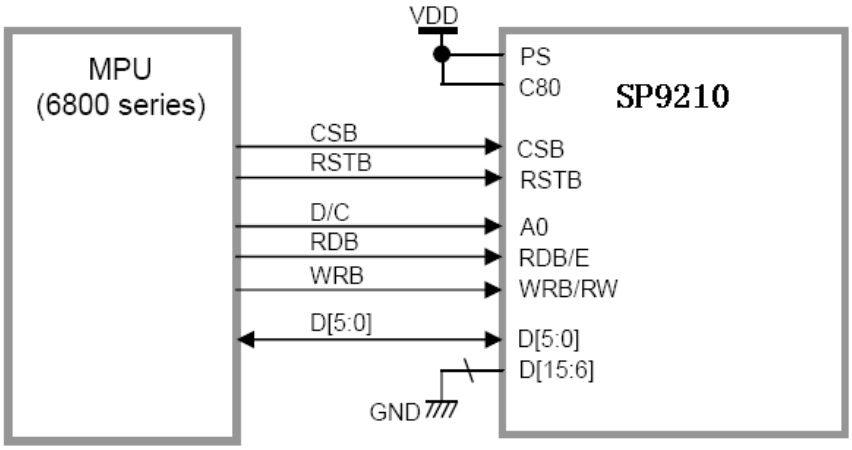
10.1 MPU Serial Interface



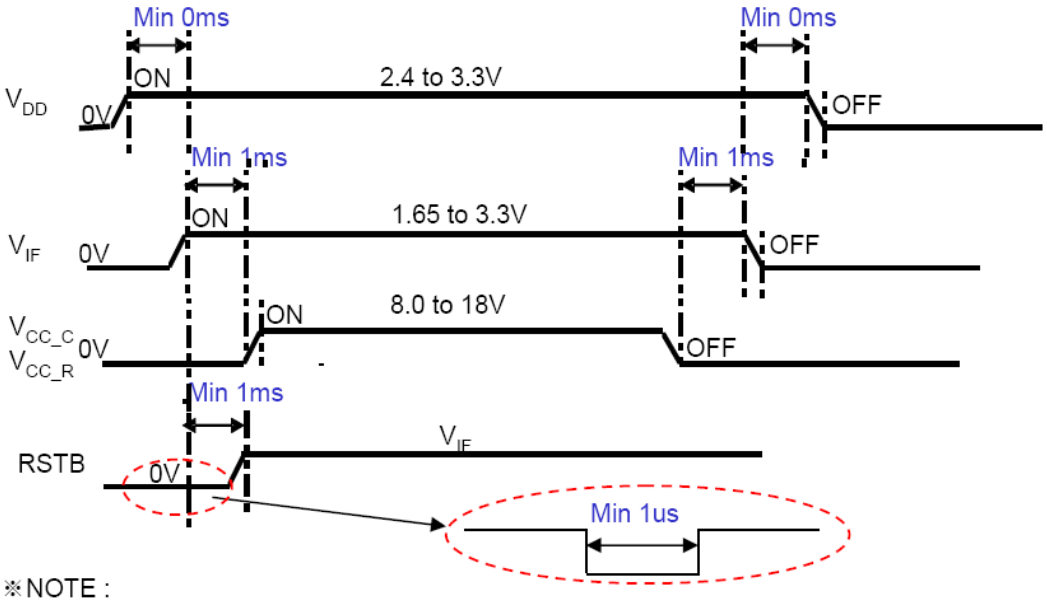
10.2 8080-series MPU Interface With 6 Bit Bus



10.3 6800-series MPU Interface With 6Bit Bus



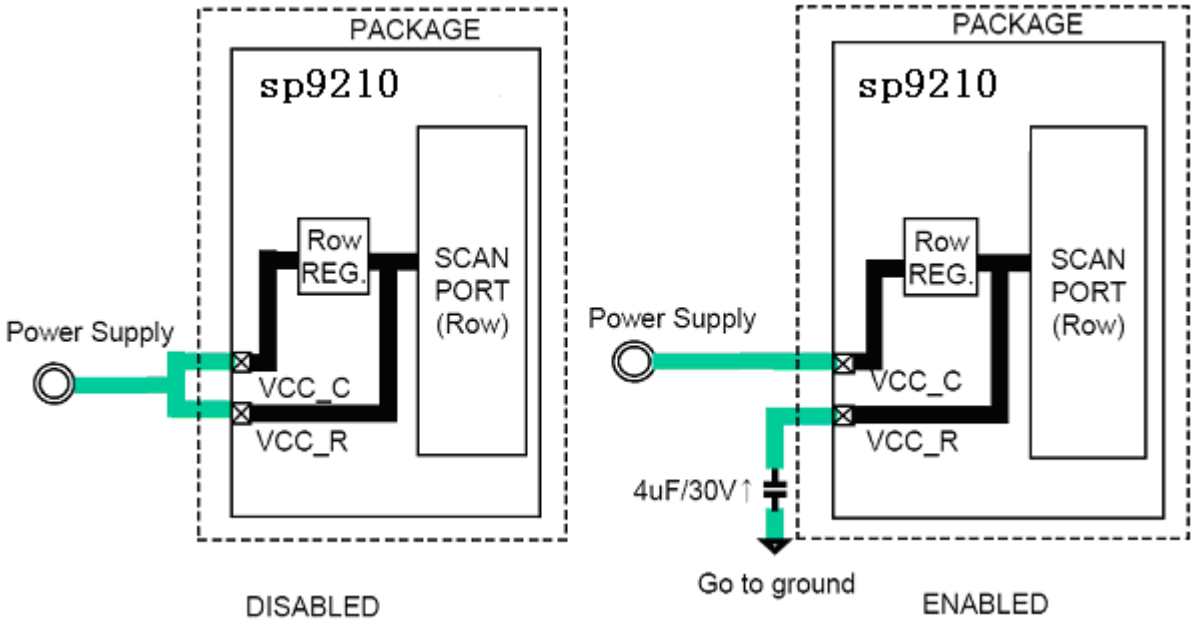
10.4 Power ON/OFF Sequence



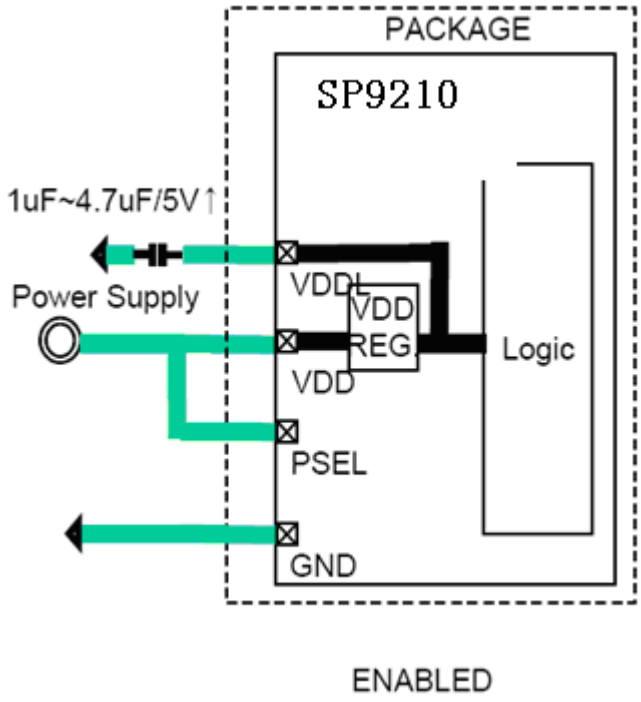
※NOTE :

1. The power on sequence is in order of V_{DD} / V_{IF}→V_{CC_C} / V_{CC_R}

10.5 Internal Regulator for Row Driver

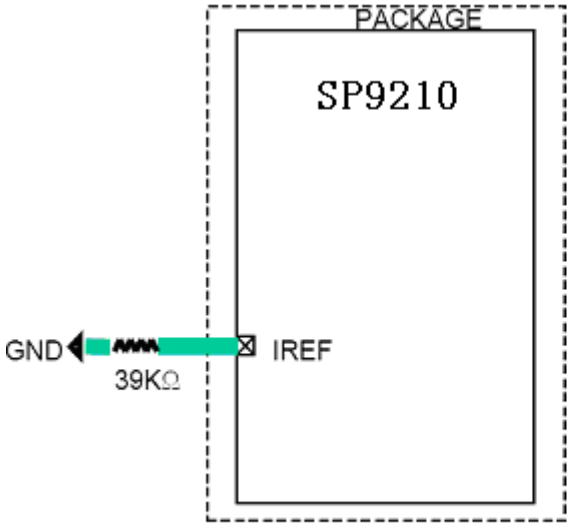


10.6 Internal Regulator for Logic VDD

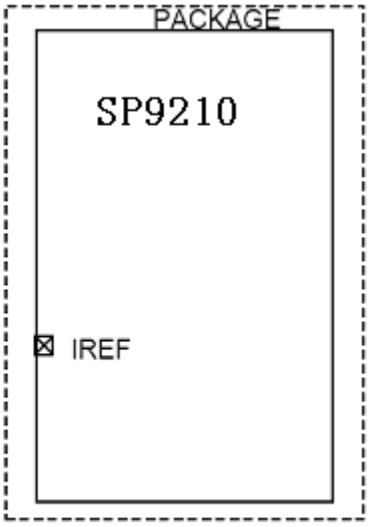


ENABLED

10.7 Basic Circuit for DOT Display

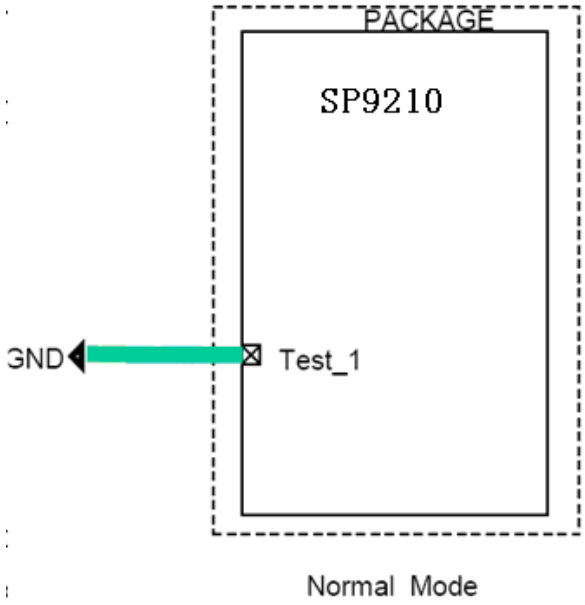


External Resister Mode

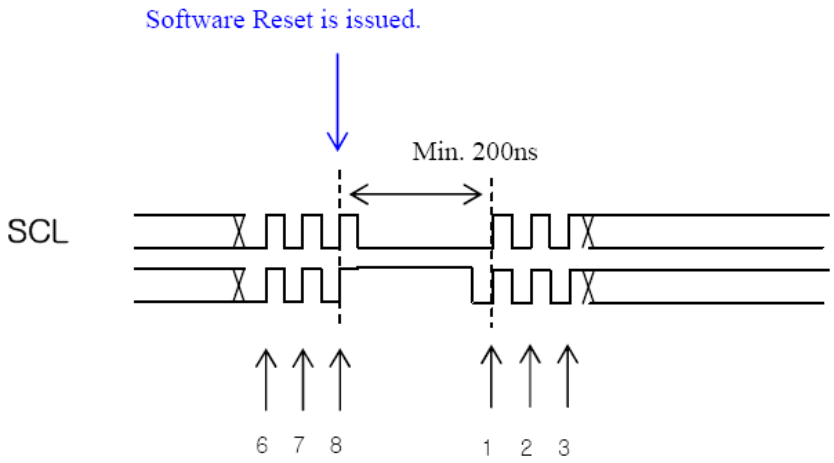


Internal Resister Mode

10.8 Basic Circuit for Test Pin (Test_1)



10.9 Serial I/F Rser Guide using Software Reset command



In the case of Software Reset Command
Minimum 200ns is necessary from 8th SCL up-edge to next 1st SCL up-edge.

APPENDIX - A
COMMAND DESCRIPTION

1. DOT DISPLAY COMMAND

1.1. Software Reset (0x01h)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
SOFTRES	W	L	X	X	0	0	0	0	0	1	

- ◆ All registers are initialized with default value without altering the graphic RAM.
- ◆ All Dot display are turned OFF.
- ◆ The OSC is stopped.

1. 2. Set Dot Matrix Display ON/OFF (0x02h)

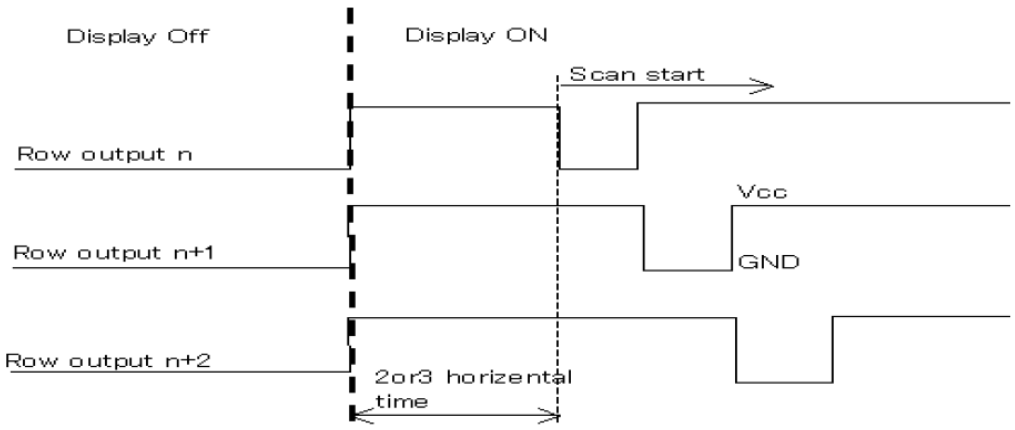
Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
DDISP ON/OFF	W	L			0	0	0	0	1	0	
PARAMETER	W	H			0	0	0	0	0	P0	00h

- ◆ P0 = 0: indicates the dot matrix display turns OFF (Default).
- ◆ P0 = 1: indicates the dot matrix Display turns ON.

※NOTE

Display OFF means

- ▪ All Column Output go to pre-charge level.
- ▪ All Row Output go to the ground level
- ▪ Stop Data transfer from memory to Dot Matrix Driver.



1.3. Set Dot Matrix Display Stand-by ON/OFF (0x03h)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
DSTBYON/OFF	W	L			0	0	0	0	1	1	
PARAMETER	W	H			0	0	0	0	0	P0	01h

◆ P0 = 0 : Indicates the dot oscillator is starting. And it does not make the dot matrix display turn ON.
◆ P0 = 1 : Indicates the dot oscillator is stopping. And it make the dot matrix display OFF.

※NOTE

After software or hardware reset command is executed, it makes dot matrix display stand-by ON.

1. 4. Set OSC Control (0x04h)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
DFRAME	W	L			0	0	0	1	0	0	
PARAMETER	W	H			0	M1	M0	F2	F1	F0	02h

◆ Parameter Definition

F2	F1	F0	Frame Frequency *1)
0	0	0	60Hz
0	0	1	75Hz
0	1	0	90Hz(Default) *2)
0	1	1	105Hz
1	0	0	120Hz

◆ OSC mode selection
m[1:0] =00 Internal RC Oscillation mode

*1) Conditions
Pre-Charge_Width(Pcw) = 16
Peak-Pulse_Width(Ppw) = 10
Peak_Pulse_Delay(Pdw) = 1
Scan Nember(Scan_N) = 160

*2) Osc_Frequency(Fosc) = 4.08 MHz

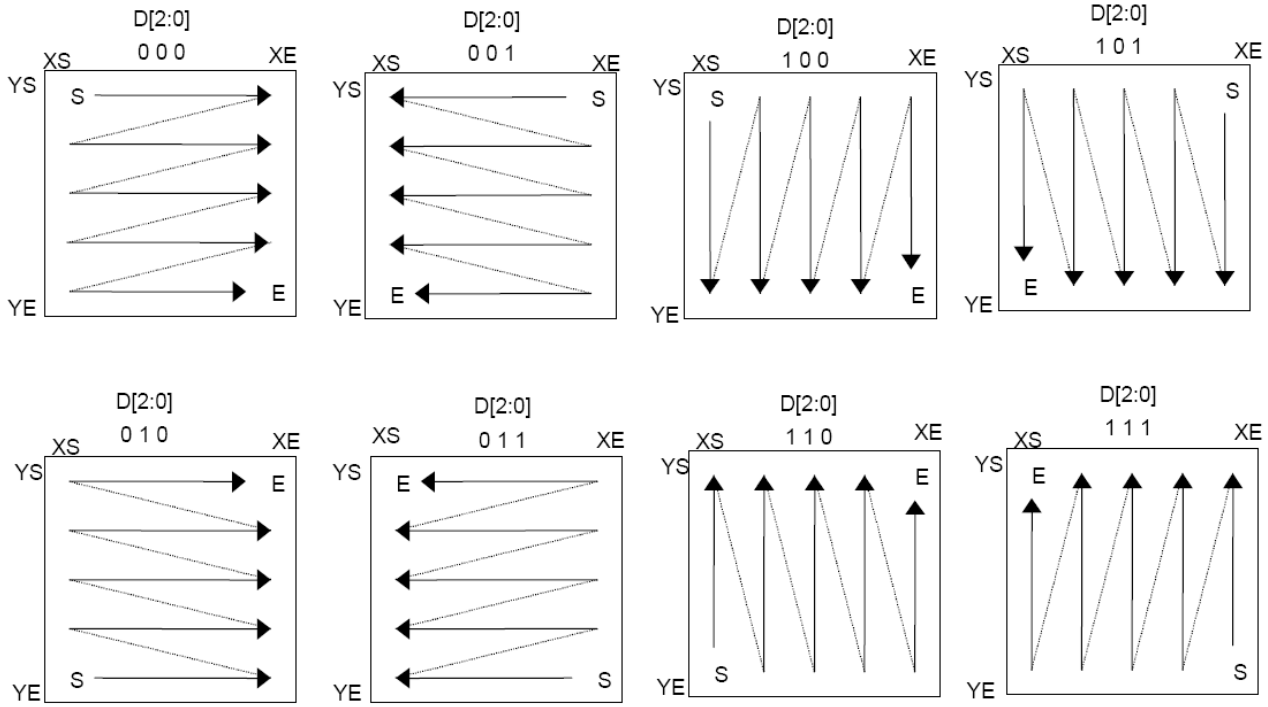
Frame Frequency(Hz) = 1 / [(1/Fosc)*(Pcw+Ppw+Pdw+256) * Scan_N]

* Frame Frequency Table (Refer to Page 51)

1.5. Set Graphic RAM Writing Direction (0x05h)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
WriteDrection	W	L			0	0	0	1	0	1	
PARAMETER	W	H			0	0	D3	D2	D1	D0	00h

D3=0: indicates the Graphic RAM is accessed by order of RGB.
D3=1: indicates the Graphic RAM is accessed by order of BGR



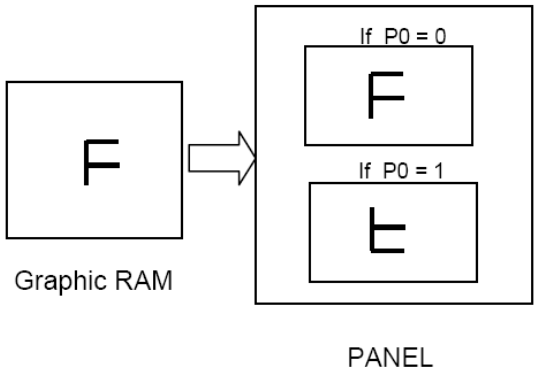
1.6. Set Row Scan Direction (0x06h)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
ScanDirection	W	L			0	0	0	1	1	0	
PARAMETER	W	H			0	0	0	0	0	P0	00h

P0 = 0: indicates row address is scanning from min. to max.

P0= 1: indicates row address is scanning from max. to min.

For example is as bellows;



1. 7. Set Display Size (0x07h)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
DispSize	W	L			0	0	0	1	1	1	
1st Xstart 1	W	H			-	-	-	FX6	FX5	FX4	00h
2nd Xstart 2	W	H			-	-	FX3	FX2	FX1	FX0	00h
3rd Xend 1	W	H			-	-	-	TX6	TX5	TX4	07h
4th Xend 2	W	H			-	-	TX3	TX2	TX1	TX0	0Fh
5th Ystart 1	W	H			-	-	FY7	FY6	FY5	FY4	00h
6th Ystart 2	W	H			-	-	FY3	FY2	FY1	FY0	00h
7th Yend 1	W	H			-	-	TY7	TY6	TY5	TY4	09h
8th Yend 2	W	H			-	-	TY3	TY2	TY1	TY0	0Fh

◆ Setting Row and Column Outputs Range (= Active area).

◆ From FX to TX ：The range of active Column Outputs setting (Range：00h up to 7Fh)

Setting Value = Pixel number –1

"Xend＜Xstart" is inhibited.

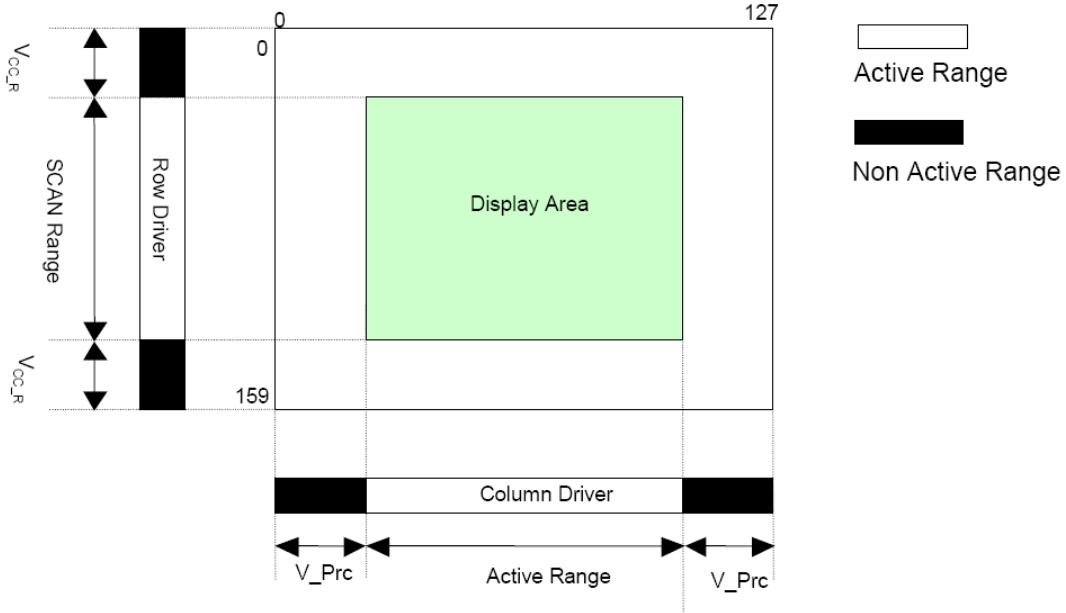
◆ From FY to TY ：The range of active Row Outputs setting(Range：00h up to 9Fh)

Setting Value = Pixel number –1

"Yend＜Ystart" is inhibited.

※NOTE

1. The outputs that are out of setting range go to Pre_charge voltage for Column and V_{CC_R} for Row.
2. Line scan frequency is same under any display size. Frame frequency is changed by DispSize command.



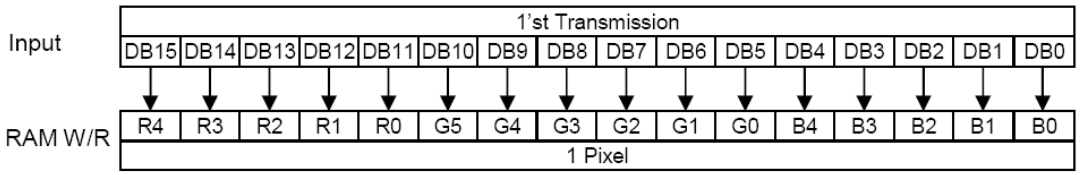
1.8. Set Interface Bus Type (0x08h)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
I/F Bus Sel	W	L			0	0	1	0	0	0	
Parameter	W	H			-	-	-	-	P1	P0	00h

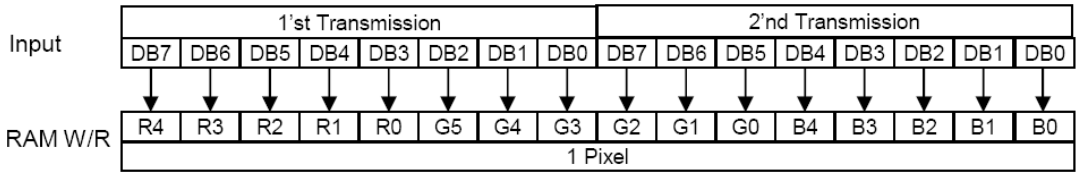
P1	P0	Description
0	0	6Bit I/F Bus
0	1	8Bit I/F Bus
1	1	16Bit I/F Bus

Instruction

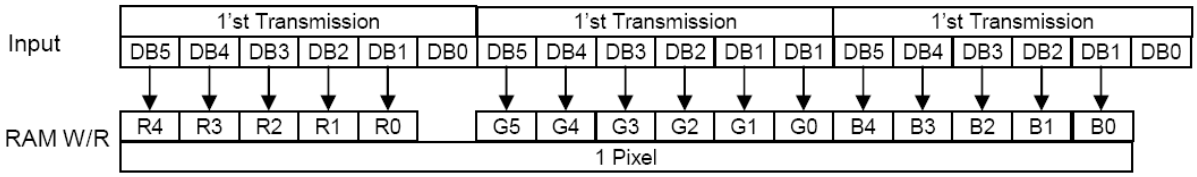
16-Bit I/F(65K color)



8-Bit I/F(65K color)



6-Bit I/F(65K color)



1. 9. Set Masking Data (0x09h)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
Data_Masking	W	L			0	0	1	0	0	1	
PARAMETER	W	H			-	RV	-	R	G	B	07h

◆ When RV ="1", Output Data = (Data XOR "FFFFh") AND Pallet (R,G,B).

◆ When RV ="0", Data AND Pallet(R,G,B) ⇒ Output Data

◆ For example, If pallet is (0,1,1) then R data is 00h and G&B is FFFFh.

1.10. Set Read/Write Box Data (0x0Ah)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
MBOXSize	W	L			0	0	1	0	1	0	
1st Xstart 1	W	H			-	-	-	XS6	XS5	XD4	00h
2nd Xstart 2	W	H			-	-	XS3	XS2	XS1	XS0	00h
3rd Xend 1	W	H			-	-	-	XE6	XE5	XE4	07h
4th Xend 2	W	H			-	-	XE3	XE2	XE1	XE0	0Fh
5th Ystart 1	W	H			-	-	YS7	YS6	YS5	YD4	00h
6th Ystart 2	W	H			-	-	YS3	YS2	YS1	YS0	00h
7th Yend 1	W	H			-	-	YE7	YE6	YE5	YE4	09h
8th Yend 2	W	H			-	-	YE3	YE2	YE1	YE0	0Fh

XS6-XS0 ：X axis Reading/Writing Start Point (Range: 00h ~ 7Fh)
XE6-XE0 ：X axis Reading/Writing End Point （Range：00h ~ 7Fh）
"XE＜XS" is inhibited.

YS7-YS0 ： Y axis Reading/Writing Start Point (Range : 00h~9Fh).
YE7-YE0 ： Y axis Reading/Writing Start Point (Range : 00h~9Fh).
"YE<YS"is inhibited.

◆ After this command executes, writing address is set like under table.

Writing Direction Mode	X address	Y address
00	XS	YS
01	XE	YS
10	XS	YE
11	XE	YE

※NOTE : Refer to the Writing Direction Set Command.

1.11. Set Display Start Address (0x0Bh)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
DISPStart	W	L			0	0	1	0	1	1	
1st Parameter	W	H			-	-	-	DX6	DX5	DX4	00h
2nd Parameter	W	H			-	-	DX3	DX2	DX1	DX0	00h
3rd Parameter	W	H			-	-	DY7	DY6	DY5	DY4	00h
4th Parameter	W	H			-	-	DY3	DY2	DY1	DY0	00h

◆ This command shift the memory reading address.
◆ DX6-DX0 ：X axis Reading Start address (Range: 00h ~ 7Fh)
◆ DY7-DY0 ：Y axis Reading Start address （Range：00h ~ 9Fh）

1.12. Read/Write Dot matrix Display Data (0x0Ch)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0
DataWrite/Read	W	L			0	0	1	1	0	0

Parameter Mode	W/R	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
16 Bit Write/Read	W/R	H	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

Parameter Mode	W/R	A0	D8	D7	D6	D5	D4	D3	D2	D1	D0
8 Bit Write/ Read	W	H		R4	R3	R2	R1	R0	G5	G4	G3
8 Bit Write/ Read	W	H		G2	G1	G0	B4	B3	B2	B1	B0

Parameter Mode	W/R	A0	D8	D7	D6	D5	D4	D3	D2	D1	D0
6Bit Write/ Read	W/R	H				R4	R3	R2	R1	R0	-
6Bit Write/ Read	W/R	H				G5	G4	G3	G2	G1	G0
6Bit Write/ Read	W/R	H				B4	B3	B2	B1	B0	-

- ◆ This command can't write data in the out of reading / writing-box.
- ◆ Address is auto increment acceding to WriteDirection setting direction.
- ◆ When memory address increment/decrement is reached at the end of reading /writing-box memory write finish.
- ◆ If you read / write again, re-inter "Data Write/Read" command.

◆ Data Write Sequence

Seq.	RW	A0	16Bit DATA BUS	8 Bit DATA BUS	6 Bit DATA BUS
1	W	L	Data Write/ Read command	Data Write/ Read command	Data Write / Read command
2	W	H	Write 1st Parameter	Write 1st Upper Parameter.	Write 1st Upper Parameter.
3	W	H	Write 2nd Parameter	Write 1st Lower Parameter.	Write 1st Middle Parameter.
4	W	H	:	:	Write 1st Lower Parameter.
:	:	:	:	:	:
N+1	W	H	Write nth Parameter	:	:
:	:	:		:	:
2N	W	H		Write nth Upper Parameter.	:
2N+1	W	H		Write nth Lower Parameter.	:
:	:	:			:
3N-1	W	H		.	Write nth Upper Parameter.
3N	W	H			Write nth Middle Parameter.
3N+1	W	H			Write nth Lower Parameter.

◆ Data Read Sequence

Seq.	RW	A0	16 Bit Mode DATA BUS	8 Bit Mode DATA BUS	6 Bit Mode DATA BUS
1	W	L	DataWrite/ Read command	Data Write/ Read command	Data Write/ Read command
2	R	H	Dummy	Dummy	Dummy
3	R	H	Read 1st Parameter	Dummy	Dummy
4	R	H	Read 2nd Parameter	Read 1st Upper Parameter.	Dummy
5	R	H		Read 1st Lower Parameter.	Read 1st Upper Parameter.
6	R	H			Read 1st Middle Parameter.
7	R	H	:	:	Read 1st Lower Parameter.
:	:	:	:	:	:
N+2	R	H	Read nth Parameter	:	:
:	:	:		:	:
2N+2	R	H		Read nth Upper Parameter.	:
2N+3	R	H		Read nth Lower Parameter.	:
:	:	:		:	:
3N+2	R	H			Read nth Upper Parameter.
3N+3	R	H			Read nth Middle Parameter.
3N+4	R	H			Read nth Lower Parameter.

1.13. Read Register Status (0x0Dh)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
READREG	W	L			0	0	1	1	0	1	
Parameter	R	H			D5	D4	D3	D2	D1	D0	
:	R	H			:	:	:	:	:	:	
Parameter	R	H			D5	D4	D3	D2	D1	D0	

◆ Read out specific internal register

Order	Register
1	DDISP_ON/OFF, DSTBY_ON/OFF
2	DispSize XS<6:4>
3	DispSize XS<3:0>
4	DispSize XE<6:4>
5	DispSize XE<3:0>
6	DispSize YS<7:4>
7	DispSize YS<3:0>
8	DispSize YE<7:4>
9	DispSize YE<3:0>
10	Row Overlap<5:0>
11	IC TEST Mode

1.14. Set Dot Matrix Current Level (0x0Eh)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
DotCurrent	W	L			0	0	1	1	1	0	
1st Parameter	W	H			–	–	IR7	IR6	IR5	IR4	00h
2nd Parameter	W	H			–	–	IR3	IR2	IR1	IR0	00h
3rd Parameter	W	H			–	–	IG7	IG6	IG5	IG4	00h
4th Parameter	W	H			–	–	IG3	IG2	IG1	IG0	00h
5th Parameter	W	H			–	–	IB7	IB6	IB5	IB4	00h
6th Parameter	W	H			–	–	IB3	IB2	IB1	IB0	00h

◆ Parameter Definition (1.0uA Step)

I[7:0]	Output Current [Iref]
00h	0.0 uA
01h	1.0 uA
:	:
FEh	254.0 uA
FFh	255.0 uA

1.15. Set Dot Matrix Peak Current Level (0x0Fh)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
PeakCurrent	W	L			0	0	1	1	1	1	
1st Parameter	W	H			PR5	PR4	PR3	PR2	PR1	PR0	00h
2nd Parameter	W	H			PG5	PG4	PG3	PG2	PG1	PG0	00h
3rd Parameter	W	H			PB5	PB4	PB3	PB2	PB1	PB0	00h

◆ Parameter Definition (16uA Step)

I[5:0]	Output Current [Iref]
00h	0.0 uA
01h	16.0 uA
:	:
3Eh	992.0 uA
3Fh	1008.0 uA

1.16. Set Pre-Charge Width (0x1Ch)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
PreC_Width	W	L			0	1	1	1	0	0	
1st Parameter	W	H			T5	T4	T3	T2	T1	T0	08h

◆ Parameter Definition (DCLK Unit)

T[5:0] *1)	Pre-Charge Pulse Width
02h	2
:	
08h	8 (Default)
:	
3Eh	62
3Fh	63

*1) Don't use a parameter
"T[5:0]=00h" & "T[5:0]=01h"

◆ Parameter Range : 02h ~ 3Fh

1.17. Set Peak Pulse Width (0x1Dh)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
PeakWidth	W	L			0	1	1	1	0	1	
1st Parameter	W	H			W5	W4	W3	W2	W1	W0	0Ah (for Red)
2nd Parameter	W	H			W5	W4	W3	W2	W1	W0	0Ah (for Green)
3rd Parameter	W	H			W5	W4	W3	W2	W1	W0	0Ah (for Blue)

◆ Parameter Definition (DCLK Unit)

W[5:0] *1)	Peak Pulse Width
01h	1
:	:
0Ah	10 (Default)
:	:
3Eh	62
3Fh	63

*1) Don't use a parameter "W[5:0]=00h".

◆ Parameter Range : 01h ~ 3Fh

1.18. Set Peak Pulse Delay (0x1Eh)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
PeakDelay	W	L			0	1	1	1	1	0	
Parameter	W	H					W3	W2	W1	W0	01h

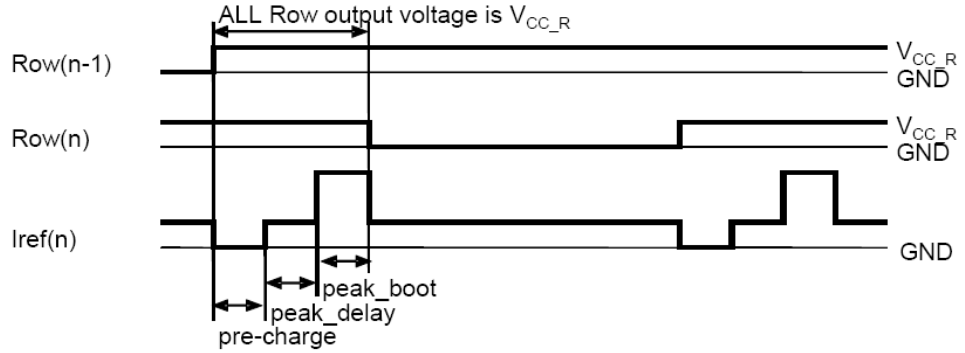
◆ Parameter Definition (DCLK Unit)

W[3:0]	Peak Pulse Width
00h	0
01h	1(Default)
:	:
05h	5
:	:
0Eh	14
0Fh	15

◆ Parameter Range : 00h ~ 0Fh

1.19. Set Row Scan Operation (0x1Fh)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
Row_Scan	W	L			0	1	1	1	1	1	
Parameter	W	H			D5	D4	D3	-	D1	D0	00h



◆ Row Output V_{CC_R} timing setting table

D5	D4	All Row V_{CC_R} Time
0	0	None (Default)
0	1	Pre-Charge Timing
1	0	Pre-Charge + Peak Delay Timing
1	1	Pre-Charge + Peak Delay + Max(RGB)Peak boot Timing

◆ Parameter Definition

D3=0 Normal Scan.

D3=1 All Row are in GND.

◆ Row Scan Sequence

D1,D0	Row Scan Mode
00	Mode 1 : alternate scan mode. (Default)
01	Mode 2 : sequential scan mode.
10	Mode 3 : simultaneous scan mode. (half period)

D1,D0	DispDirection	Case of 160 Line Scan
00	0	R0,R1,R2 ….. R158,R159,R0,R1
	1	R159,R158,R157 ….. R1,R0,R159,R158
01	0	R0,R2,R4 ….. R158,R1,R3, ….. R159,R0
	1	R159,R157,R155 ….. R1,R158,R156 ….. R0,R159
10	0	R0,R2 ….. R158,R0,R2 ….. R1,R3 ….. R159,R1,R3 …..
	1	R159,R157 ….. R1,R159,R157 ….. R158,R156 ….. R0,R158,R156 …..

◆ In Mode 3, Maximum Row number is 80 line at Display Size setting.

2. Optional Command

2.1. Set IC Test Mode (0x3Dh)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
TESTCNT	W	L			1	1	D				00h

Set IC Test Mode (0x3Eh)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
TESTCNT	W	L			1	1	E				

2.2. Set Internal Regulator for Row Scan (0x30h)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
VCC_R_SEL	W	L			1	1	0	0	0	0	
Parameter	W	H			-	D4	D3	D2	D1	D0	03h

"D4" = "1" => Internal regulator enable
"D4" = "0" => Internal regulator disable

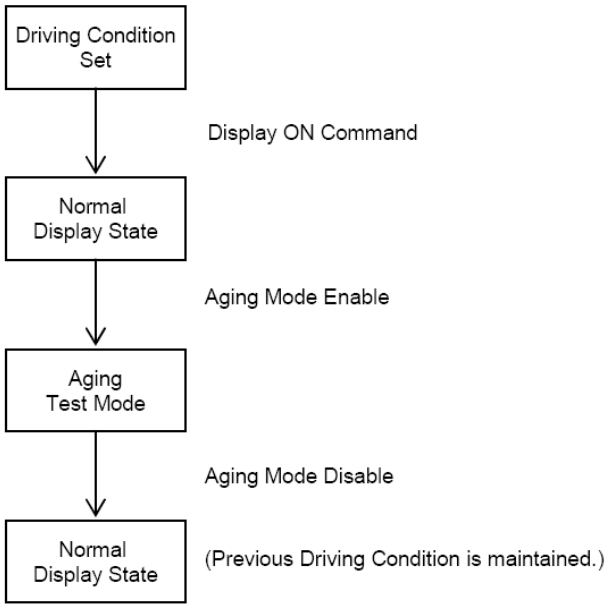
D[3:0]	V_{CC_R}
0000	VCC_C ×0.94
0001	VCC_C ×0.88
0010	VCC_C ×0.82
0011	VCC_C ×0.76
0100	VCC_C ×0.70
0101	VCC_C ×0.64
0110	VCC_C ×0.58
0111	VCC_C ×0.52
1000	VCC_C ×0.46
1001	VCC_C ×0.40

2. 3. Set AGING Mode (0x35h)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
AGING_EN	W	L			1	1	1	0	0	1	
Parameter	W	H			-	-	-	-	-	P0	00h

- If P0 = 0, then AGING Mode is disable.
- If P0 = 1, then AGING Mode is enable.

- This command is used only for aging test mode.
- If P0 = 1, then column state is always forced to the data drive period regardless of the driving conditions.



2. 4. Set Gamma Correction Table Set (0x3Ah)

INSTRUCTION	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
Gamma Tune	W	L			3		A				
R_PW0	W	H			-	-	I7	I6	I5	I4	00h
	W	H			-	-	I3	I2	I1	I0	00h
R_PW1	W	H			-	-	I7	I6	I5	I4	00h
	W	H			-	-	I3	I2	I1	I0	08h
⋮							⋮				
R_PW30	W	H			-	-	I7	I6	I5	I4	0Fh
	W	H			-	-	I3	I2	I1	I0	00h
R_PW31	W	H			-	-	I7	I6	I5	I4	0Fh
	W	H			-	-	I3	I2	I1	I0	0Fh
G_PW0	W	H			-	-	I7	I6	I5	I4	00h
	W	H			-	-	I3	I2	I1	I0	00h
G_PW1	W	H			-	-	I7	I6	I5	I4	00h
	W	H			-	-	I3	I2	I1	I0	04h
⋮							⋮				
G_PW62	W	H			-	-	I7	I6	I5	I4	0Fh
	W	H			-	-	I3	I2	I1	I0	08h
G_PW63	W	H			-	-	I7	I6	I5	I4	0Fh
	W	H			-	-	I3	I2	I1	I0	0Fh
B_PW0	W	H			-	-	I7	I6	I5	I4	00h
	W	H			-	-	I3	I2	I1	I0	00h
B_PW1	W	H			-	-	I7	I6	I5	I4	00h
	W	H			-	-	I3	I2	I1	I0	08h
⋮							⋮				
B_PW30	W	H			-	-	I7	I6	I5	I4	0Fh
	W	H			-	-	I3	I2	I1	I0	00h
B_PW31	W	H			-	-	I7	I6	I5	I4	0Fh
	W	H			-	-	I3	I2	I1	I0	0Fh

64 Parameters

128 Parameters

64 Parameters

2. 5. Set Gamma Correction Table Initialize (0x3Bh)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
Gamma_initial	W	L			1	1	1	0	1	1	

- This command initialize the Gamma Table to the linear scale.
  Linear Scale : 00h, 04h, 08h, 0Ch, ..., F4h, F8h, FFh (Green)
  Linear Scale : 00h, 08h, 10h, 18h, ..., E8h, F0h, FFh (Red, Blue)

2. 6. Even_Odd Compare Register Set (0x36h)

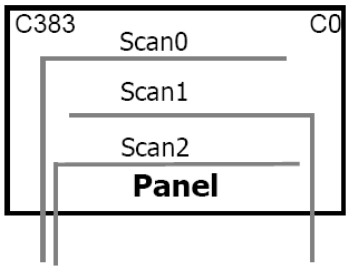
Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
EOCompData	W	L			3		6				
ParameterR	W	H			D5	D4	D3	D2	D1	D0	00h
ParameterG	W	H			D5	D4	D3	D2	D1	D0	00h
ParameterB	W	H			D5	D4	D3	D2	D1	D0	00h

2. 7. Even_Odd Control Set (0x37h)

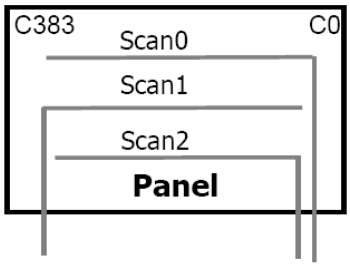
Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
EOControl	W	L			3		7				
Parameter	W	H			BI	GI	RI	–	SEL	EN	00h

◆ EN = 1 : Even_Odd Function Enable.
◆ EN = 0 : Even_Odd Function Disable.

◆ SEL = 0



◆ SEL = 1



◆ RI / GI / BI = 1 : Current Weight is 2.
◆ RI / GI / BI = 0 : Current Weight is 1.

2. 8. Set Even_Odd Gray Register Set (0x38h)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
EOGrayReg	W	L			3			8			
EOGR0	W	H			D5	D4	D3	D2	D1	D0	00h
EOGR1	W	H			D5	D4	D3	D2	D1	D0	02h
EOGR2	W	H			D5	D4	D3	D2	D1	D0	04h
⋮					⋮	⋮	⋮	⋮	⋮	⋮	
EOGR29	W	H			D5	D4	D3	D2	D1	D0	3Ah
EOGR30	W	H			D5	D4	D3	D2	D1	D0	3Ch
EOGR31	W	H			D5	D4	D3	D2	D1	D0	3Fh
EOGG0	W	H			D5	D4	D3	D2	D1	D0	00h
EOGG1	W	H			D5	D4	D3	D2	D1	D0	02h
EOGG2	W	H			D5	D4	D3	D2	D1	D0	04h
⋮					⋮	⋮	⋮	⋮	⋮	⋮	
EOGG29	W	H			D5	D4	D3	D2	D1	D0	3Ah
EOGG30	W	H			D5	D4	D3	D2	D1	D0	3Ch
EOGG31	W	H			D5	D4	D3	D2	D1	D0	3Fh
EOGB0	W	H			D5	D4	D3	D2	D1	D0	00h
EOGB1	W	H			D5	D4	D3	D2	D1	D0	02h
EOGB2	W	H			D5	D4	D3	D2	D1	D0	04h
⋮					⋮	⋮	⋮	⋮	⋮	⋮	
EOGB29	W	H			D5	D4	D3	D2	D1	D0	3Ah
EOGB30	W	H			D5	D4	D3	D2	D1	D0	3Ch
EOGB31	W	H			D5	D4	D3	D2	D1	D0	3Fh

32 Parameters

32 Parameters

32 Parameters

2. 9. Column Port Current Resister Mode Set (0x3Fh)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
ColResSet	W	L			3		F				
Parameter	W	H			-	-	-	-	-	-	00h
Parameter	W	H			-	-	-	-	EXT	-	00h

◆ EXT = 0 : Internal resister mode for column port current.

◆ EXT = 1 : External resister mode for column port current.

3. Screen Saver Command

3.1. Set Screen Saver Sleep Timer (0x10h)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
S_SleepTimer	W	L			0	1	0	0	0	0	
1st Parameter	W	H			-	-	T6	T5	T4	T3	00h
2nd Parameter	W	H			-	-	T2	T1	T0	-	00h

◆ The period of Screen Saver Sleep Timer is 0-127sec.(Frame Freq. : 90Hz)

3.2. Set Screen Saver Sleep Start (0x11h)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
S_SleepStart	W	L			0	1	0	0	0	1	
Parameter	W	H			-	-	-	-	-	P0	00h

◆ This command stop screen saver and display off after setting time will gone.
P0 = "0" : Sleep Stop (Default)
P0 = "1" : Sleep Start.

◆ S_SleepStart is execute the follows after setting time will gone.
S_SaverStop (SS = 0h)
S_SleepStart (P0 = 0h)
DDIPS_OFF (P0 = 0h)

3.3. Set Screen Saver Step Timer (0x12h)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
S_StepTimer	W	L			0	1	0	0	1	0	
1st Parameter	W	H					T6	T5	T4	T3	00h
2nd Parameter	W	H					T2	T1	T0	-	00h

◆ Screen Saver event timer setting

3.4. Set Screen Saver Step Unit (0x13h)

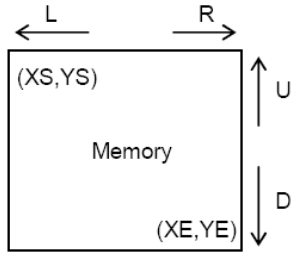
Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
S_StepUnit	W	L			0	1	0	0	1	1	
Parameter	W	H			-	-	-	-	S1	S0	00h

◆ Parameter Definition (Frame Freq. : 90Hz)
S[1:0] = 0 : Timer Stop (Default)
S[1:0] = 1 : 1 ms Unit
S[1:0] = 2 : 0.1s Unit

3.5. Set Screen Saver Condition (0x16h)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
S_Condition	W	L			0	1	0	1	1	0	
Parameter	W	H			-	-	U	D	R	L	00h

◆ UDRL : Direction (Default = 0h)



3.6. Set Screen Saver Start/Stop (0x17h)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
S_Start/Stop	W	L			0	1	0	1	1	1	
Parameter	W	H			-	-	-	-	-	SS	00h

SS="0": Screen Saver Stop (Default)
SS="1": Screen Saver Start

3.7. Set Screen Saver Mode (0x18h)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
S_Mode	W	L			0	1	1	0	0	0	
Parameter	W	H			-	-	S3	S2	S1	S0	02h

S[3:0]	Screen Saver Mode
0	-
1	-
2	S_MultiScroll
3	-
4	-
5	-
6	-
7	-
8	-

3.8. Set Screen Saver MultiScroll

◆ Up Down Right Left Scroll.

Time Step	Move Step	Box	LO
Moving by One pixel	1 pixel fixed	No relation	No relation

U	D	R	L	Meaning
1	0	0	0	Up Scroll
0	1	0	0	Down Scroll
0	0	1	0	Right Scroll
0	0	0	1	Left Scroll

4. Xtalk Command

4. 1. Set XTALK Condition Setting (0x31h)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
XTALK_Mode	W	L			3		1				
1st Parameter	W	H			RS5	RS4	RS3	RS2	RS1	RS0	00h
2nd Parameter	W	H			–	–	RD3	RD2	RD1	RD0	00h
3rd Parameter	W	H			GS5	GS4	GS3	GS2	GS1	GS0	00h
4th Parameter	W	H			–	–	GD3	GD2	GD1	GD0	00h
5th Parameter	W	H			BS5	BS4	BS3	BS2	BS1	BS0	00h
6th Parameter	W	H			–	–	BD3	BD2	BD1	BD0	00h

S[2：0]	Mode 1 Sampled Level
000	Level 0 is sampled
001	Level 1 is sampled
010	Level 2 is sampled
011	Level 3 is sampled
100	Level 4 is sampled
101	Level 5 is sampled

S[5:3]	Mode 2 Sampled Level
000	Level 0 is sampled
001	Level 1 is sampled
010	Level 2 is sampled
011	Level 3 is sampled
100	Level 4 is sampled
101	Level 5 is sampled

D[1：0]	Mode 1 Control Unit
00	Unit 0 (0.125uA)
01	Unit 1 (0. 25uA)
10	Unit 2 (0.5uA)
11	Unit 3 (1.0uA)

D[3:2]	Mode 2 Control Unit
00	Unit 0 (0.5uA)
01	Unit 1 (1uA)
10	Unit 2 (2uA)
11	Unit 3 (4uA)

◇ In the case of high luminance, Sampled Level and Control Unit may be selected to high. According to the specific picture, select the relevant conditions.

◇ Each color is controlled separately.
For Red, 1st/2nd parameter is used.
For Green, 3rd/4th parameter is used.
For Blue, 5th/6th parameter is used.

4. 2. Set XTALK Enable (0x32h)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
XTALK_EN	W	L			3			2			
Parameter	W	H			–	–	–	M2	M1	M0	00h

M[2 : 0]	Mode Set
000	XTALK Disable
001	Mode 1 Enable
010	Mode 2 Enable
011	Mode 1/2 Both Enable
100	Mode 3 Enable
101	Mode 1/3 Both Enable
110	Mode 2/3 Both Enable
111	Mode 1/2/3 All Enable

4. 3. Dot X-talk Ref. Setting (0x33h)

INSTRUCTION	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
Xtalk-Ref	W	L			3		3				
REF00	W	H			-	-	-	I8	I7	I6	07h
-	W	H			I5	I4	I3	I2	I1	I0	3Fh
REF01	W	H			-	-	-	I8	I7	I6	07h
-	W	H			I5	I4	I3	I2	I1	I0	3Fh
REF02	W	H			-	-	-	I8	I7	I6	07h
-	W	H			I5	I4	I3	I2	I1	I0	3Fh
REF03	W	H			-	-	-	I8	I7	I6	07h
-	W	H			I5	I4	I3	I2	I1	I0	3Fh
⋮											
REF45	W	H			-	-	-	I8	I7	I6	07h
-	W	H			I5	I4	I3	I2	I1	I0	3Fh
REF46	W	H			-	-	-	I8	I7	I6	07h
-	W	H			I5	I4	I3	I2	I1	I0	3Fh
REF47	W	H			-	-	-	I8	I7	I6	07h
-	W	H			I5	I4	I3	I2	I1	I0	3Fh
⋮											
REF92	W	H			-	-	-	I8	I7	I6	07h
-	W	H			I5	I4	I3	I2	I1	I0	3Fh
REF93	W	H			-	-	-	I8	I7	I6	07h
-	W	H			I5	I4	I3	I2	I1	I0	3Fh
REF94	W	H			-	-	-	I8	I7	I6	07h
-	W	H			I5	I4	I3	I2	I1	I0	3Fh
REF95	W	H			-	-	-	I8	I7	I6	07h
-	W	H			I5	I4	I3	I2	I1	I0	3Fh

Guide : Frame Frequency Table

Frame Frequency(Hz) = 1 / [(1/Fosc)*(Pcw+Ppw+Pdw+256) * Scan_N]

◆ Example :Frame Frequency = 90Hz

Pcw	Ppw	Pdw	Frame Frequency (Spec. Value)	Osc. Frequency(Fosc) (Designed Value)	Frame Frequency (Expected Value)	ETC
16	10	1	90Hz		4.08MHz	*1)
8	1	0	-			
8	2	0	-			
10	7	5	-			

*1) Conditions (Default)
Pre-Charge_Width(Pcw) = 8 (16 Dclk)
Peak-Pulse_Width(Ppw) = A (10 Dclk)
Peak_Pulse_Delay(Pdw) = 1 (1 Dclk)
Scan Nember(Scan_N) = 160

* Command Register

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
01h	SOFTRES	–	–	–	–	–	–	–	–	–
02h	DDISPON/OFF	–	–	–	–	–	–	–	P0	00h
03h	DSTBYON/OFF	–	–	–	–	–	–	–	P0	01h
04h	DFRAME	–	–	–	D4	D3	D2	D1	D0	02h
05h	WriteDirection	–	–	–	–	D3	D2	D1	D0	00h
06h	ScanDirection	–	–	–	–	–	–	–	P0	00h
07h	DispSize	–	–	–	–	–	FX6	FX5	FX4	00h
		–	–	–	–	FX3	FX2	FX1	FX0	00h
		–	–	–	–	–	TX6	TX5	TX4	07h
		–	–	–	–	TX3	TX2	TX1	TX0	0Fh
		–	–	–	–	FY7	FY6	FY5	FY4	00h
		–	–	–	–	FY3	FY2	FY1	FY0	00h
		–	–	–	–	TY7	TY6	TY5	TY4	09h
		–	–	–	–	TY3	TY2	TY1	TY0	0Fh
08h	IF Bus Sel	–	–	–	–	–	–	P1	P0	00h
09h	Data_Masking	–	–	–	RV	–	R	G	B	07h
0Ah	MBOXSize	–	–	–	–	–	XS6	XS5	XD4	00h
		–	–	–	–	XS3	XS2	XS1	XS0	00h
		–	–	–	–	–	XE6	XE5	XE4	07h
		–	–	–	–	XE3	XE2	XE1	XE0	0Fh
		–	–	–	–	YS7	YS6	YS5	YD4	00h
		–	–	–	–	YS3	YS2	YS1	YS0	00h
		–	–	–	–	YE7	YE6	YE5	YE4	09h
		–	–	–	–	YE3	YE2	YE1	YE0	0Fh
0Bh	DISPStart	–	–	–	–	–	DX6	DX5	DX4	00h
		–	–	–	–	DX3	DX2	DX1	DX0	00h
		–	–	–	–	DY7	DY6	DY5	DY4	00h
		–	–	–	–	DY3	DY2	DY1	DY0	00h
0Ch	DataWrite/Read	D7	D6	D5	D4	D3	D2	D1	D0	–
0Dh	READREG	D7	D6	D5	D4	D3	D2	D1	D0	–

* Command Register

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0Eh	DotCurrent	–	–	–	–	IR7	IR6	IR5	IR4	00h
		–	–	–	–	IR3	IR2	IR1	IR0	00h
		–	–	–	–	IG7	IG6	IG5	IG4	00h
		–	–	–	–	IG3	IG2	IG1	IG0	00h
		–	–	–	–	IB7	IB6	IB5	IB4	00h
		–	–	–	–	IB3	IB2	IB1	IB0	00h
0Fh	PeakCurrent	–	–	PR5	PR4	PR3	PR2	PR1	PR0	00h
		–	–	PG5	PG4	PG3	PG2	PG1	PG0	00h
		–	–	PB5	PB4	PB3	PB2	PB1	PB0	00h
1Ch	PreC_Width	–	–	D5	D4	D3	D2	D1	D0	08h
1Dh	PeakWidth	–	–	D5	D4	D3	D2	D1	D0	0Ah
		–	–	D5	D4	D3	D2	D1	D0	0Ah
		–	–	D5	D4	D3	D2	D1	D0	0Ah
1Eh	PeakDelay	–	–	–		D3	D2	D1	D0	01h
1Fh	Row_Scan	–	–	D5	D4	D3	–	D1	D0	00h
30h	VCC_R_SEL	–	–	–	D4	D3	D2	D1	D0	03h
35h	AGING_EN	–	–	–	–	–	–	–	P0	00h
3Ah	Gamma_Tune	–	–	–	–	I3	I2	I1	I0	00h
3Bh	Gamma_Init	–	–	–	–	–	–	–	–	–
3Dh	TESTCNT	–	–	D5	D4	D3	D2	D1	D0	00h
3Eh	TESTCNT0	–	–	D5	D4	D3	D2	D1	D0	–
36h	EOCompData	–	–	XR5	XR4	XR3	XR2	XR1	XR0	00h
		–	–	XG5	XG4	XG3	XG2	XG1	XG0	00h
		–	–	XB5	XB4	XB3	XB2	XB1	XB0	00h
37h	EOCtrl	–	–	D5	D4	D3	D2	D1	D0	00h
38h	EOGray_Reg	–	–	D5	D4	D3	D2	D1	D0	00h
3Fh	ColResSet	–	–	–	–	–	–	D1	–	00h

* Command Register

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
10h	S_SleepTimer					T6	T5	T4	T3	00h
						T2	T1	T0	–	00h
11h	S_SleepStart	–	–	–	–	–	–	–	P0	00h
12h	S_StepTimer					T6	T5	T4	T3	00h
						T2	T1	T0	–	00h
13h	S_StepUnit	–	–	–	–	–	–	S1	S0	00h
16h	S_Condition	–	–	–	–	U	D	R	L	00h
17h	S_Start/Stop	–	–	–	–	–	–	–	SS	00h
18h	S_Select	–	–	–	–	S3	S2	S1	S0	00h
31h	XTALK_Mode			RS5	RS4	RS3	RS2	RS1	RS0	00h
				–	–	RD3	RD2	RD1	RD0	00h
		–	–	GS5	GS4	GS3	GS2	GS1	GS0	00h
				–	–	GD3	GD2	GD1	GD0	00h
				BS5	BS4	BS3	BS2	BS1	BS0	00h
		–	–	–	–	BD3	BD2	BD1	BD0	00h
		–	–	–	–	BD3	BD2	BD1	BD0	00h
32h	XTALK_EN	–	–	–	–	–	M2	M1	M0	00h
33h	XTALK-Ref	–	–	–	–	–	I8	I7	I6	07h
		–	–	I5	I4	I3	I2	I1	I0	3Fh
		–	–	–	–	–	I8	I7	I6	07h
		–	–	I5	I4	I3	I2	I1	I0	3Fh
		–	–	–	–	–	I8	I7	I6	07h
		–	–	I5	I4	I3	I2	I1	I0	3Fh

◎ **Revision History**

REV.	Contents	Date
1.0	The First Version	2007. 06. 05
1.1	Modify a "1.8. Set Interface Bus Type (0x08h)" (page 35) Modify a "1.17. Set Peak Pulse Width (0x1Dh)" (page 43)	2007. 07. 19
1.2	Modify a "1.16. Set Pre-Charge Width (0x1Ch)" (page 42) Don't use a parameter "T[5:0]=00h" & "T[5:0]=01h" Modify a "1.17. Set Peak Pulse Width (0x1Dh)" (page 43) Don't use a parameter "W[5:0]=00h".	2007. 07. 26
1.3	Change a Device Name from "LD7230" to "LD7130" Modify a "2.7.Even_Odd Control Set (0x37Fh)" (page 47)	2007. 08. 08
1.4	Modify a "2.9.Column Port Current Resister - - (0x3Fh)" (page 50) Add a "Screen Saver Function". (page 51 ~53) Add a "Crosstalk Function". (page 54 ~55)	2007. 10. 12
1.5	Modify a "8. DC Characteristics" Changed a Cptp1, Carea1, Cchip1 (P19-20)	2008. 03. 07