GEC PLESSEY
SEMICONDUCTORS

SP973T8

30MHz 8-BIT FLASH ADC (TTL/CMOS OUTPUTS)

The SP973T8 is a wideband, full flash analog-to-digital converter that requires no preceding sample and hold. The device contains a full 8-bit D-type latch which ensures that the 8 TTL/CMOS outputs are accurately registered and have a good data valid time at high clock speeds.

Operating from a single +5 volt supply the device is capable of conversion rates well in excess of 30MHz and its wideband input allows signals with frequencies up to the Nyquist limit to be digitised with high accuracy. An internal bandgap voltage regulator gives low DC drift over a wide operating temperature range.

The SP973T8 is designed for applications where power consumption and package size is at a premium.

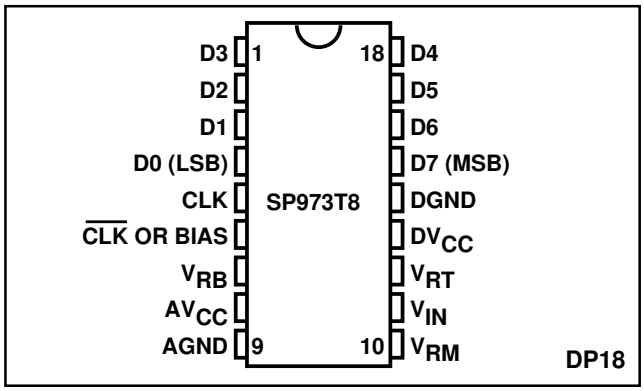


Fig.1 Pin connections - top view

FEATURES

- Flash Converter, No Sample and Hold Required
- Wideband Analog Input 70MHz, 3dB (Typ.)
- Low Power Consumption (600mW Typ.)
- Latched TTL/CMOS Compatible Outputs
- No Missing Codes - Guaranteed
- Designed for Wideband Operation
- Single 5V Supply
- Production Tested at 30MHz

ORDERING INFORMATION

SP973T8 C DP (Commercial - Plastic DIL package)

APPLICATIONS

- Studio Quality Video
- DBS Broadcast Video
- High Resolution TV
- Nucleonics
- Radar
- Computing

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	7V
Output Current	10mA
Input Voltage, V_{IN}	V_{CC}
Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C

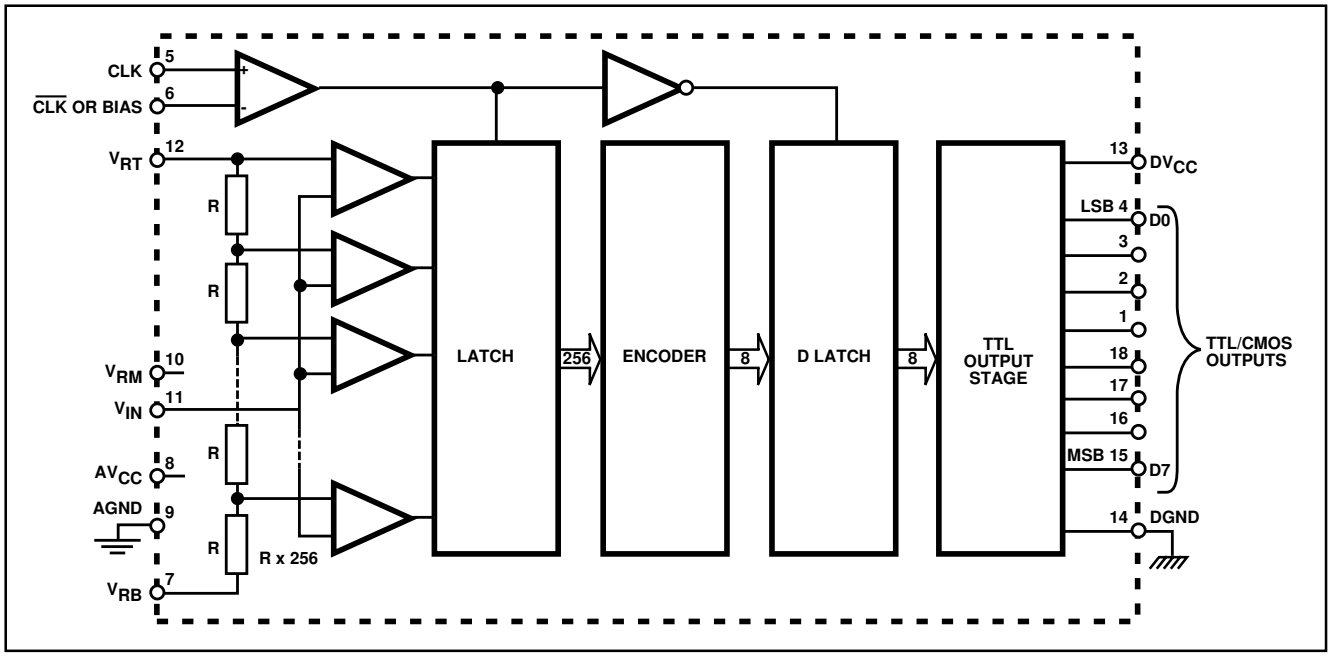


Fig.2 Internal block diagram

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):

T_{amb} = 25°C, V_{CC} = +5V ± 0.25V

Full temperature range = 0°C to +70°C

DC CHARACTERISTICS

Characteristic	Symbol	Temp.	Test level	Value			Units	Conditions
				Min.	Typ.	Max.		
Power Supply								
Supply current	I_{CC}	Full	4	100		140	mA	
		25	1	110	120	130	mA	
Power dissipation	P_D	Full	4	475		735	mW	
		25	1	520	600	680	mW	
Analog Input								
Input range	V_{IN}	Full	4	1.8		V_{CC}-0.7	V	
Input bias current	I_{IN}	25	1	150	390	1100	µA	$V_{IN} = V_{RT}$
3dB bandwidth	f_{3db}	25	4		70		MHz	
Input capacitance	C_{IN}	25	4		30		pF	
Reference Ladder								
Ladder resistance	R_D	25	1	325	440	550	Ω	
Ladder voltage (top)	V_{RT}	Full	4		4.3	V_{CC}-0.7	V	
Ladder voltage (bottom)	V_{RB}	Full	4	1.8	2.3		V	
Ladder offset (top)	V_{RT0}	25	5		-4		mV	
Ladder offset (bottom)	V_{RB0}	25	5		+3		mV	
Ladder temp. coeff.	R_{TC}	Full	5		1.5		Ω/°C	
Clock Input								
Logic '1' voltage	V_{IH}	Full	4	2.75	4.3	V_{CC}	V	A swing of 1V centred on the voltage applied to the CLK pin
Logic '1' current	I_{IH}	25	1			25	µA	
Logic '0' voltage	V_{IL}	Full	4	1.75	3.3	V_{CC}-1.0	V	
Logic '0' current	I_{IL}	25	1			2	µA	
Digital Outputs								
Logic '1' voltage	V_{OH}	Full	4	3.3			V	Into Standard LS TTL Load
		25	1	3.5	3.8		V	
Logic '0' voltage	V_{OL}	Full	4			0.4	V	
		25	1		0.1	0.4	V	
Static performance								
Differential non-linearity	DNL	Full	4			±1	LSB	
		25	4			±0.5	LSB	
Integral non-linearity	INL	Full	4			±1	LSB	
		25	4			±1	LSB	

AC CHARACTERISTICS (Refer to Fig.7)

Characteristic	Symbol	Temp.	Test level	Value			Units	Conditions
				Min.	Typ.	Max.		
Clock min. high	t_{PW1}	25	4	10			ns	
Clock min. low	t_{PW0}	25	4	10			ns	
Max. conversion rate		Full	4	30	50		MHz	A_{IN} = 15MHz at FS
Aperture delay	t_{AD}	25	5		3		ns	
Output data delay	t_D	25	4		7		ns	
Output rise time	t_R	25	4		6		ns	
output fall time	t_F	25	4		8		ns	
Dynamic Performance								With F_{CLK} = 30MHz
Differential non-linearity	DNL	25	1	-0.85	±0.5	+1	LSB	$A_{IN\ MAX}$ = 10MHz at FS
Integral non-linearity	INL	25	1		±1	±2	LSB	$A_{IN\ MAX}$ = 10MHz at FS
S/N ratio	SNR	25	1	40.9	44.5		dBc	$A_{IN\ MAX}$ = 1MHz at FS
			4		44.1		dBc	$A_{IN\ MAX}$ = 5MHz at FS
			4		43.3		dBc	$A_{IN\ MAX}$ = 10MHz at FS
Effective No. of bits	ENOB	25	1	6.5	7.1		bits	$A_{IN\ MAX}$ = 1MHz at FS
			4		7.0		bits	$A_{IN\ MAX}$ = 5MHz at FS
			4		6.9		bits	$A_{IN\ MAX}$ = 10MHz at FS
Bit Error Rate	BER	25	4		1 in 10^9			

ELECTRICAL CHARACTERISTICS DEFINITIONS

Analog Bandwidth

The analog input frequency at which the spectral power of the fundamental frequency, as determined by Fast Fourier Transform analysis is 3dB down on the DC level.

Aperture Delay

The delay between the falling edge of the CLOCK signal and the instant at which the analog input is sampled.

Bit Error Rate (BER)

The number of spurious code errors produced for any given input sinewave frequency. In this case it is the number of codes occuring outside the histogram cusp for a $^3/_4$ F.S. sinewave.

Differential Non-Linearity (DNL)

The deviation of any code width from an ideal 1LSB step.

Effective Number of Bits (ENOB)

This is a measure of the dynamic performance and is calculated from the following expression.

$$ENOB = \frac{SNR-1.76}{6.02}$$

SNR is the signal-to-noise ratio, in decibels, at the test frequency.

Integral Non-Linearity (INL)

The deviation of the centre of each code from a reference line which has been determined by a least squares curve fit.

Output Data Delay

The delay between the 50% point of the falling edge of the clock signal and the 50% point of any data output change.

Reference Ladder Offset

The voltage error at the ends of the resistor chain caused by the lead frame and bond wire.

Signal-to-Noise Ratio (SNR)

The ratio of the RMS signal amplitude to the RMS value of 'noise' which is defined as the sum of all other spectral components including harmonics but excluding DC with a full scale analog input signal.

Test Levels

Level 1 - 100% production tested
Level 2 - 100% production tested at 25°C and sample tested at specified temperatures
Level 3 - Sample tested only
Level 4 - Parameter is guaranteed by design and characteristics testing
Level 5 - Parameter is a typical value only

PIN DESCRIPTIONS

Pin No.	Function	Description
1, 2, 3, 4	D3, D2, D1, D0	Output data bits 3, 2, 1, 0
5	CLK	Clock input pin
6	$\overline{CLK}$	Clock threshold level pin
7	V_{RB}	Bottom of reference resistor chain
8	AV_{CC}	5 Volt power to all circuitry except the TTL output
9	AGND	
10	V_{RM}	Middle of reference resistor chain
11	V_{IN}	Analog input voltage pin
12	V_{RT}	Top of reference resistor chain
13	DV_{CC}	5 Volt power supply to the TTL output stage
14	DGND	
15	D7	Most significant bit (output data bit 7)
16, 17, 18	D6, D5, D4	Output data bits 6, 5, 4

RECOMMENDED OPERATING CONDITIONS

Supply Voltage V_{CC}	+5.0V
Reference V_{RT}	+4.3V
Reference V_{RB}	+2.3V
AV_{CC} to DV_{CC}	0mV
AGND to DGND	0mV
Analog Input V_{IN}	2 Vp-p max

THERMAL CHARACTERISTICS

	DP	
Thermal resistance, chip-to-case θ_{jc}	20	°C/W
Thermal resistance, chip-to-ambient θ_{jA}	75	°C/W

APPLICATION NOTES

Analog Input Pin (Fig.3)

The analog input of the SP973T8 is connected to 256 comparators which have a combined capacitance of about 30pF. The sample/latch operation of the comparators causes the input capacitance to vary slightly as the comparator input transistors turn on/off. For this reason the input driver circuit should provide a low impedance signal to keep the harmonic distortion levels of the driver to a minimum.

The maximum amplitude of the analog input is defined by the setting of the two reference voltages V_{RT} and V_{RB}. Optimum performance will be obtained with the input signal biased midway between V_{RT} and V_{RB} with a peak to peak amplitude of V_{RT}-V_{RB}. The SP973T8 has excellent overload tracking of input signals with amplitudes greater than V_{RT}-V_{RB}, and will not be damaged if the absolute maximum ratings are adhered to.

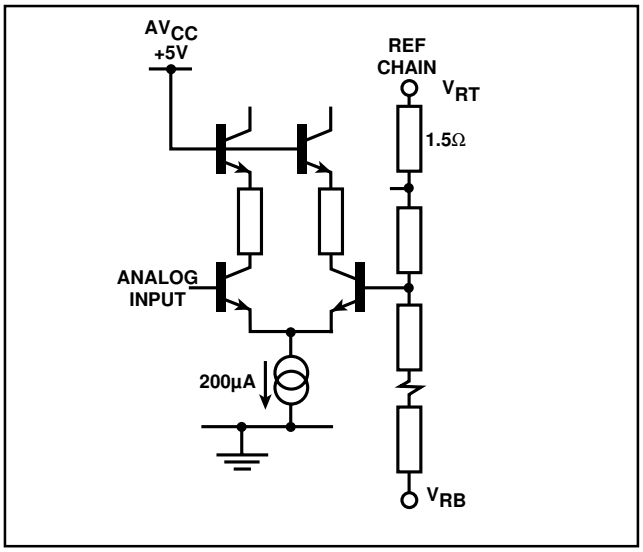


Fig.3 One of 255 analog inputs connected to pin 11

Voltage Reference Pins (Fig.4)

The SP973T8 converts analog signals in the range V_{RB}<V_{IN}<V_{RT} into digital format, where V_{RB} produces code 0 and V_{RT} produces code 255. Between the pins V_{RT} and V_{RB} are a series of 256 resistors forming a reference chain with a total resistance of 425Ω (typically). The centre point of the reference chain is also connected to an external pin named V_{RM} by which it is possible to provide precision trimming of the integral linearity of the device.

The maximum value of V_{RT} is V_{CC}-0.7 volts since values above this figure will start to saturate the comparator, resulting in noticeable distortion. Optimum performance from a +5 Volt power supply is obtained with V_{RT}<+4.3V and V_{RB} a further 2 volts below V_{RT}. In addition the V_{RT}, V_{RB} and V_{RM} pins should be decoupled to ground close to the device pins using good quality 10nf capacitors. A simple method for providing the reference voltages is shown in Fig.4, and further information may be found in applications note AN72. With a reference ladder voltage of less than 2V the reduced LSB size causes a larger differential linearity error. Operation of the device below 1.5V may therefore cause missing codes.

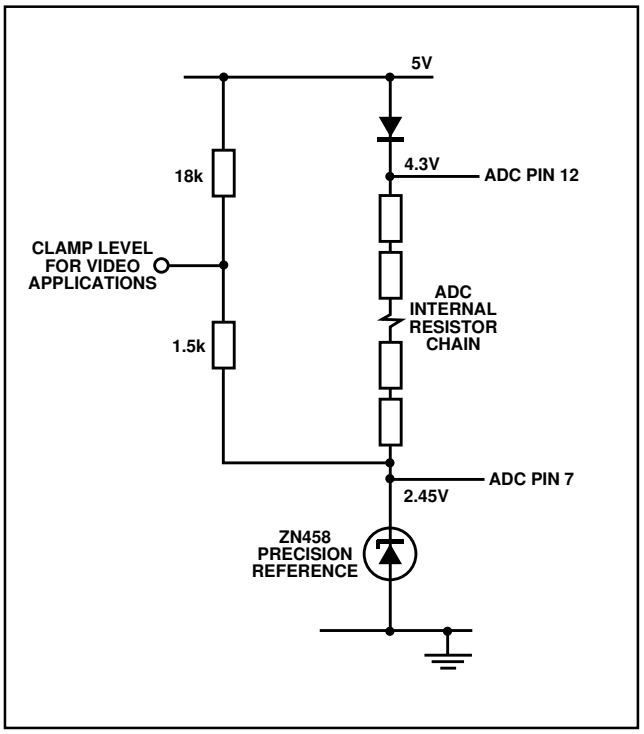
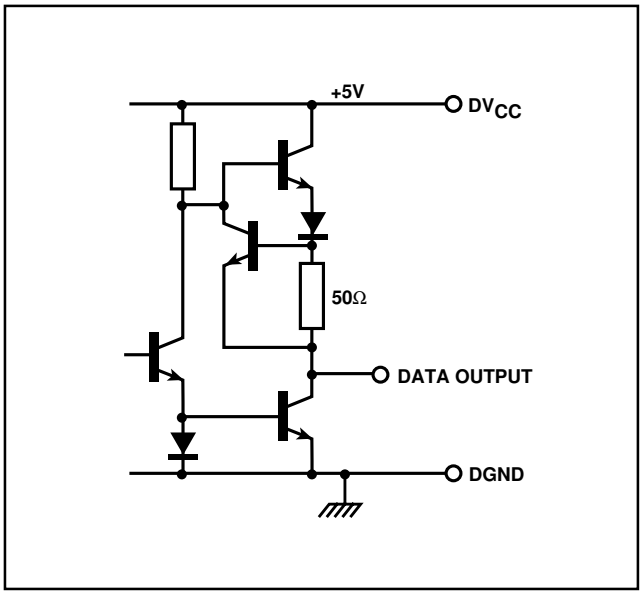


Fig.4 Simple reference voltage generation

TTL/CMOS Outputs (Fig.5)

The data output levels of the SP973T8 are TTL/CMOS compatible and switch from 0V to +4V. The output circuit is capable of operation at clock frequencies in excess of 60MHz when driving into a standard LSTTL load.



Fig,5 TTL output stage

Clock Input (Fig.6)

The SP973T8 will operate at clock frequencies up to and above 30MHz. The clock input has been designed to accept a 1Vpp signal, in either differential or single-ended mode, between the $V_{IH(MAX)}$ and $V_{IL(MIN)}$ levels indicated in the electrical specification. At $V_{IH(MAX)}$ or $V_{IL(MIN)}$ the CLK input will sink 800µA or source 3.2mA of current, respectively. (See Fig.6).

When used in single-ended operation, CLK may be decoupled to ground so that this input will then self-bias at approximately 1.2V below the supply V_{CC}. It may then be used to bias the CLK input, through a termination resistor, for AC-coupled applications as shown in Fig.8.

Alternatively a TTL level clock may be used by inserting an appropriate value resistor in series with the coupling capacitor.

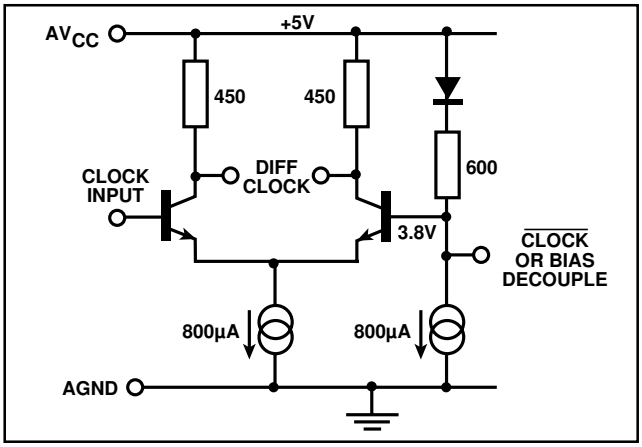


Fig.6 Clock input stage

TIMING (Fig.7)

The analog input is sampled by the SP973T8 approximately 3ns (t_{AD}) after the falling edge of the clock. Due to the pipeline operation of the device, a further one clock cycle is required to produce the output data. As shown in Fig.7, the output has a good data valid time, enabling the data to be latched at both the rising and falling edges of the clock.

However, for clock frequencies above 25MHz the clock-to-output delay time may lead to an inadequate data set up time relative to the rising clock edge and it is therefore recommended that the output data is latched on the falling clock edge.

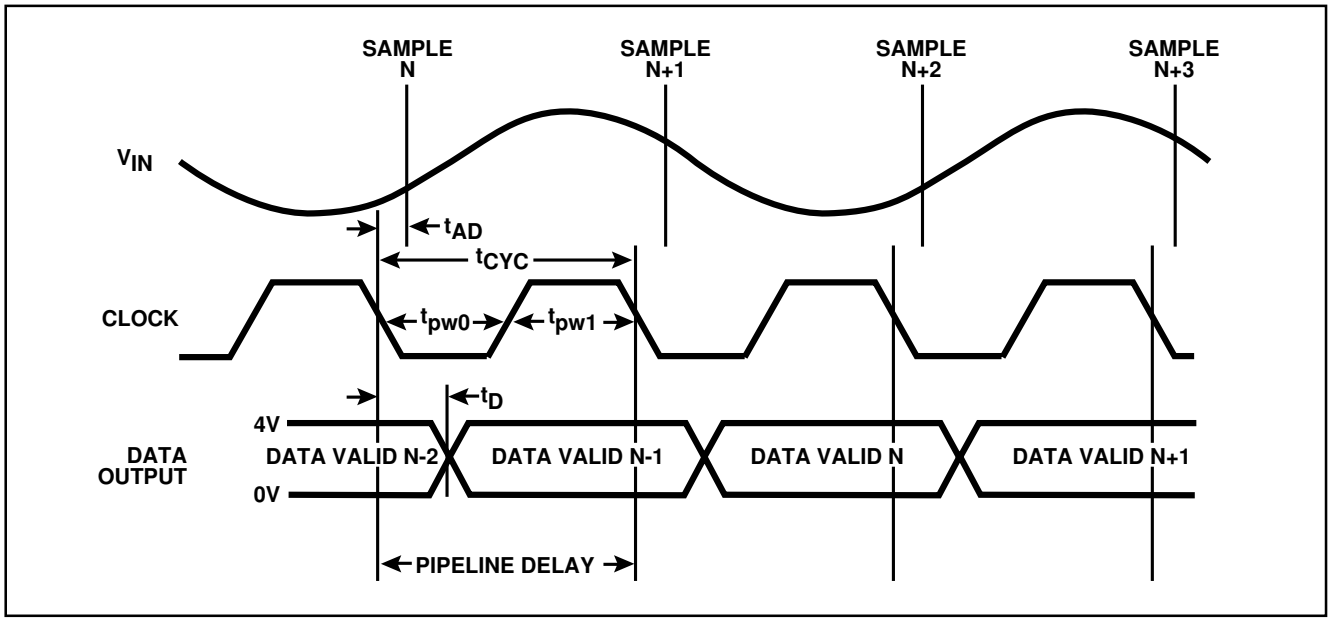


Fig.7 Timing diagram

Circuit Board Construction (Fig.8)

Excellent performance can be obtained from this ADC using only one solid ground plan for both analog and digital signals.

With all flash ADCs it is important to restrict digital crosstalk into the input, not only within the wanted signal bandwidth but also at frequencies between Nyquist and clock, as such signals will be aliased down into the wanted signal bandwidth.

We can give the designer two useful suggestions to reduce the above. First, due to the on-chip clock regeneration circuit, a low level clock can be fed to the ADC 1V p-p is recommended. The second suggestion is the addition of a small bead inductor in series with and close to the device analog input.

Supply line decoupling is very important when dealing with a mix of analog and digital signals as they can provide a source of digital feedback from the digital output currents. It is wise, therefore, to decouple the SP973T8 close to the device supply pins with good quality, high frequency, low inductance capacitors.

Due to the high clock rates involved, long clock lines to the device should be avoided to reduce the noise pick up.

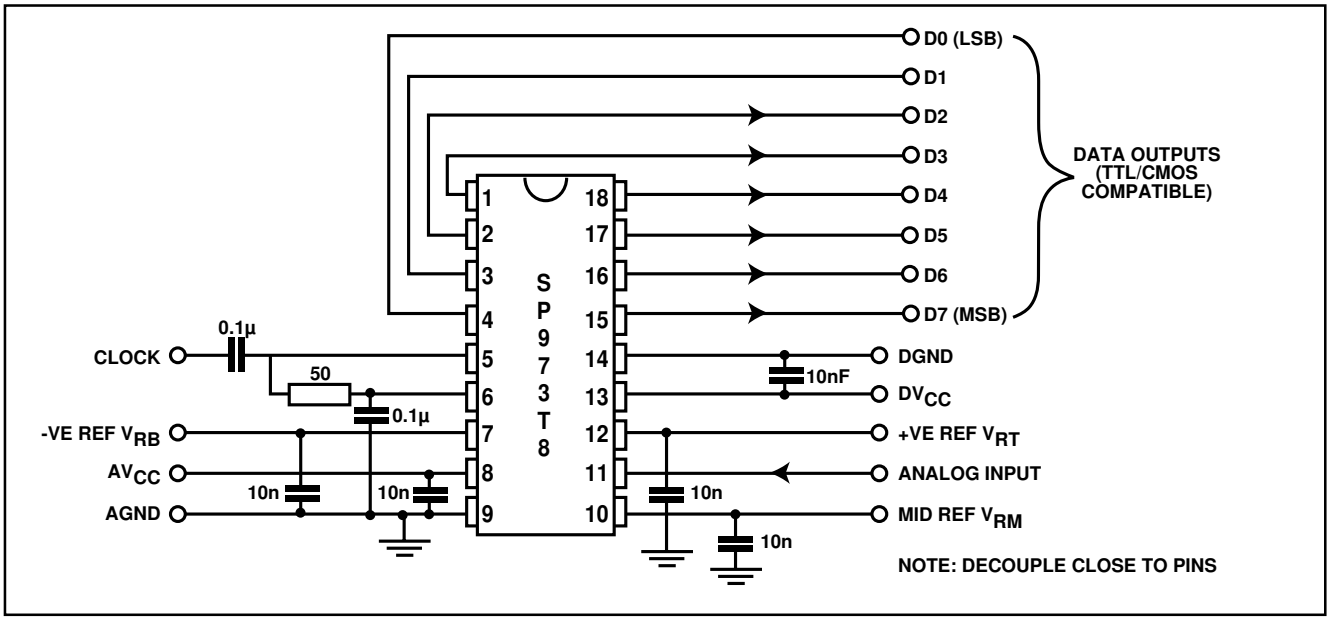


Fig.8 Test/application circuit

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