GEC PLESSEY

SEMICONDUCTORS

PRELIMINARY INFORMATION

3022-1.0

T-75-49

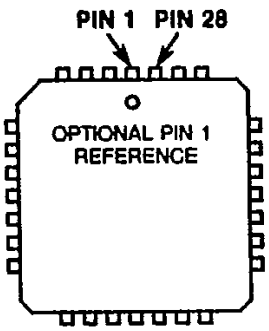
SP9930

FDDI CLOCK RECOVERY AND DE-SERIALISING RECEIVER

FDDI (Fibre Distributed Data Interface) is a standard defined by ANSI (American National Standard Institute) for a token passing ring network operating at a user rate of 100MB/s. The SP9930 receiver is one of two devices which service the 4B/5B codec to NRZI interface.

Only two external components are required to provide RC phase lock loop filtering. When no data is present at the input the internal VCO is locked to 5 times the local symbol clock. This arrangement gives an accurate 125MHz free running clock and a very short lock on time of less than 1 microsecond.

When data is input the device changes mode and locks to the data. Following clock recovery the data is converted from NRZI to NRZ before the parallel to serial conversion.



HG28

Pin	Function	Pin	Function	Pin	Function
1	RDATA D_1	11	FLTR	21	SDI+
2	RDATA D_2	12	AV_{EE}	22	SDI
3	RDATA D_3	13	ERROR	23	SDO
4	RDATA D_4	14	AV_{CC}	24	LSCLK
5	TGND	15	LTXD	25	MODE
6	DGND	16	LPBCK	26	RBYCLK
7	SRDATA	17	TEST	27	DV_{CC}
8	EGND	18	RCVD-	28	RDATA D_0
9	RBCLK	19	RCVD+		
10	AGND	20	DV_{EE}		

Fig.1 Pin connections - top view

FEATURES

- FDDI Standard Compatible
- 125MHz Clock Guaranteed (Typ. 170MHz at 25°C)
- Receive bit Clock Jitter <2.3ns
- Lock on time <1.0μs
- +5.0V/ -5.2V Supplies
- Very Low External Component Requirement

APPLICATIONS

- FDDI Communication System

ORDERING INFORMATION

SP9930 C HG (Commercial - Quad Cerpac package)

ASSOCIATED PRODUCTS

SP9970 FDDI transmitter
SP9944E 200MBit/s data regenerator
SL9901 50MHz transimpedance amplifier
SP9921 50MBit/s Manchester biphase-mark Decoder
SP9960 50MBit/s Manchester biphase-mark Encoder

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	+5.5V
Supply voltage V_{EE}	-5.75V
Operating temperature	0°C to +70°C
Maximum junction temperature	+125°C
Storage temperature	-55°C to +150°C

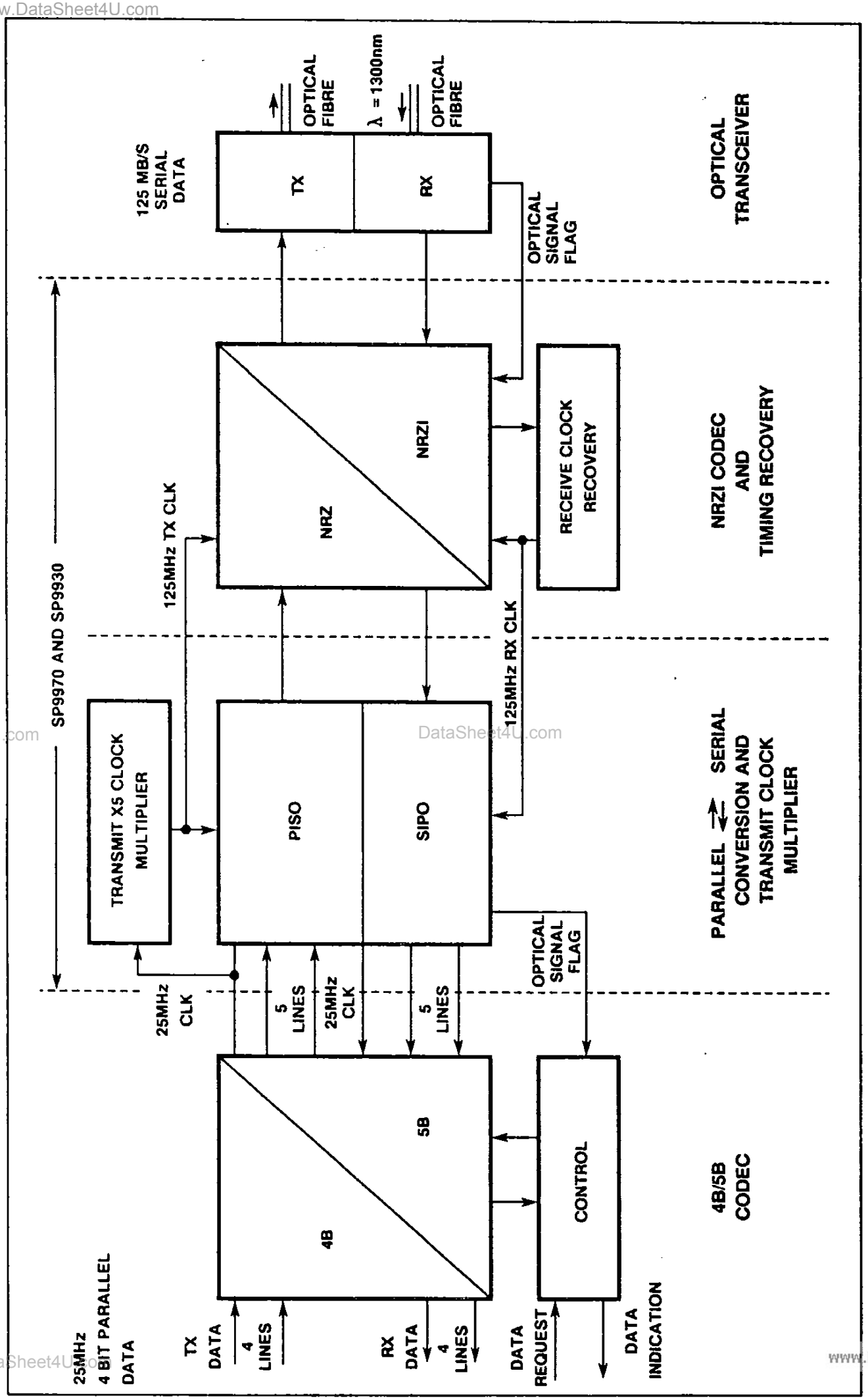


Fig.2 FDDI physical layer (block diagram)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
T_{AMB} = +25°C, V_{CC} = +5V ±10%, V_{EE} = -5.25V ±10%
Full temperature range = 0°C to +70°C

DC CHARACTERISTICS

Characteristic	Symbol	Temp. (°C)	Test level	Value			Units	Conditions
				Min	Typ	Max		
Supply current	I_{CC}	Full	1		25	50	mA	
	I_{EE}	Full	1		150	200	mA	
TTL Inputs								
Logic '1' current	I_{IH}	Full	1		3	20	µA	See Note 1
Logic TEST pin		Full	1		120	130	µA	See Note 1
Logic '0' current	I_{IL}	Full	1			-600	µA	See Note 1
ECL Inputs								
Logic '1' current	I_{IH}	Full	1			200	µA	See Note 3
Logic '0' current	I_{IL}	Full	1	-0.01		300	µA	See Note 4
TTL Outputs								
Logic '1' voltage	V_{OH}	Full	1	2.4	2.9		V	I_{OH} = -400µA
Logic '0' voltage	V_{OL}	Full	1		0.35	0.525	V	I_{OL} = 4mA
Short circuit current	I_{OS}	Full	5	-3.0		-40	mA	V_O = 0V
Output current								
ECL Outputs								
Logic '1' voltage	V_{OH}	0	4	-1.17	-0.9	-0.84	V	RL = 100Ω to -2V
		+25	1	-1.13	-0.85	-0.8	V	RL = 100Ω to -2V
		+70	4	-1.07	-0.8	-0.72	V	RL = 100Ω to -2V
Logic '0' voltage	V_{OL}	0	4	-1.95	-1.7	-1.48	V	RL = 100Ω to -2V
		+25	1	-1.95	-1.7	-1.48	V	RL = 100Ω to -2V
		+70	4	-1.95	-1.7	-1.45	V	RL = 100Ω to -2V

NOTES
1. TTL input under test set to 2V all other TTL inputs set to 0.8V
2. TTL input under test set to 0.8V all other TTL inputs set to 2V
3. ECL input under test set to-0.81V all other ECL inputs set to -1.85V
4. ECL input under test set to -1.85V all other ECL inputs set to -0.81V

TEST LEVELS
Level 1 - 100% production tested
Level 4 - Parameter guaranteed by design and characteristics testing
Level 5 - Parameter is a typical vaue only

AC CHARACTERISTICS

Guaranteed by design and AC characteristics testing.
Characteristics assume 125M/bit operation

CONDS

T-75-49

Characteristic	Symbol	Temp. (°C)	Value			Units	Conditions
			Min	Typ	Max		
ECL Outputs							
Rise times 20%-80%	t_R	0		2	2.5	ns	RL = 100Ω to -2V
		25		2.7	3	ns	RL = 100Ω to -2V
		70		3	5	ns	RL = 100Ω to -2V
Fall times 20%-80%	t_F	0		2	2.5	ns	RL = 100Ω to -2V
		25		2.7	3	ns	RL = 100Ω to -2V
		70		3	5	ns	RL = 100Ω to -2V
TTL Outputs							
Rise times 20%-80%	t_R	0		5	12	ns	
		25		6	16	ns	
		70		7	19	ns	
Fall times 10%-90%	t_F	0		6	12	ns	
		25		6	12	ns	
		70		6	13	ns	
RBCLK							
Duty cycle distortion	D_{CD}	Full	-2.5	-2	+2.5	ns	
Jitter p-p	t_{CJ}	Full	-0.5	0.2	+0.5	ns	LSCLK to RBCLK

ELECTRICAL CHARACTERISTICS DEFINITIONS

Duty cycle distortion (DCD)

The maximum difference between the high time of this signal and the low time.

Jitter (tcj)

The maximum deviation of the rising edge of LSCLK to the rising edge of RBCLK.

CONTROL INPUTS (TTL)				FUNCTION	SRDATA (ECL)	RDATAn (TTL)	SDO (TTL)	MODE (TTL)
SDI (ECL)		LPBACK (TTL)	TEST (TTL)					
+	-							
Hi	Lo	1	0	Normal operation	RCVD data	Decoded data from RCVD	1	1 = locked 0 = unlocked
Lo	Hi	1	0	Fibre optic receive disabled	Lo	0	0 on next LSCLK ↑edge	0
X	X	0	0	Loopback mode	LPBCK data	Decoded data from LPBCK	1	1 = locked 0 = unlocked
X	X	X	X	Test mode for manufacturer's use only	X	1	X	X

Table 1 Receiver function table

INTRODUCTION TO FDDI SYSTEMS

FDDI (Fibre Distributed Data Interface) is a standard defined by ANSI (American National Standard Institute) for a token passing ring network operating at a user rate of 100MB/s. The standard consists of 4 documents;

1. Physical Media Dependant (PMD)
2. Physical Layer Protocol (PHY)
3. Media Access Control (MAC)
4. Station Management (SMT)

These documents correspond closely with the OSI seven layer model, PMD and PHY are sublayers of the OSI physical layer. The MAC document implements some of the OSI Data link layer. Overall control of the PHY and MAC functions is provided by the SMT.

Technical Overview (The Physical Layer)

Fig. 2 shows a block diagram of the Physical Layer, the first section is the 4B/5B codec, here the data is in symbols, four bits wide at a rate of 25MB/S. Each four bit code received, is converted into a 5 bit code according to a pre-defined table. This extra bit is added to prevent long runs of zeros, it also allows the addition of signalling words by the control section. A circuit incorporating the codec function is not yet available but it could be implemented in semi-custom CMOS, such as CLA60K series.

After conversion to a 5-bit word the data undergoes a parallel to serial conversion, this multiplies the transmission rate up to 125MB/s. In order to clock the data out at this rate the clock needs to be multiplied five times up to 125MHz, this is achieved with a phase locked loop in this chip set. Before transmission over the fibre the data is converted to a code called NRZI, in this code a '1' is represented by a transition and '0' as no transition. This coding maximises transistions without increasing the bandwidth of the signals, and when combined with the 4B/5B coding this system minimises the DC content of the signal. On the receive side the transitions within the NRZI code are used to recover the 125MHz clock.

FDDI specifies a fibre optic transmission medium of 62.5 µm core multimode fibre (this is the recommended core size; 50, 85 and 100µm cored fibres are allowed alternatives), a 1300nm LED source, and a maximum distance between nodes of 2km.

Up to 500 nodes and a total fibre length of 200km are supported by FDDI. A distance of up to 2km is supported by the present multimode interface, and work is in progress to modify the standard to allow a single mode interface for larger distances.

A further modified network called FDDI-II is proposed that uses 6MB/s time slots for isochronous data such as voice, low rate video and point to point data links. FDDI-II uses the same physical layer as FDDI-I.

THE FDDI CHIPS

At present FDDI chips are available which support the 4B/5B to NRZI interface, this circuitry is contained in two 28 pin devices, a transmitter chip and a receiver chip Both chips operate on a supply of +5V/-5.2V. TTL and differential ECL interfaces are used for the 25MB/s and 125MB/s signals respectively, all control and alarm signals are TTL levels.

The ECL interfaces are 10KH compatible. Although the devices are designed to operate at a line rate of 125MB/s, performance up to 170MB/s can be expected at 25°C. Both transmitter and receiver have a loopback mode, serial data from the local transmitter is looped back to the local receiver. The devices are manufactured using a high speed bipolar process.

The SP9930 Receiver

The receiver (device type SP9930) is powered from a +5V and -5.2V supply with currents of 40mA and 170mA respectively. Only two external components are required, a capacitor and a resistor, these provide the phase lock loop filtering.

A block diagram of the receiver is shown in Fig. 3. the serial data is input from the fibre optic receiver through a differential ECL input stage. When no data is present at the input, indicated by a low on Signal Detect Input (SDI), the internal VCO is locked to five times the local symbol clock (LSCLK). This arrangement gives an accurate 125MHz free running clock and a very short lock-on time of $<1\mu s$. When the SDI pin is high the device changes mode and locks to the received data (RCVD), the MODE pin is used to indicate which mode the device is operating in.

While the VCO is locked to the RCVD its frequency is continuously monitored, if the frequency error exceeds ±1% the phase locked loop (PLL) changes back to the LSCLK mode.

Once a frequency accuracy of ±0.5%, relative to the LSCLK is achieved the PLL returns to the RCVD mode, provided SDI is high. Jitter on the receive bit clock should be <2.27ns pk-pk provided the RCVD jitter is <4.2ns pk-pk. External components are used to select the time constant of the PLL, and the error voltage from the comparator is available at an external pin (ERROR) through a buffer.

Following clock recovery the data is converted from NRZI to NRZ before the parallel to serial conversion. Parallel data is presented as five bit wide symbols at the RDATA outputs (TTL levels). The data bits transmitted will not necessarily appear on the same pins as they were transmitted, this is because the framing is performed in the 4B/5B decoder. A 25MHz Receive Byte Clock (RBYCLK) is provided, to allow data to be clocked into the following word alignment and decoding circuits.

A Signal Detect Output (SDO) is provided, this directly reflects the SDI input, except that it is clocked out on the next LSCLK positive edge after SDI changes.

PHASE LOCKED LOOP CHARACTERISTICS

The receiver PLL is more complex than the transmitter as it is required to lock on to varying data patterns. Under worst conditions (Master Line State) 1 transistion occurs every 10 bits. However the device will still recover clock with only 1 transition in every 16 timeslots with the filter components shown in fig 4.

Unlike the transmitter the receiver PLL operates in two modes. In mode 0 the VCO is locked to five times the LSCLK input and in mode 1 the VCO is locked to the incoming data. As shown in table 1 the actual operating mode is indicated by the logic level at the mode output pin. While in mode 1 a frequency counter monitors the VCO frequency to check that it is five times the LSCLK frequency; if the error is more than ± 1% the PLL defaults back to mode 0 and this indicates that lock has been lost. Before switching back to mode 1 the VCO must achieve an accuracy of ± 0.5% when compared to five times the LSCLK input.

Note that the measurement period is 40 cycles of the LSCLK so that at 25MHz at least 1.6µs must be allowed before the PLL will switch back to mode 1.

Whenever the SDI flag is raised the PLL will automatically switch to mode 0 as this indicates there is no valid input signal. Conversely when the 'LP BACK' signal goes 'low' the device will default to mode '1', this allows loopback to be used regardless of the optical input signal condition.

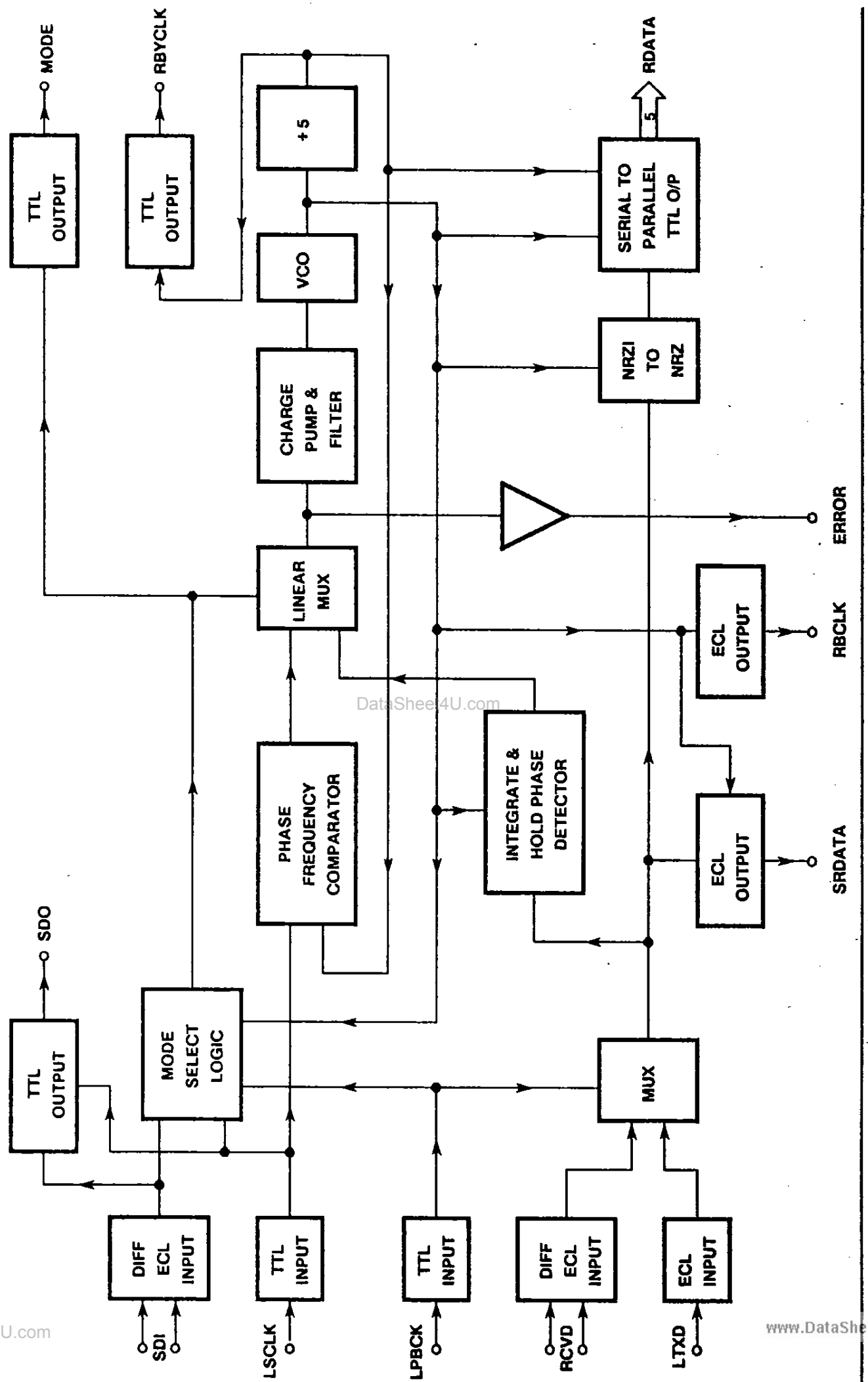


Fig.3 SP9930 receiver block diagram

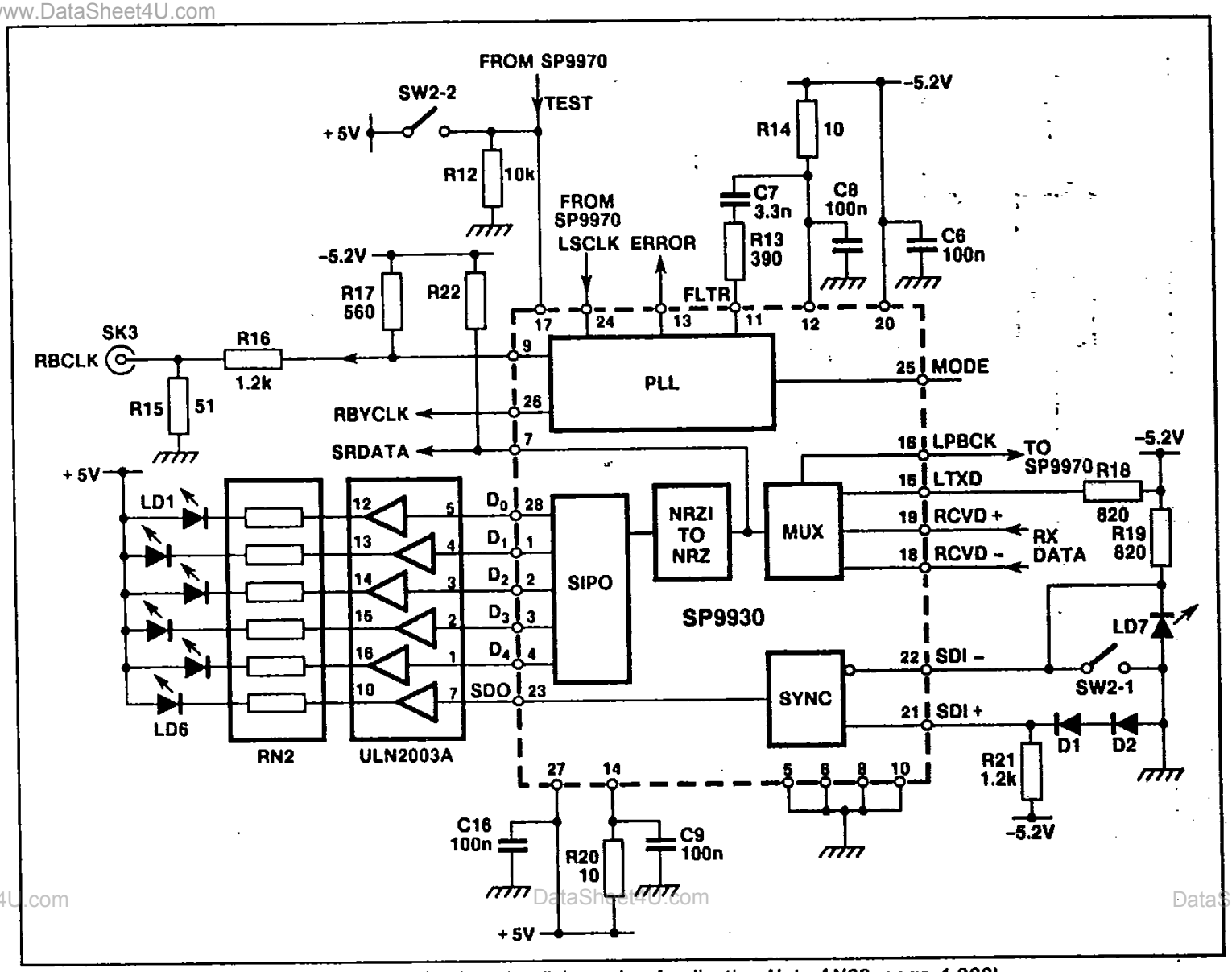


Fig.4 SP9930 application circuit (see also Application Note AN66, page 4-233)

Internally the PLL consists of a patented integrate and hold phase comparator driving a charge pump with an internal reservoir capacitor. The reservoir capacitor smoothes the current pulses from the charge pump and provides a relatively noise free voltage to control the VCO. A small resistor in series with the capacitor allows small instantaneous changes in frequency, increasing this resistor improves the capture time but adversely affects the jitter. In practice using the values shown in Fig. 4 will produce a capture time of $< 1\mu s$ and very low jitter.

Fig. 5. shows the VCO frequency against the control voltage at the FLTR pin; the control voltage goes positive for the higher frequencies. As shown by the graph the device has a wide range of operation from 60 to 175MHz. If the device is used at a non FDDI frequency the LSCLK must always be a fifth of the operating frequency (±0.25%), otherwise the frequency comparator will switch into mode 0. The reliability of operation at the frequency extremes is not guaranteed, jitter does increase at the low frequencies but at the higher frequencies it is minimal.

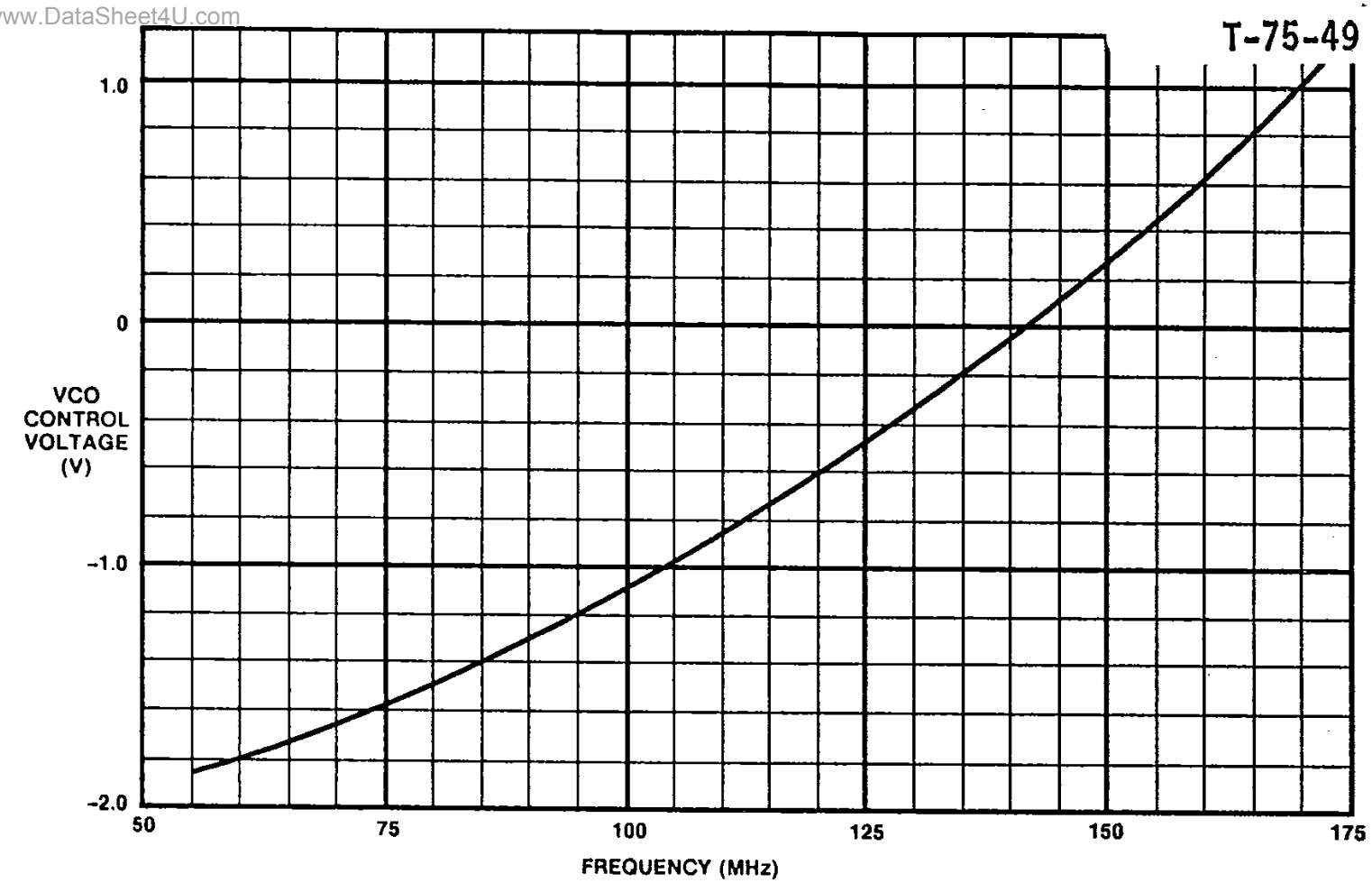


Fig.5 Receiver VCO characteristic (typical)

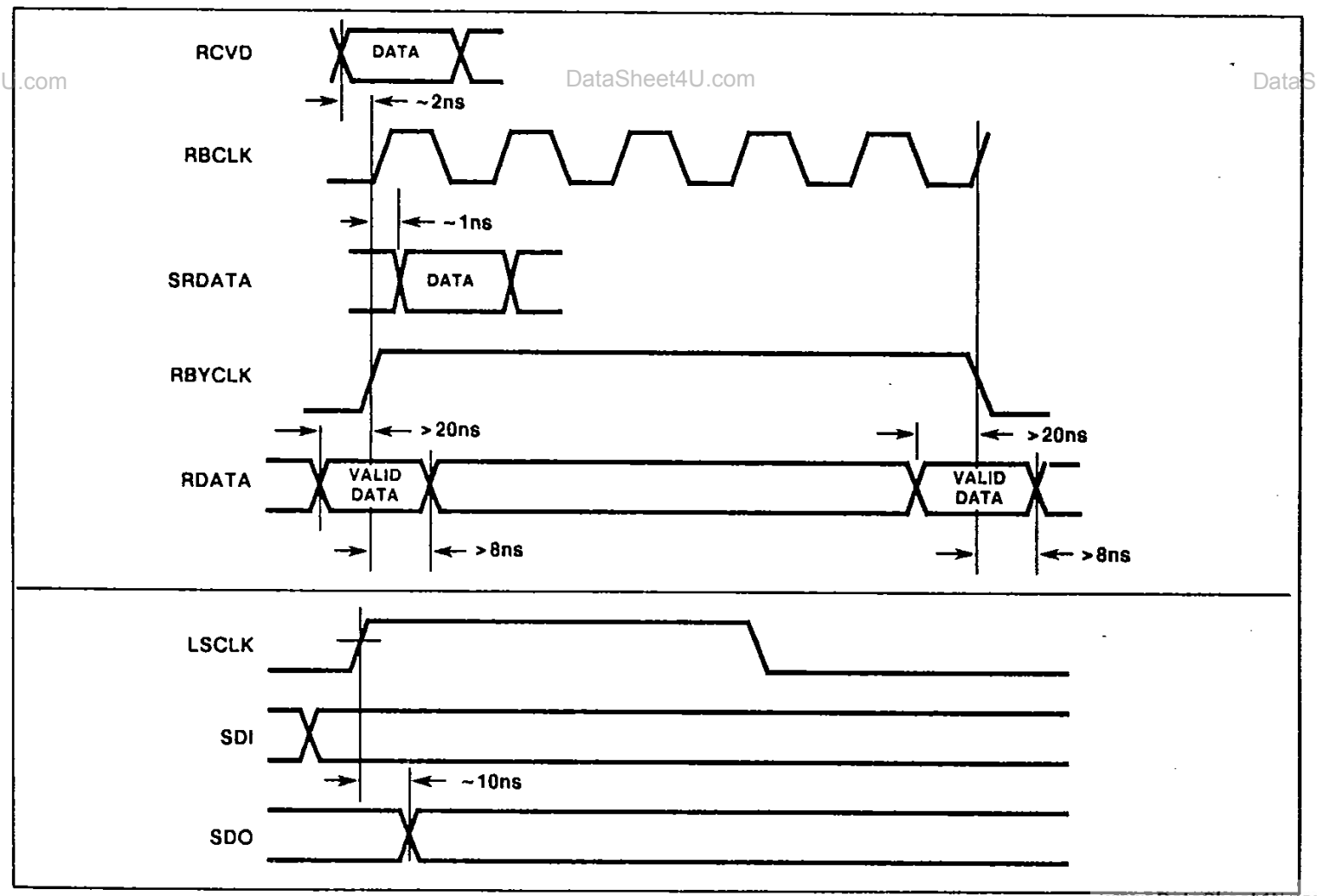


Fig.6 Receiver timing diagram

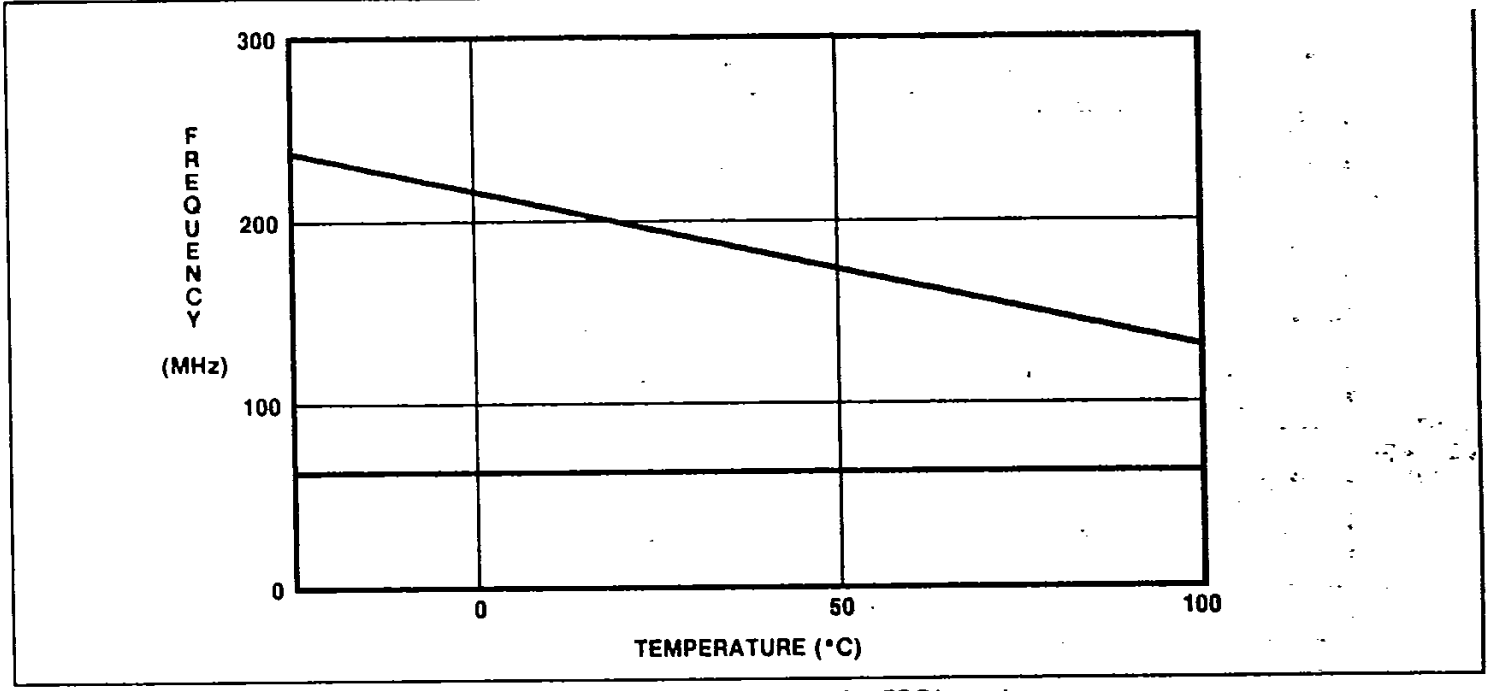


Fig.7 Operating clock frequency for FDDI receiver

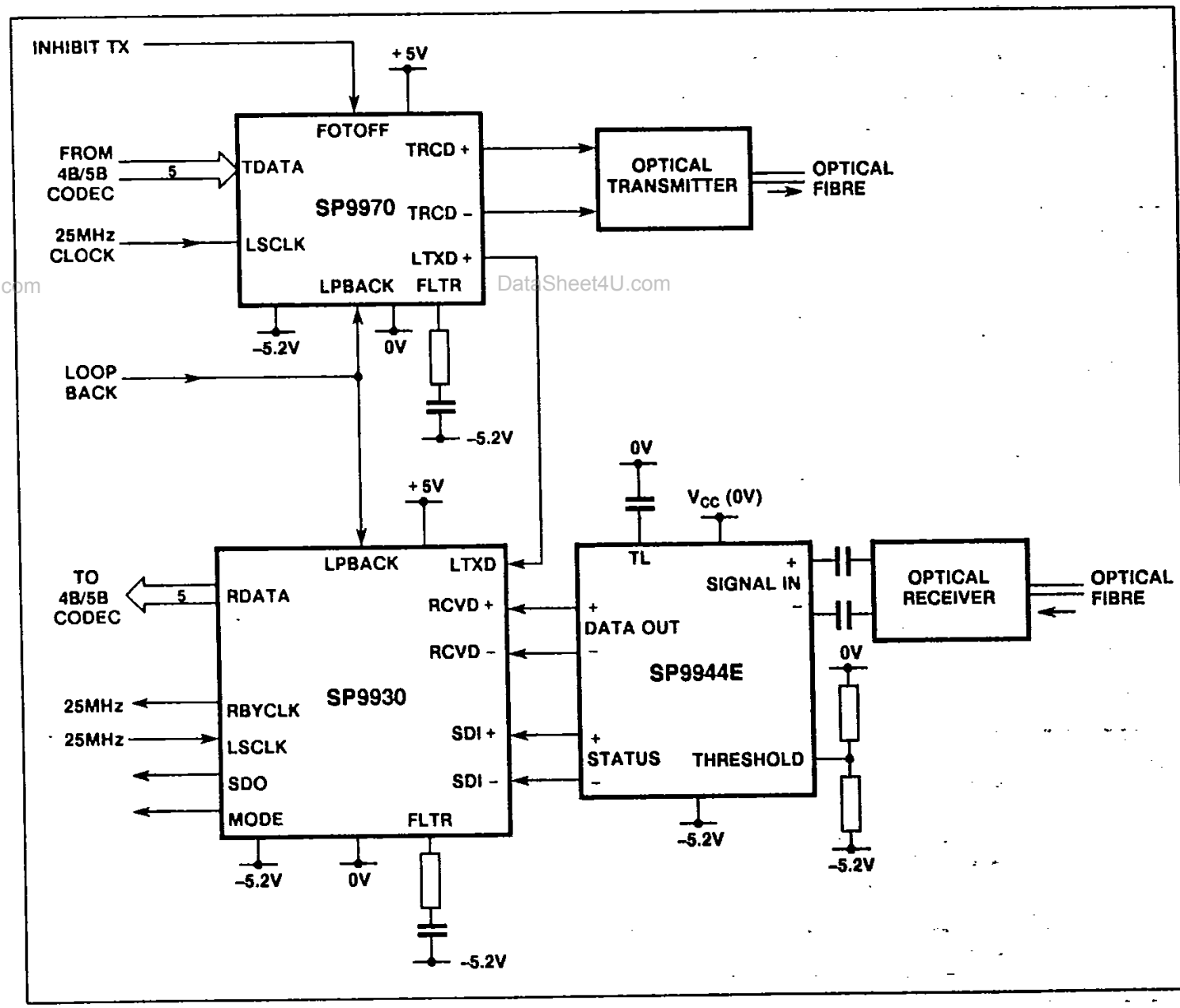


Fig.8 Typical FDDI application circuit