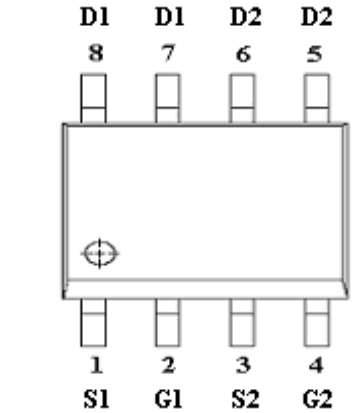
SPC1810
N & P Pair Enhancement Mode MOSFET

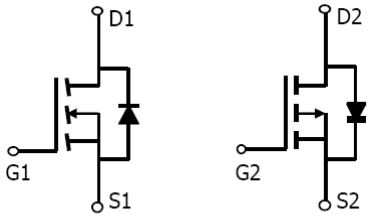
DESCRIPTION
The SPC1810 is the N- and P-Channel enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where high-side switching , low in-line power loss, and resistance to transients are needed.

FEATURES
- N-Channel
  100V/5A,$R_{DS(ON)}$=160mΩ@V_{GS}=10V
- P-Channel
  -100V/-8A,$R_{DS(ON)}$=160mΩ@V_{GS}=-10V
  -100V/-4A,$R_{DS(ON)}$=200mΩ@V_{GS}=-4.5V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP–8 package design

APPLICATIONS
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION(SOP–8)





n-channel p-channel

PART MARKING

A : Lot Code
B : Date Code

SPC1810
N & P Pair Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	S1	Source 1
2	G1	Gate 1
3	S2	Source 2
4	G2	Gate 2
5	D2	Drain 2
6	D2	Drain 2
7	D1	Drain 1
8	D1	Drain 1

ORDERING INFORMATION

Part Number	Package	Part Marking
SPC1810S8RGB	SOP- 8	SPC1810

※ SPC1810S8RGB 13” Tape Reel ; Pb – Free ; Halogen – Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical		Unit
			N-Channel	P-Channel	
Drain-Source Voltage		V_{DSS}	100	-100	V
Gate –Source Voltage		V_{GSS}	±20	±20	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_D	8.0	-8.0	A
	T_A=70℃		6.0	-6.0	
Pulsed Drain Current		I_{DM}	12	-12	A
Continuous Source Current(Diode Conduction)		I_S	2.3	-2.3	A
Power Dissipation	T_A=25℃	P_D	2.5	2.8	W
	T_A=70℃		1.6	1.8	
Operating Junction Temperature		T_J	-55/150		℃
Storage Temperature Range		T_{STG}	-55/150		℃
Thermal Resistance-Junction to Ambient	T ≤ 10sec	$R_{\theta JA}$	50	52	℃/W
	Steady State		80	80	

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N & P Pair Enhancement Mode MOSFET

ELECTRICAL CHARACTERISTICS (NMOS)

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	1.0		3.0	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=80V,V_{GS}=0V			25	uA
		V_{DS}=80V,V_{GS}=0V T_J=80℃			250	
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=5A			0.16	Ω
Forward Transconductance	gfs	V_{DS}=10V,I_D=5.0A		5.6		S
Diode Forward Voltage	V_{SD}	I_S=8.0A,V_{GS}=0V			1.3	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=80V,V_{GS}=5V I_D=5A		10	16	nC
Gate-Source Charge	Q_{gs}			2.5		
Gate-Drain Charge	Q_{gd}			4.5		
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V f=1MHz		425	680	pF
Output Capacitance	C_{oss}			55		
Reverse Transfer Capacitance	C_{rss}			33		
Turn-On Time	$t_{d(on)}$	V_{DD}=50V,R_D=10Ω I_D=5.0A,V_G=10V R_G=3.3Ω		6.5		nS
	t_r			10		
Turn-Off Time	$t_{d(off)}$			13		
	t_f			3.4		

ELECTRICAL CHARACTERISTICS (PMOS)

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-250uA	-100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250uA	-1.0		-3.0	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-10V,V_{GS}=0V			-1	uA
		V_{DS}=-80V,V_{GS}=0V T_J=85℃			-25	
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D= -8A			0.16	Ω
		V_{GS}=-4.5V,I_D=-6A			0.20	
Forward Transconductance	gfs	V_{DS}=-10V,I_D= -8A		8		S
Diode Forward Voltage	V_{SD}	I_S=-12A,V_{GS}=0V			-1.3	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-80V,V_{GS}=-4.5V I_D=-8.0A		16	25	nC
Gate-Source Charge	Q_{gs}			4.4		
Gate-Drain Charge	Q_{gd}			8.7		
Input Capacitance	C_{iss}	V_{DS}=-25V,V_{GS}=0V f=1MHz		1590	2550	pF
Output Capacitance	C_{oss}			110		
Reverse Transfer Capacitance	C_{rss}			70		
Turn-On Time	$t_{d(on)}$	V_{DD}=-50V,R_D=6.25Ω I_D=-8.0A,V_G=-10V R_G=3.3Ω		9		nS
	t_r			14		
Turn-Off Time	$t_{d(off)}$			45		
	t_f			40		

TYPICAL CHARACTERISTICS (NMOS)

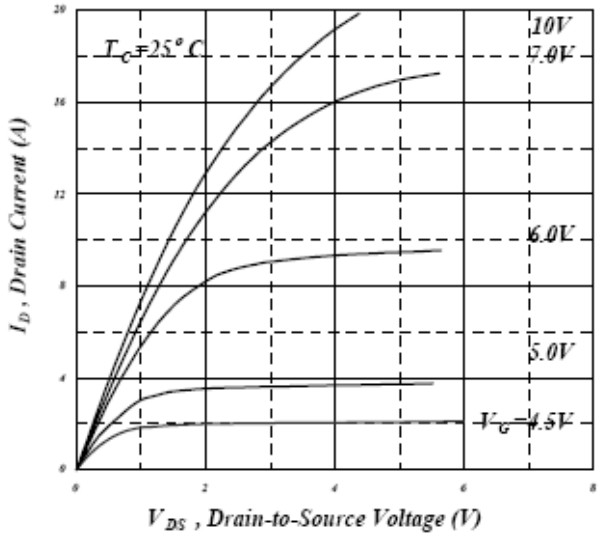

Fig 1. Typical Output Characteristics

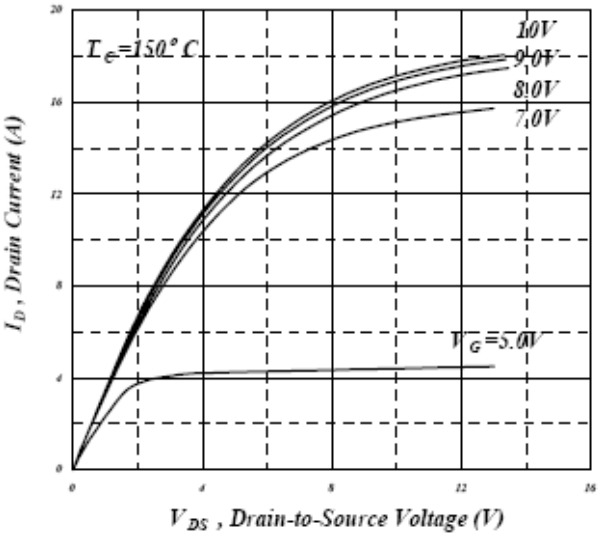

Fig 2. Typical Output Characteristics

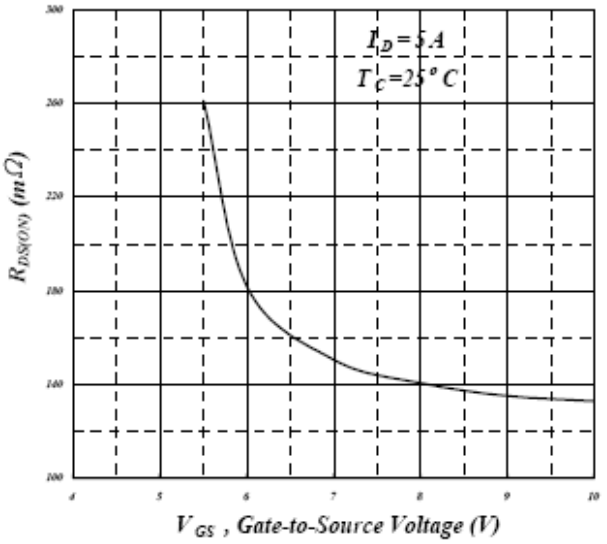

Fig 3. On-Resistance v.s. Gate Voltage

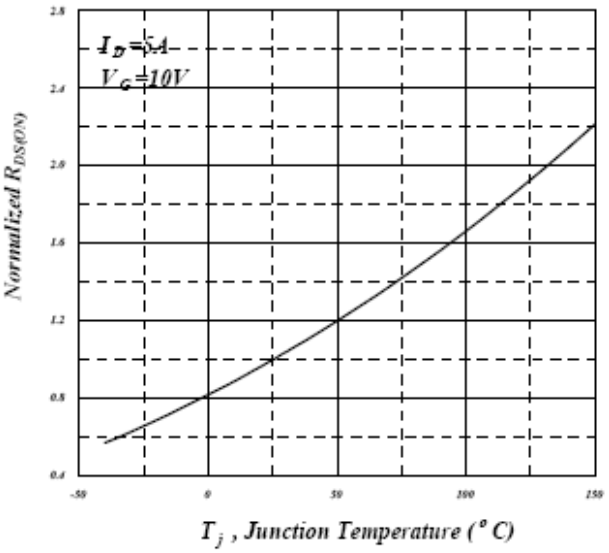

Fig 4. Normalized On-Resistance v.s. Junction Temperature

TYPICAL CHARACTERISTICS (NMOS)

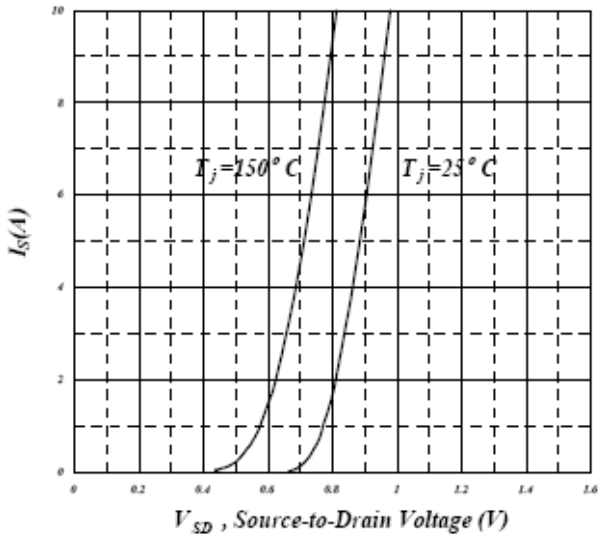

Fig 5. Forward Characteristic of Reverse Diode

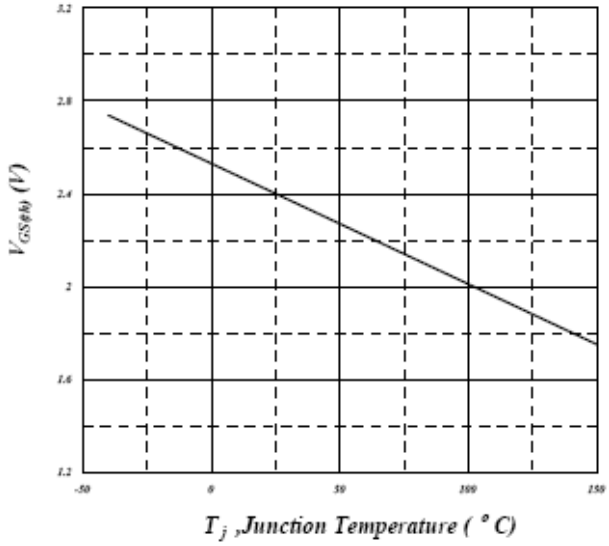

Fig 6. Gate Threshold Voltage v.s. Junction Temperature

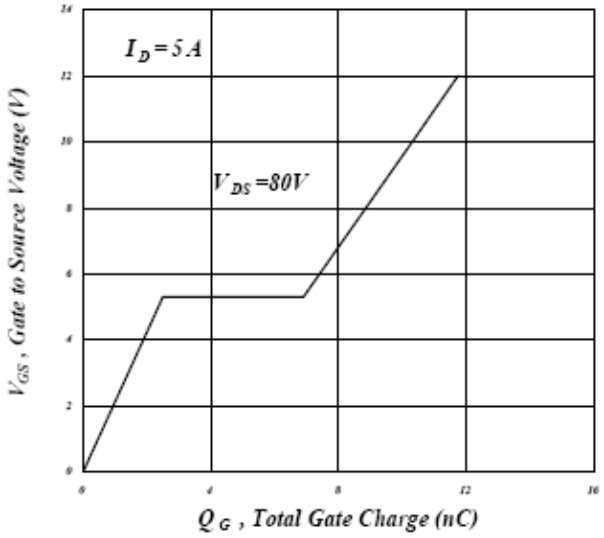

Fig 7. Gate Charge Characteristics

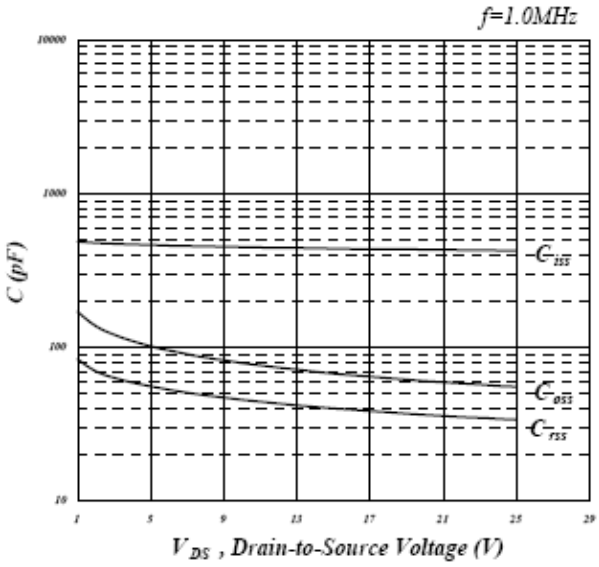

Fig 8. Typical Capacitance Characteristics

TYPICAL CHARACTERISTICS (NMOS)

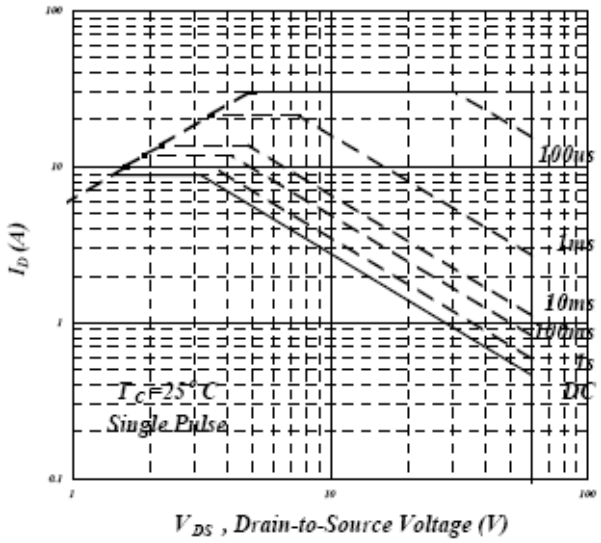

Fig 9. Maximum Safe Operating Area

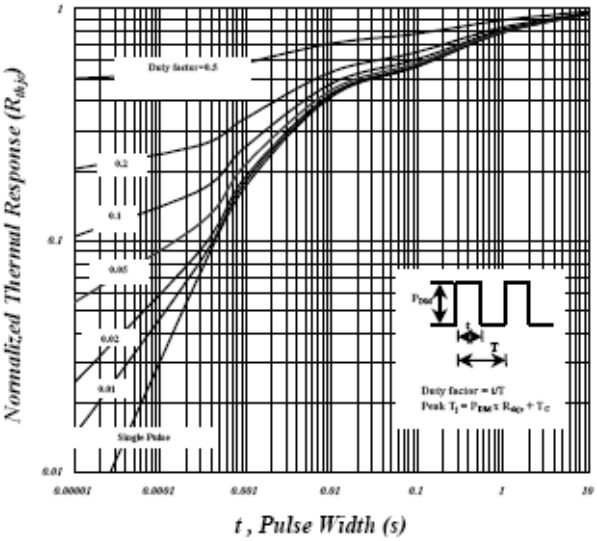

Fig 10. Effective Transient Thermal Impedance

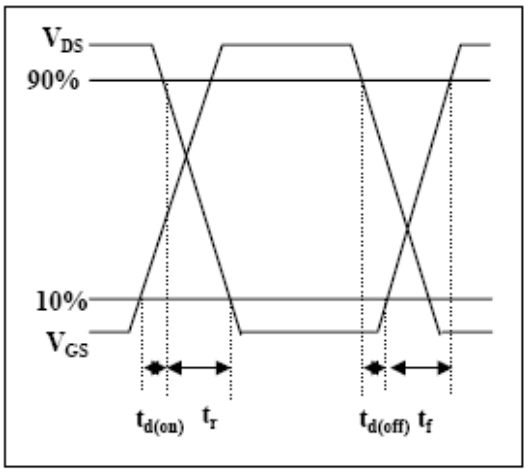

Fig 11. Switching Time Waveform

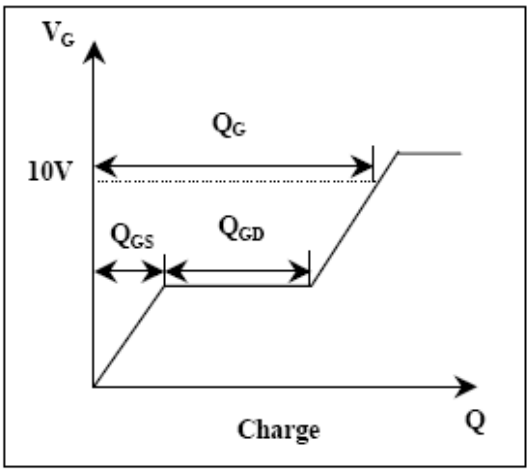

Fig 12. Gate Charge Waveform

TYPICAL CHARACTERISTICS (PMOS)

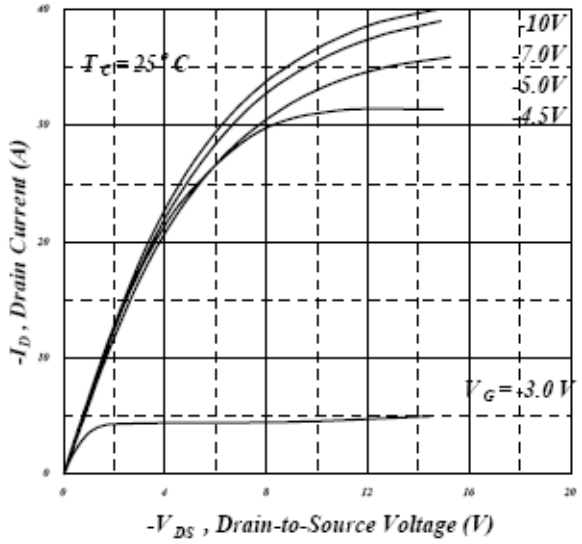

Fig 1. Typical Output Characteristics

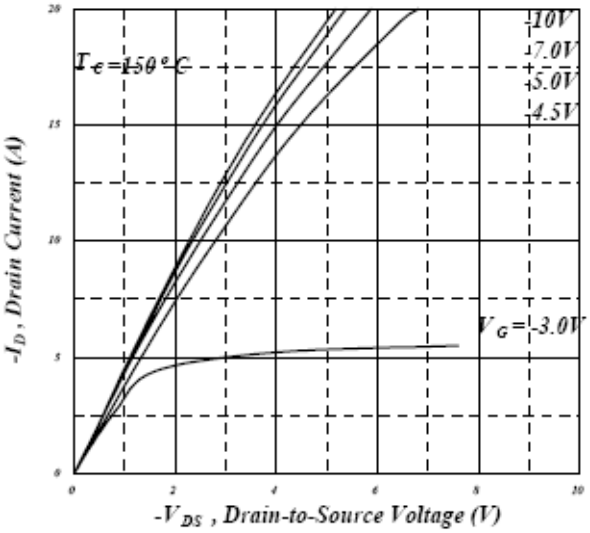

Fig 2. Typical Output Characteristics

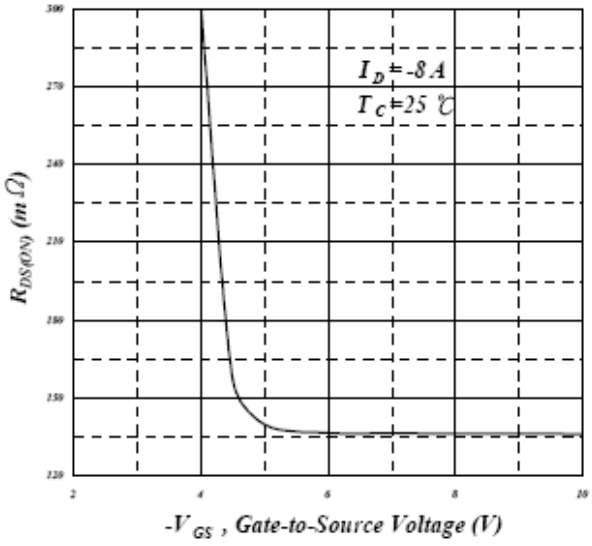

Fig 3. On-Resistance v.s. Gate Voltage

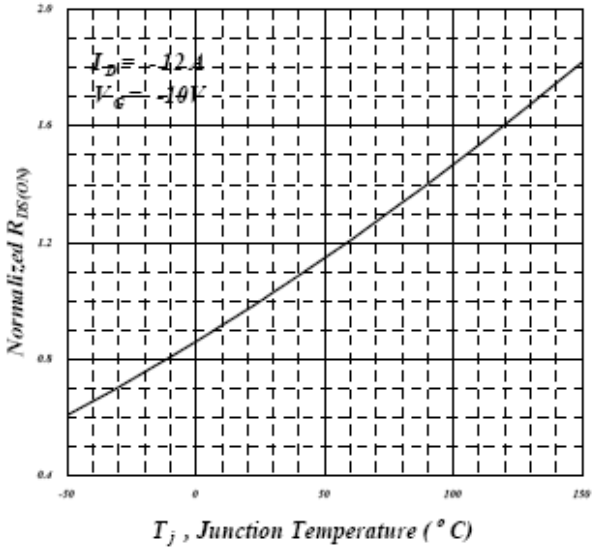

Fig 4. Normalized On-Resistance v.s. Junction Temperature

TYPICAL CHARACTERISTICS (PMOS)

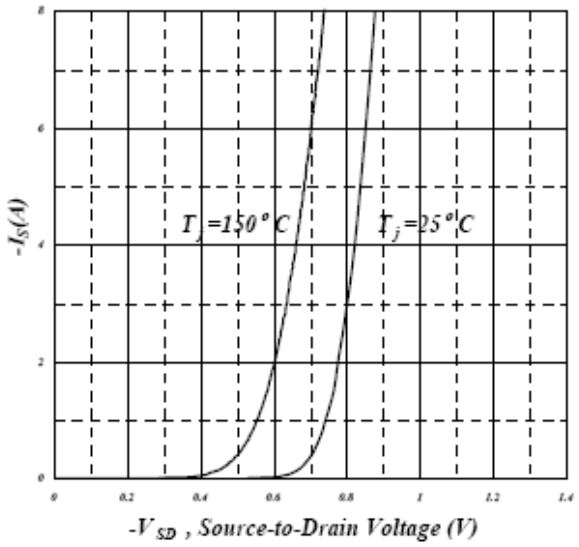

Fig 5. Forward Characteristic of Reverse Diode

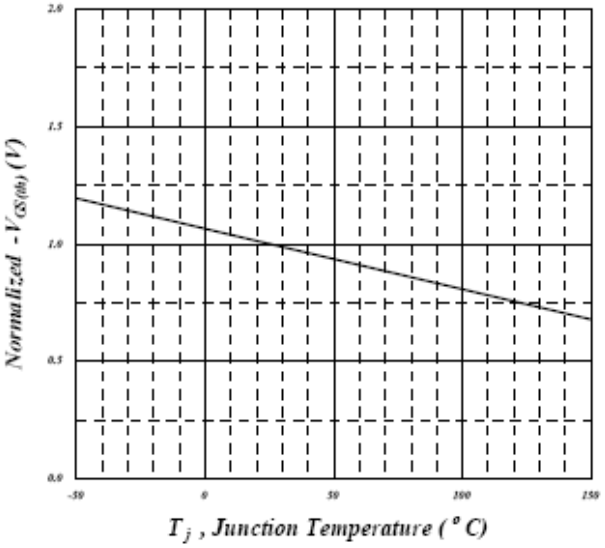

Fig 6. Gate Threshold Voltage v.s. Junction Temperature

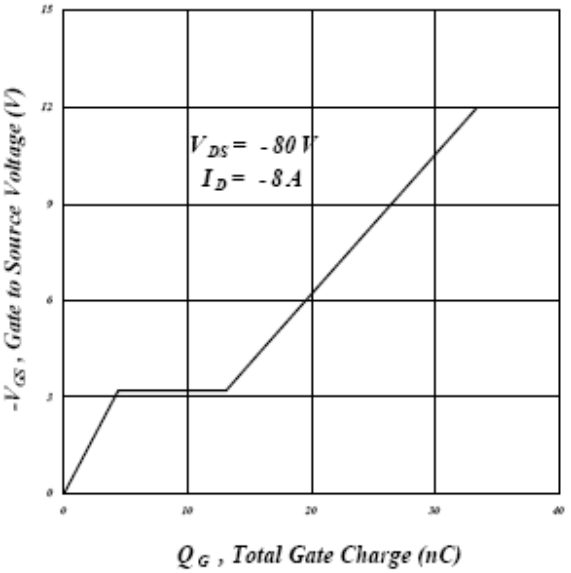

Fig 7. Gate Charge Characteristics

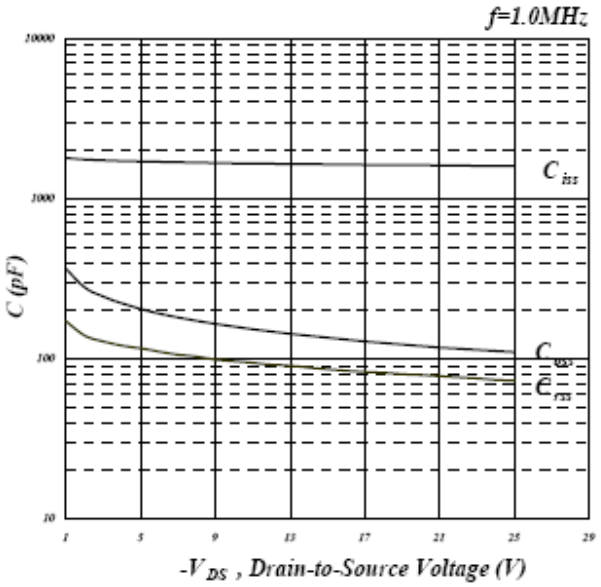

Fig 8. Typical Capacitance Characteristics

TYPICAL CHARACTERISTICS (PMOS)

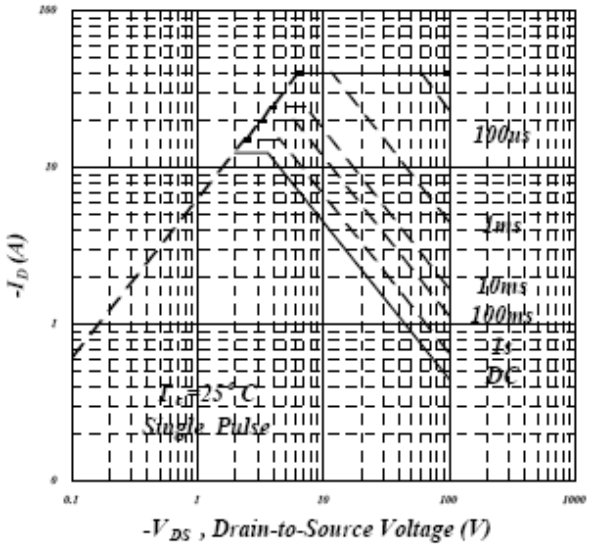

Fig 9. Maximum Safe Operating Area

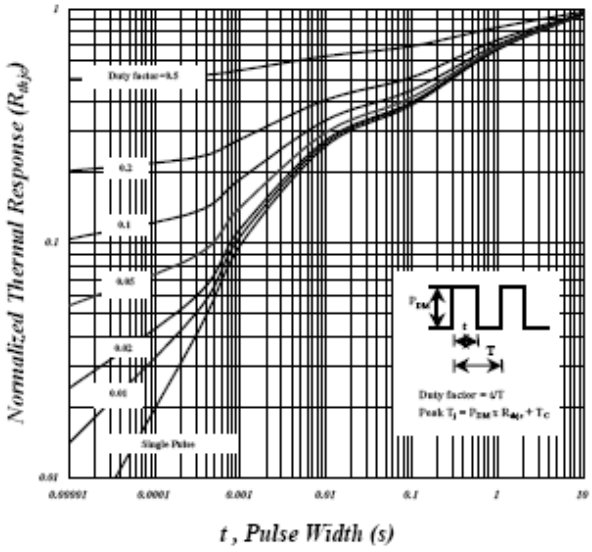

Fig 10. Effective Transient Thermal Impedance

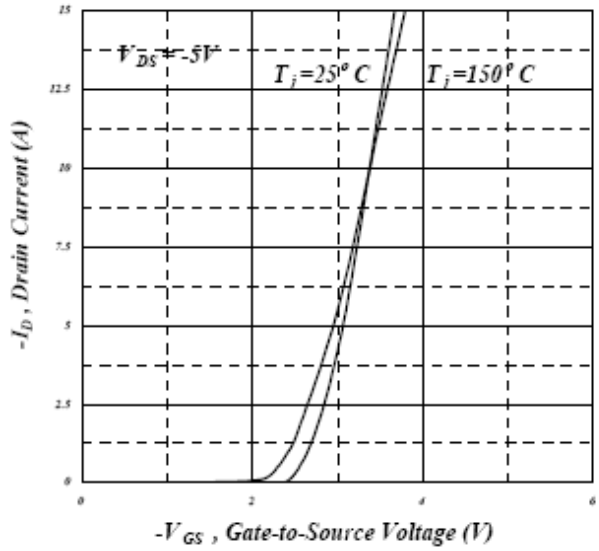

Fig 11. Transfer Characteristics

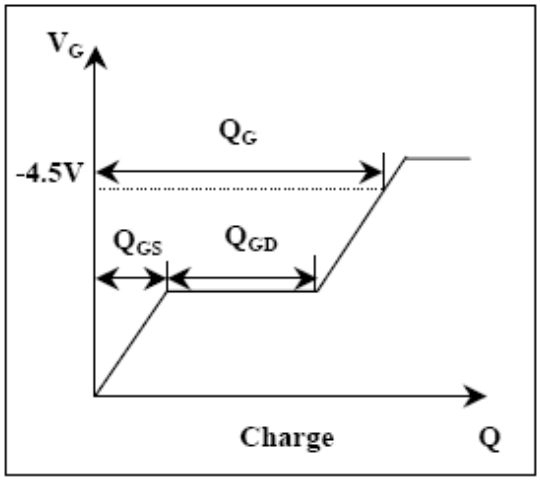

Fig 12. Gate Charge Waveform

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