



# SPC4527

## N & P Pair Enhancement Mode MOSFET

### DESCRIPTION

The SPC4527 is the N- and P-Channel enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where high-side switching , low in-line power loss, and resistance to transients are needed.

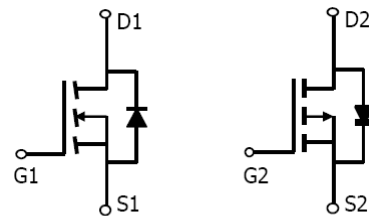
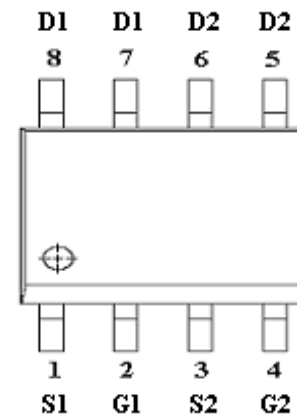
### FEATURES

- ◆ N-Channel
  - 40V/10A,  $R_{DS(ON)}=25m\Omega@V_{GS}=10V$
  - 40V/ 8A,  $R_{DS(ON)}=30m\Omega@V_{GS}=4.5V$
  - 40V/ 6A,  $R_{DS(ON)}=36m\Omega@V_{GS}=2.5V$
- ◆ P-Channel
  - 40V/-10A,  $R_{DS(ON)}=38m\Omega@V_{GS}=-10V$
  - 40V/-8A,  $R_{DS(ON)}=46m\Omega@V_{GS}=-4.5V$
- ◆ Super high density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOP-8 package design

### APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

### PIN CONFIGURATION(SOP-8)



n-channel

p-channel

### PART MARKING



A : Lot Code  
B : Date Code



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### PIN DESCRIPTION

Pin	Symbol	Description
1	S1	Source 1
2	G1	Gate 1
3	S2	Source 2
4	G2	Gate 2
5	D2	Drain 2
6	D2	Drain 2
7	D1	Drain 1
8	D1	Drain 1

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPC4527S8RGB	SOP-8	SPC4527

※ SPC4527S8RGB 13" Tape Reel ; Pb – Free ; Halogen – Free

### ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical		Unit	
		N-Channel	P-Channel		
Drain-Source Voltage	V <sub>DSS</sub>	40	-40	V	
Gate –Source Voltage	V <sub>GSS</sub>	±20	±20	V	
Continuous Drain Current(T <sub>J</sub> =150°C)	I <sub>D</sub>	TA=25°C	10.0	-10.0	A
		TA=70°C	8.0	-8.0	
Pulsed Drain Current	I <sub>DM</sub>	25	-25	A	
Continuous Source Current(Diode Conduction)	I <sub>S</sub>	2.3	-2.3	A	
Power Dissipation	P <sub>D</sub>	TA=25°C	2.5	2.8	W
		TA=70°C	1.6	1.8	
Operating Junction Temperature	T <sub>J</sub>	-55/150		°C	
Storage Temperature Range	T <sub>STG</sub>	-55/150		°C	
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	T ≤ 10sec	50	52	°C/W
		Steady State	80	80	



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### ELECTRICAL CHARACTERISTICS ( NMOS )

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	40			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5		1.0	V
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=40V, V_{GS}=0V$			1	uA
		$V_{DS}=40V, V_{GS}=0V$ $T_J=85^\circ C$			10	
On-State Drain Current	$I_{D(on)}$	$V_{DS}=5V, V_{GS}=4.5V$	10			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=10A$		0.020	0.025	$\Omega$
		$V_{GS}=4.5V, I_D=8A$		0.023	0.030	
		$V_{GS}=2.5V, I_D=6A$		0.027	0.036	
Forward Transconductance	$g_{fs}$	$V_{DS}=15V, I_D=6.2A$		13		S
Diode Forward Voltage	$V_{SD}$	$I_S=2.3A, V_{GS}=0V$		0.8	1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=20V, V_{GS}=4.5V$ $I_D=5A$		10	14	nC
Gate-Source Charge	$Q_{gs}$			2.8		
Gate-Drain Charge	$Q_{gd}$			3.2		
Input Capacitance	$C_{iss}$	$V_{DS}=20V, V_{GS}=0V$ $f=1MHz$		850		pF
Output Capacitance	$C_{oss}$			110		
Reverse Transfer Capacitance	$C_{rss}$			75		
Turn-On Time	$t_{d(on)}$	$V_{DD}=20V, R_L=4\Omega$ $I_D=5.0A, V_{GEN}=10V$ $R_G=1\Omega$		6	12	nS
	$t_r$			10	20	
Turn-Off Time	$t_{d(off)}$			20	36	
	$t_f$			6	12	



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### ELECTRICAL CHARACTERISTICS ( PMOS )

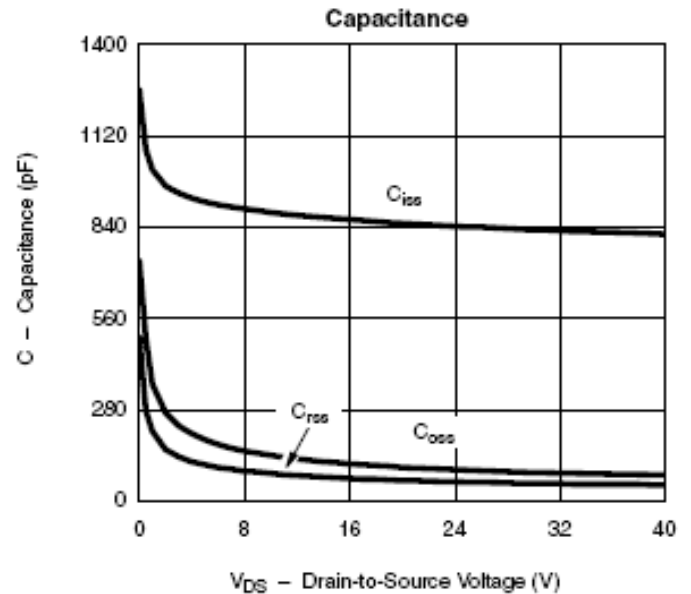
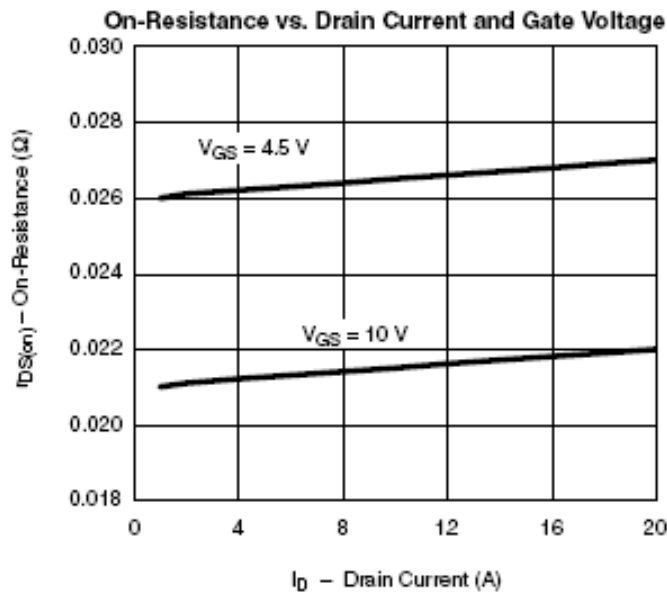
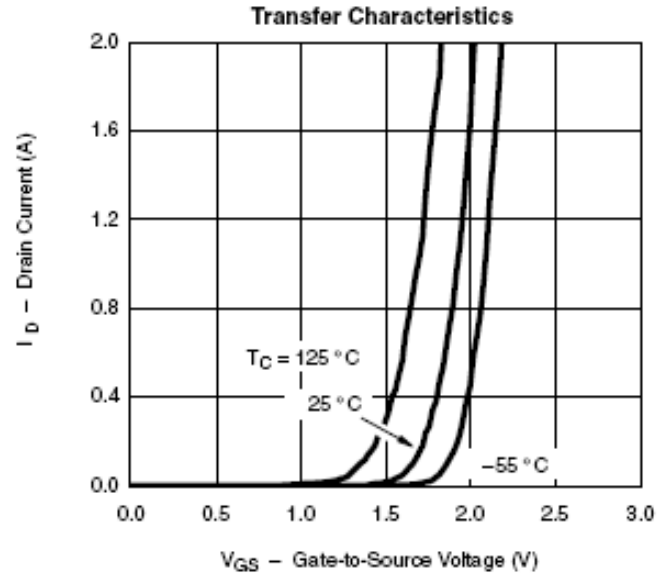
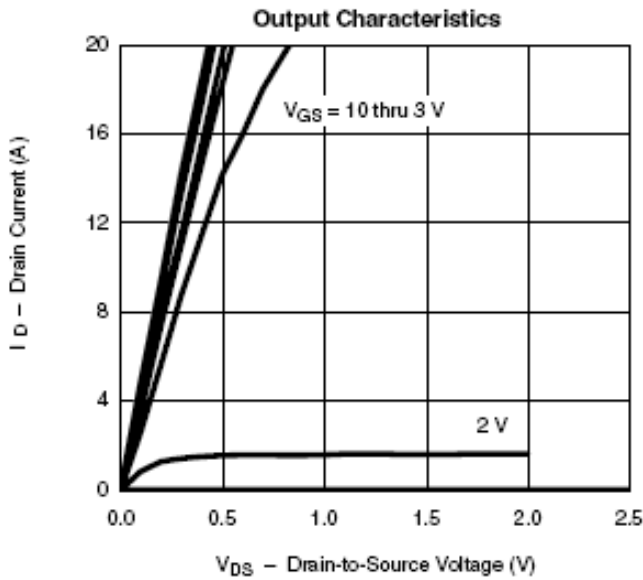
(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-40			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.8		-2.5	V
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-36V, V_{GS}=0V$			-1	uA
		$V_{DS}=-36V, V_{GS}=0V$ $T_J=85^\circ C$			-10	
On-State Drain Current	$I_{D(on)}$	$V_{DS}=-5V, V_{GS}=-4.5V$	-10			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-10A$		0.032	0.038	$\Omega$
		$V_{GS}=-4.5V, I_D=-8A$		0.036	0.046	
Forward Transconductance	$g_{fs}$	$V_{DS}=-15V, I_D=-5.7A$		13		S
Diode Forward Voltage	$V_{SD}$	$I_S=-2.3A, V_{GS}=0V$		-0.8	-1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=-20V, V_{GS}=-4.5V$ $I_D=-5.0A$		13	20	nC
Gate-Source Charge	$Q_{gs}$			4.5		
Gate-Drain Charge	$Q_{gd}$			6.5		
Input Capacitance	$C_{iss}$	$V_{DS}=-20V, V_{GS}=0V$ $f=1MHz$		1100		pF
Output Capacitance	$C_{oss}$			145		
Reverse Transfer Capacitance	$C_{rss}$			115		
Turn-On Time	$t_{d(on)}$	$V_{DD}=-20V, R_L=4\Omega$ $I_D=-5.0A, V_{GEN}=-4.5V$ $R_G=1\Omega$		40	80	nS
	$t_r$			55	100	
Turn-Off Time	$t_{d(off)}$			30	60	
	$t_f$			12	20	



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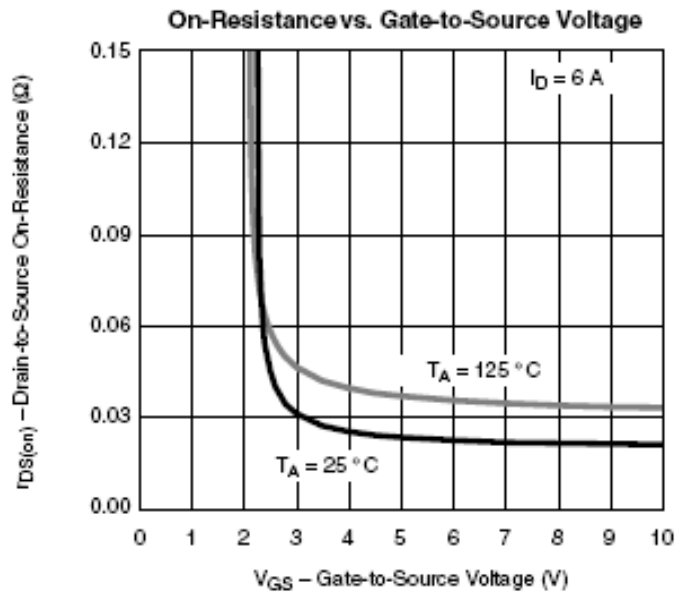
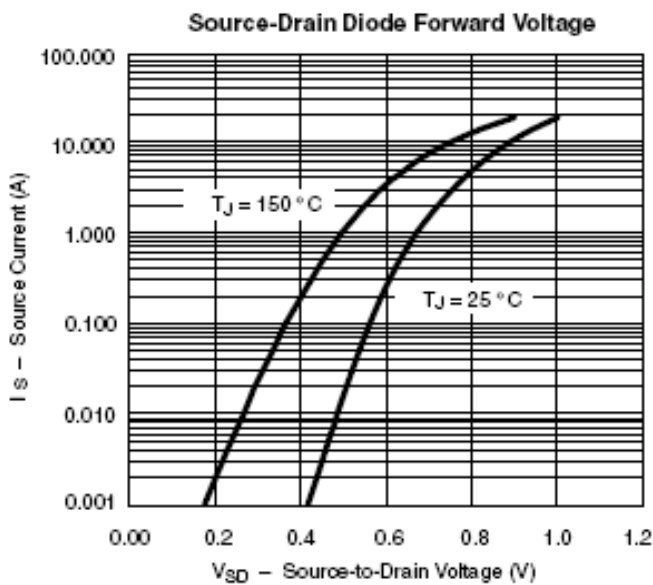
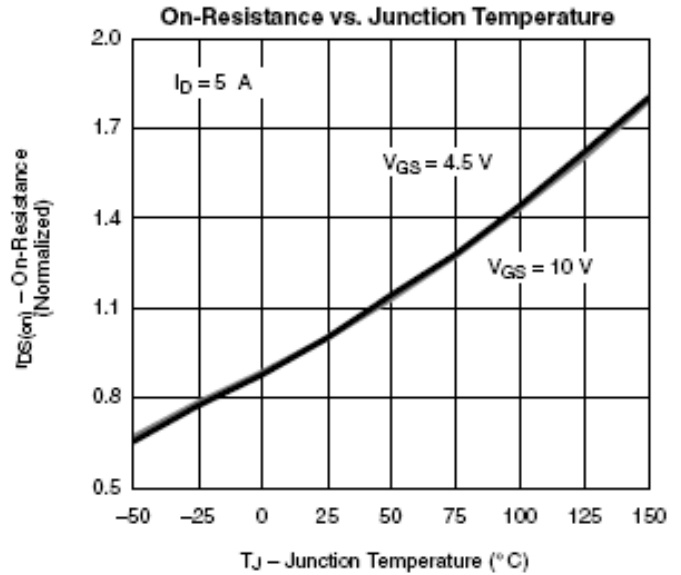
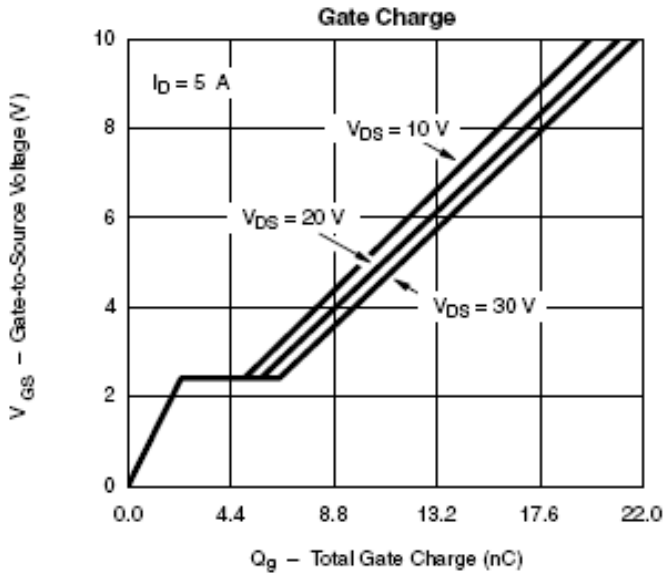
## TYPICAL CHARACTERISTICS (NMOS)





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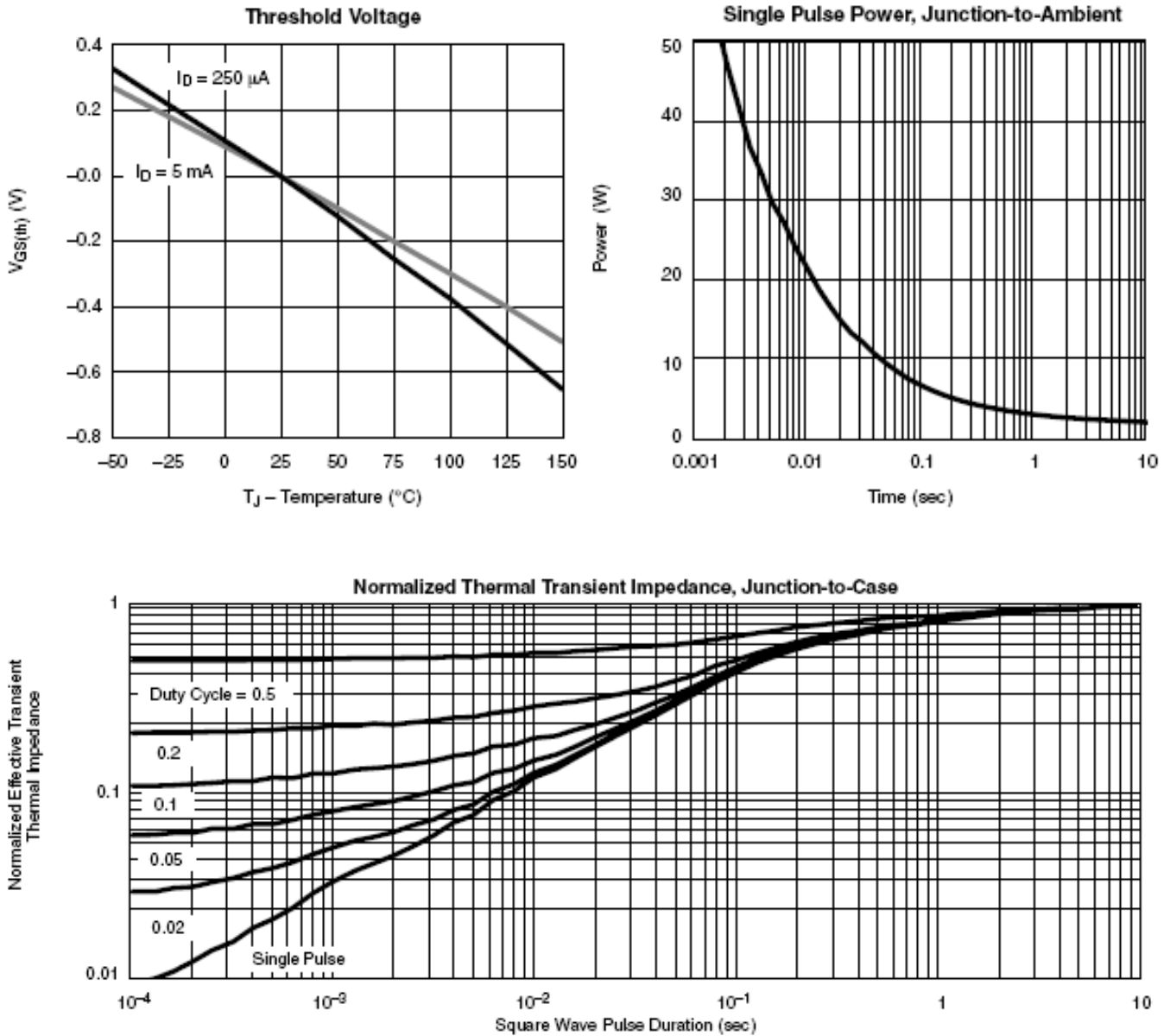
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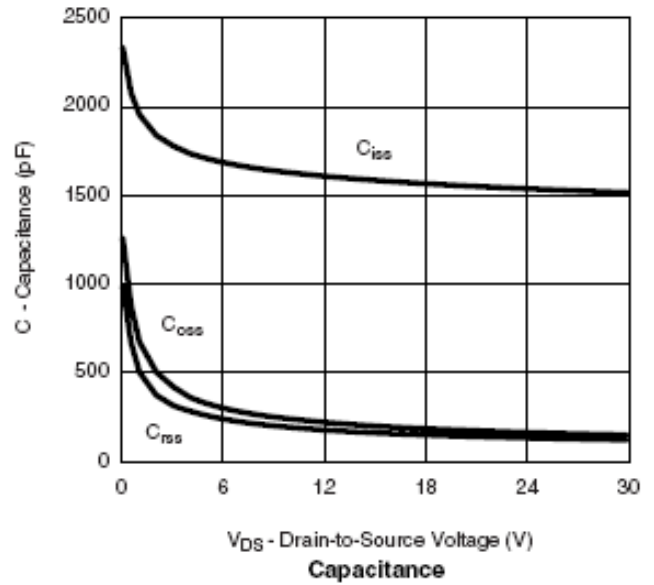
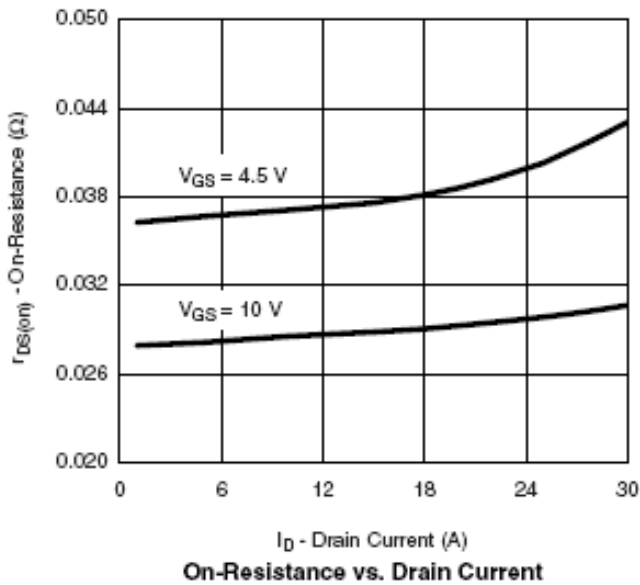
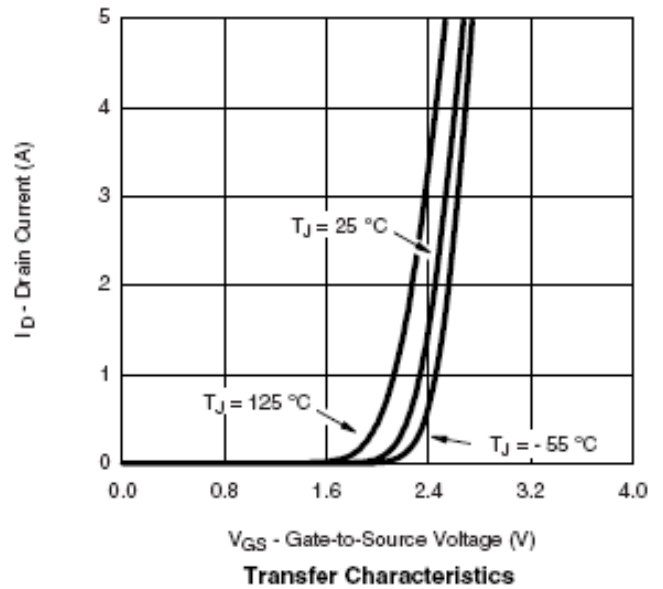
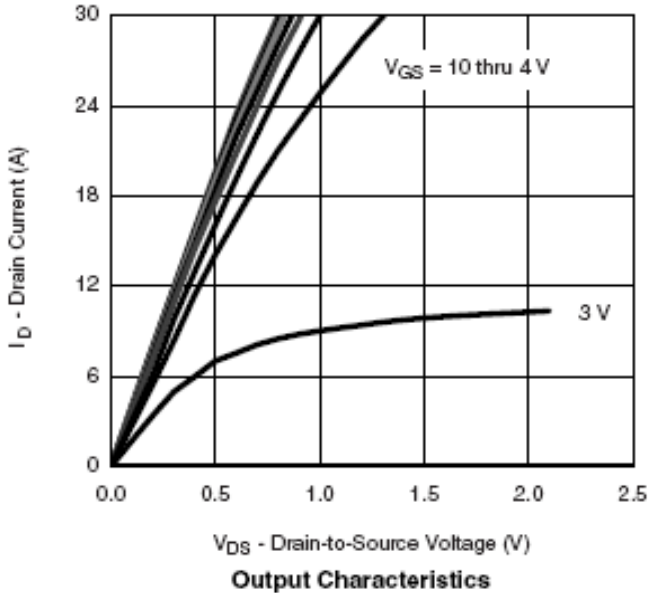




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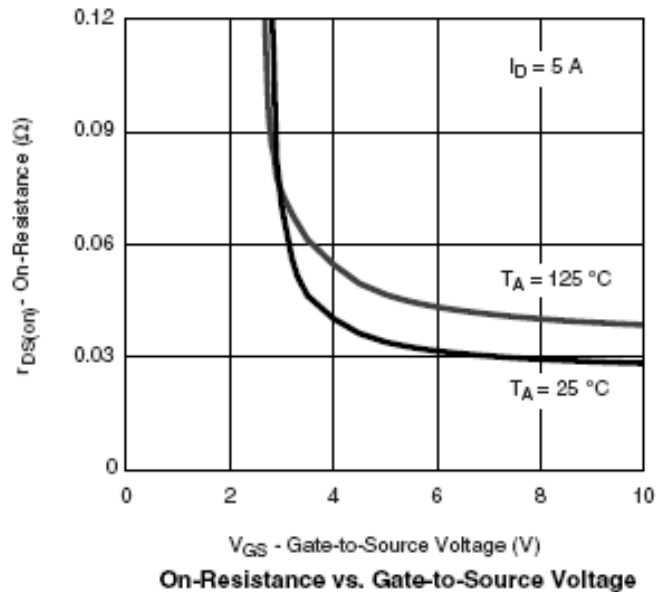
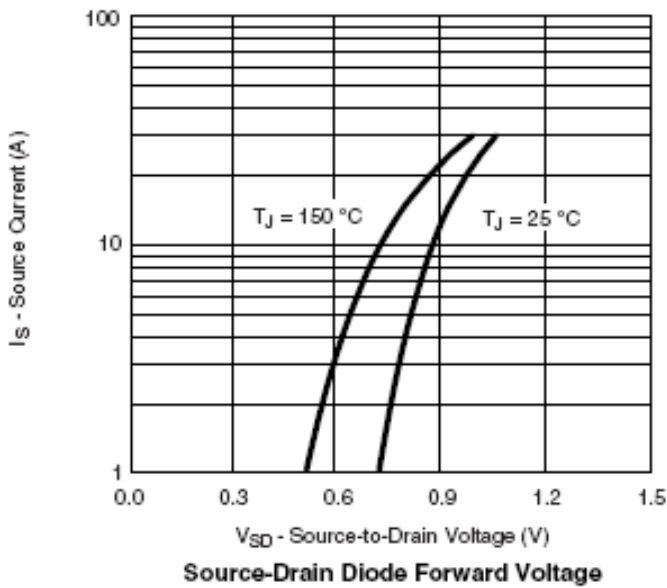
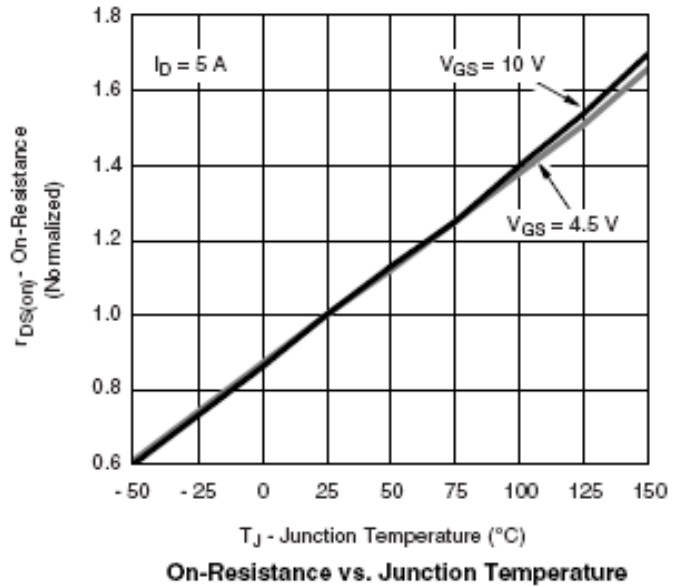
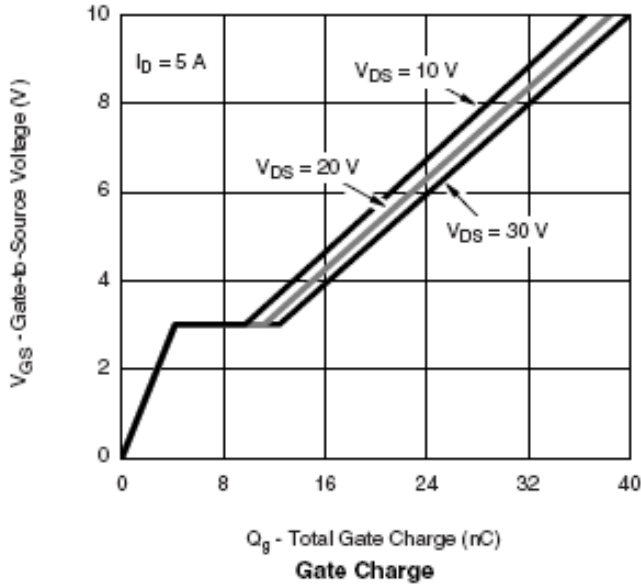






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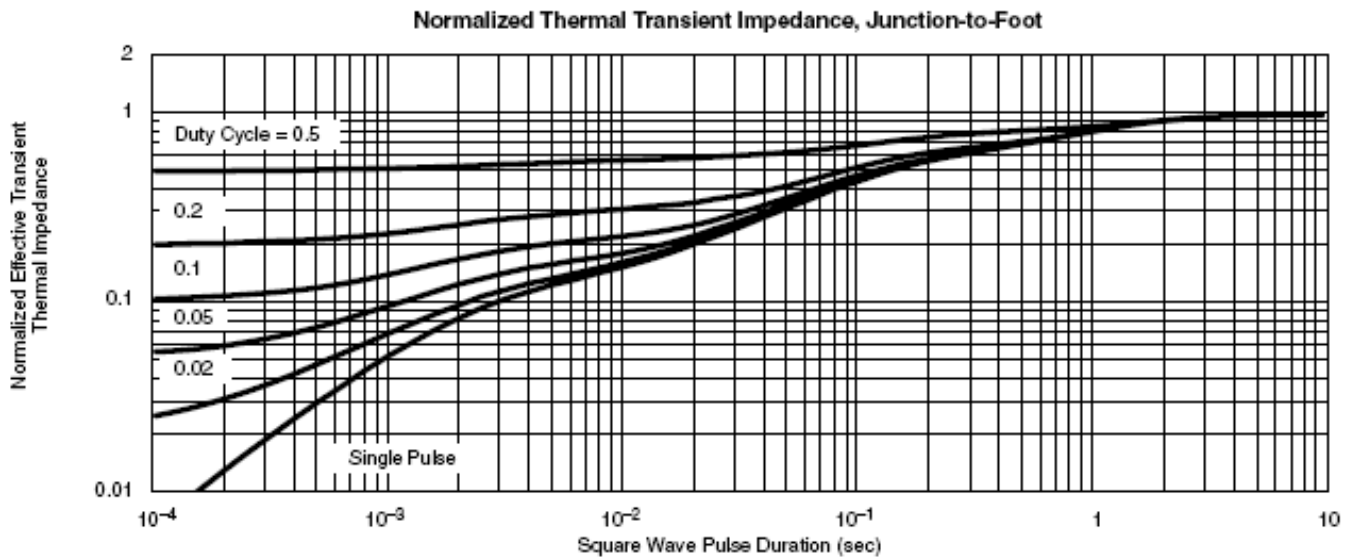
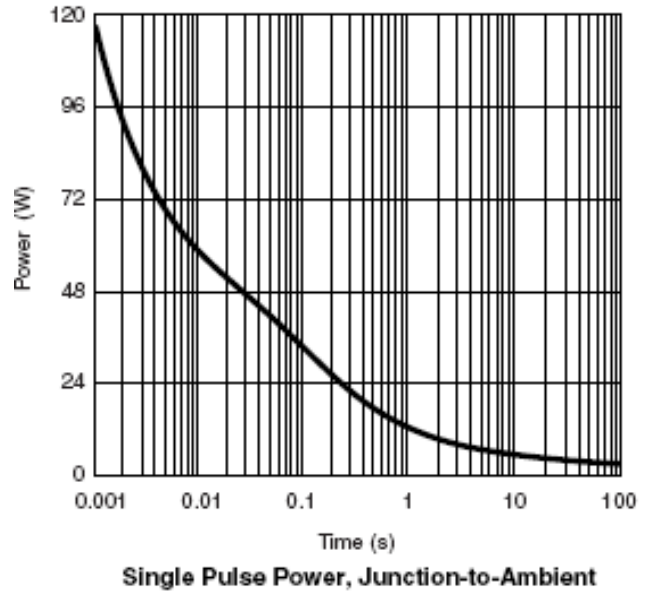
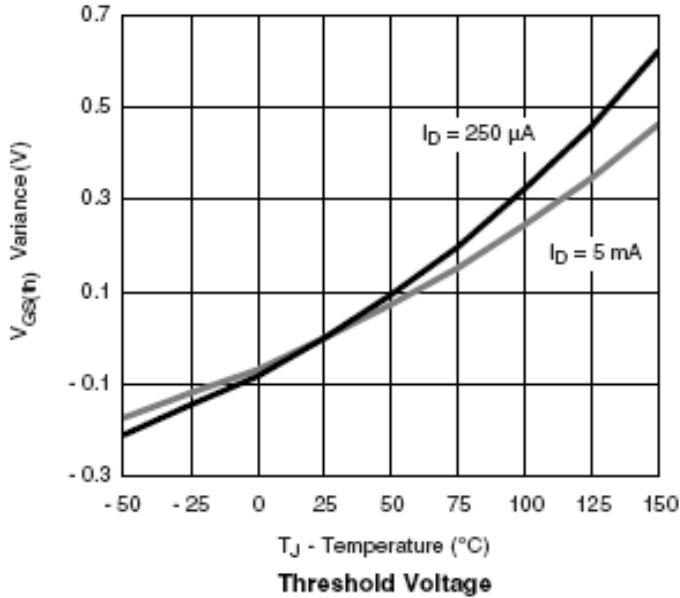
## TYPICAL CHARACTERISTICS (PMOS)





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