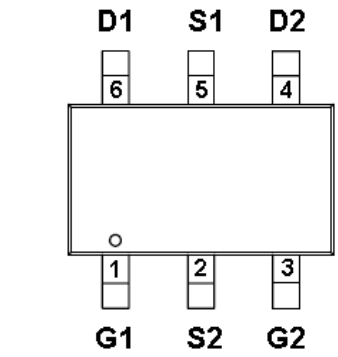
SPC6605
N & P Pair Enhancement Mode MOSFET

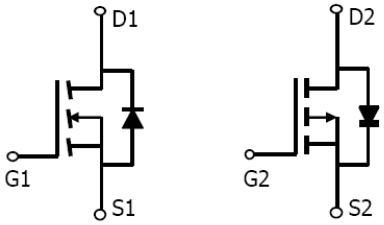
DESCRIPTION
The SPC6605 is the N- and P-Channel enhancement mode power field effect transistors are produced using high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where high-side switching, low in-line power loss, and resistance to transients are needed.

APPLICATIONS
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

FEATURES
- N-Channel
  20V/3.6A,$R_{DS(ON)}$=97mΩ@V_{GS}=4.5V
  20V/3.1A,$R_{DS(ON)}$=113mΩ@V_{GS}=2.5V
- P-Channel
  -20V/-2.4A,$R_{DS(ON)}$= 128mΩ@V_{GS}=-4.5V
  -20V/-2.0A,$R_{DS(ON)}$=188mΩ@V_{GS}=-2.5V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- TSOT-23-6L package design

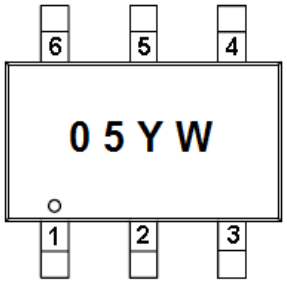
PIN CONFIGURATION(TSOT-23–6L)





n-channel p-channel

PART MARKING



Y : Year Code
W : Week Code

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PIN DESCRIPTION

Pin	Symbol	Description
1	G1	Gate 1
2	S2	Source 2
3	G2	Gate 2
4	D2	Drain 2
5	S1	Source 1
6	D1	Drain1

ORDERING INFORMATION

Part Number	Package	Part Marking
SPC6605TS26RGB	TSOT-23-6L	05

※ Week Code : A ~ Z(1 ~ 26) ; a ~ z(27 ~ 52)

※ SPC6605TS26RGB : Tape Reel ; Pb – Free ; Halogen -Free

ABSOULTE MAXIMUM RATINGS

(T_A=25°C Unless otherwise noted)

Parameter		Symbol	Typical		Unit
			N-Channel	P-Channel	
Drain-Source Voltage		V_{DSS}	20	-20	V
Gate –Source Voltage		V_{GSS}	±12	±12	V
Continuous Drain Current(T_J=150°C)	T_A=25°C	I_D	3.2	-2.4	A
	T_A=70°C		2.6	-1.8	
Pulsed Drain Current		I_{DM}	10	-8	A
Continuous Source Current(Diode Conduction)		I_S	1.6	-1.4	A
Power Dissipation	T_A=25°C	P_D	1.15		W
	T_A=70°C		0.75		
Operating Junction Temperature		T_J	-55/150		°C
Storage Temperature Range		T_{STG}	-55/150		°C
Thermal Resistance-Junction to Ambient	T ≤ 10sec	$R_{\theta JA}$	50	52	°C/W
	Steady State		90	95	

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N & P Pair Enhancement Mode MOSFET

ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions		Min.	Typ	Max.	Unit
Static							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D= 250uA	N-Ch	20			V
		V_{GS}=0V,I_D=-250uA	P-Ch	-20			
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	N-Ch	0.45		1.2	
		V_{DS}=V_{GS},I_D=-250uA	P-Ch	-0.45		-1.2	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±12V	N-Ch			±100	nA
		V_{DS}=0V,V_{GS}=±12V	P-Ch			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=20V,V_{GS}=0V	N-Ch			1	uA
		V_{DS}=-20V,V_{GS}=0V	P-Ch			-1	
		V_{DS}=20V,V_{GS}=0V T_J=55℃	N-Ch			10	
		V_{DS}=-20V,V_{GS}=0V T_J=55℃	P-Ch			-10	
On-State Drain Current	$I_{D(on)}$	V_{DS}≥ 4.5V,V_{GS}=4.5V	N-Ch	6			A
		V_{DS}≤ -4.5V,V_{GS}=-4.5V	P-Ch	-6			
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=4.5V,I_D=3.6A	N-Ch		0.085	0.097	Ω
		V_{GS}=-4.5V,I_D=-2.4A	P-Ch		0.115	0.128	
		V_{GS}=2.5V,I_D=3.1A	N-Ch		0.100	0.113	
		V_{GS}=-2.5V,I_D=-2.0A	P-Ch		0.165	0.188	
Forward Transconductance	gfs	V_{DS}=5V,I_D=-3.4A	N-Ch		10		S
		V_{DS}=-5V,I_D=-2.4A	P-Ch		6.5		
Diode Forward Voltage	V_{SD}	I_S=1.6A,V_{GS}=0V	N-Ch		0.85	1.2	V
		I_S=-1.6A,V_{GS}=0V	P-Ch		-0.8	-1.2	
Dynamic							
Total Gate Charge	Q_g	N-Channel V_{DS}=10V,V_{GS}=4.5V, I_D=3.6A P-Channel V_{DS}=-16V,V_{GS}=-4.5V ,I_D=-2.A	N-Ch		4.4		nC
			P-Ch		7.5		
Gate-Source Charge	Q_{gs}		N-Ch		0.6		
			P-Ch		1		
Gate-Drain Charge	Q_{gd}		N-Ch		1.9		
			P-Ch		3		
Input Capacitance	Ciss	N-Channel V_{DS}=10V,V_{GS}=0V, f=1.0MHz P-Channel V_{DS}=-20V,V_{GS}=0V,f=1.0MHz	N-Ch		145		pF
			P-Ch		7.5		
Output Capacitance	Coss		N-Ch		100		
			P-Ch		550		
Reverse Transfer Capacitance	Crss		N-Ch		50		
			P-Ch		55		
Turn-On Time	$t_{d(on)}$	N-Channel V_{DD}=10V,R_L=2.8Ω ,I_D=3.6A V_{GEN}=4.5V ,R_G=6Ω P-Channel V_{DD}=-10V,R_L=10Ω ,I_D=-1.0A V_{GEN}=-4.5V ,R_G=3.3Ω	N-Ch		5.2		nS
			P-Ch		8.5		
	t_r		N-Ch		37		
			P-Ch		18		
Turn-Off Time	$t_{d(off)}$		N-Ch		15		
			P-Ch		22		
	t_f		N-Ch		5.7		
			P-Ch		10		

TYPICAL CHARACTERISTICS (P-Channel)

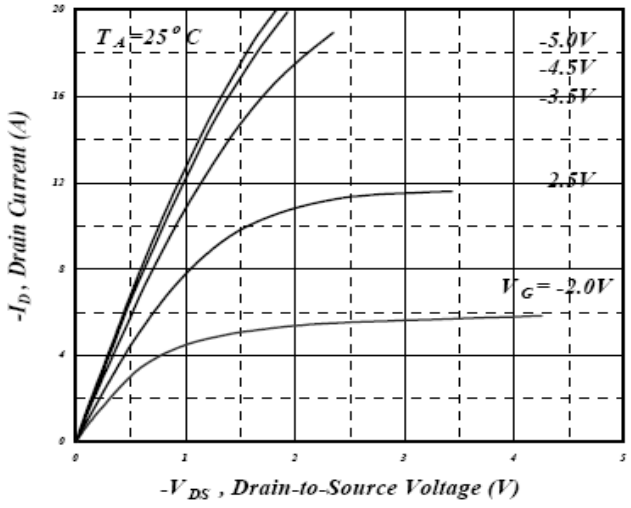


Fig 1. Typical Output Characteristics

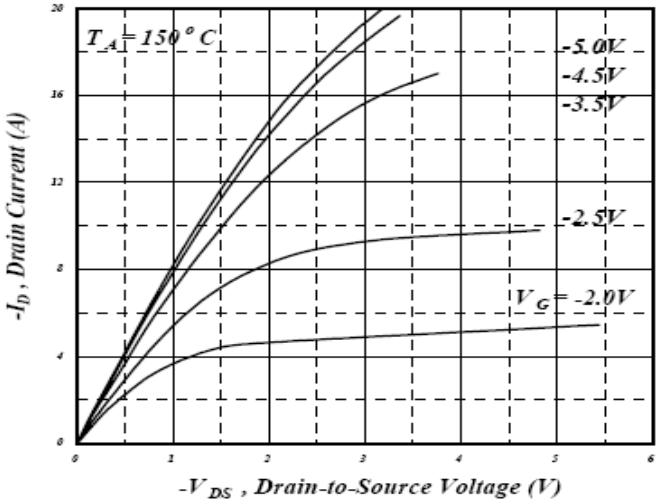


Fig 2. Typical Output Characteristics

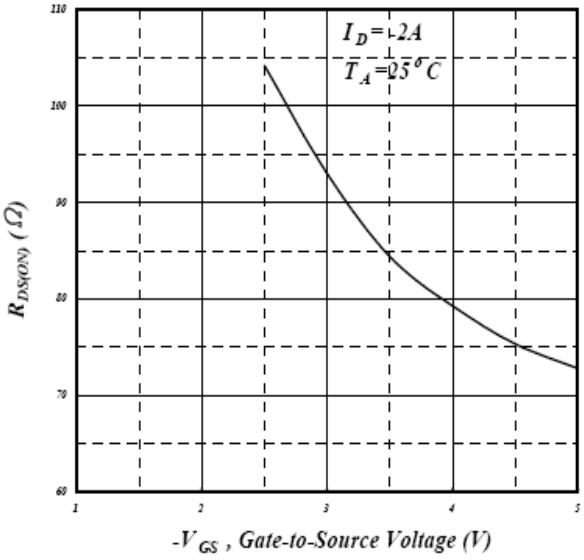


Fig 3. On-Resistance v.s. Gate Voltage

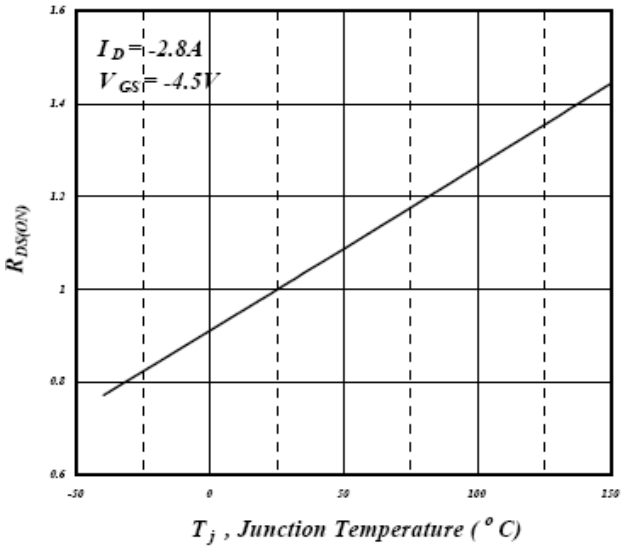


Fig 4. Normalized On-Resistance v.s. Junction Temperature

TYPICAL CHARACTERISTICS (P-Channel)

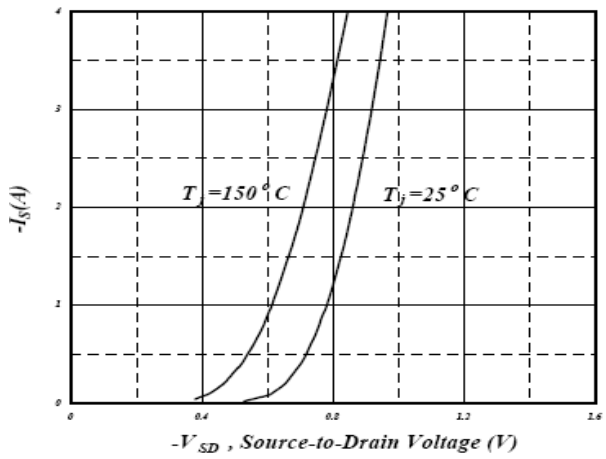


Fig 5. Forward Characteristic of Reverse Diode

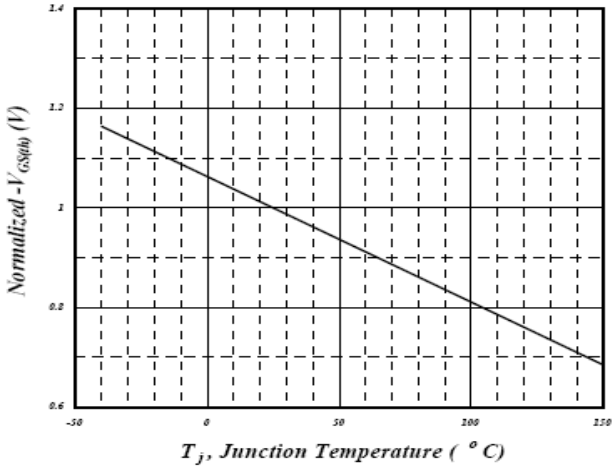


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

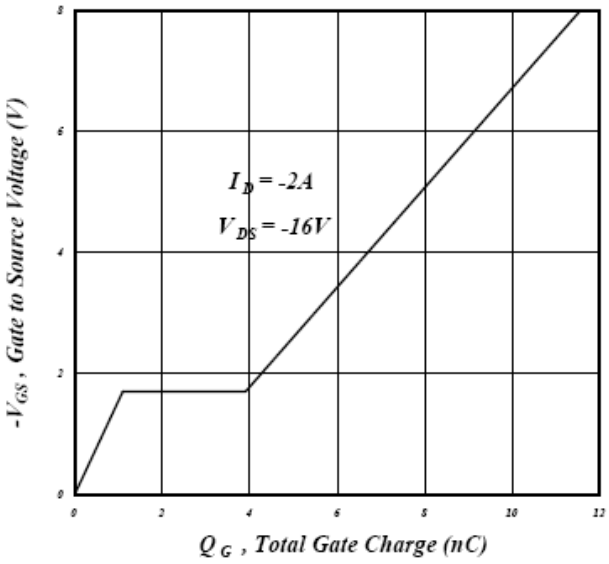


Fig 7. Gate Charge Characteristics

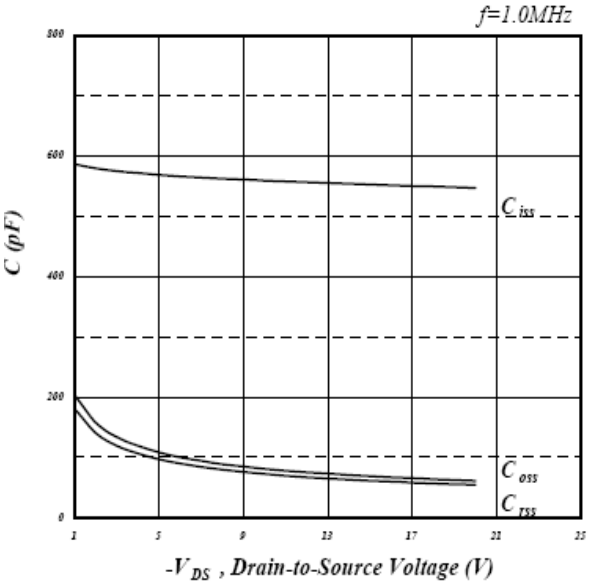


Fig 8. Typical Capacitance Characteristics

TYPICAL CHARACTERISTICS (P-Channel)

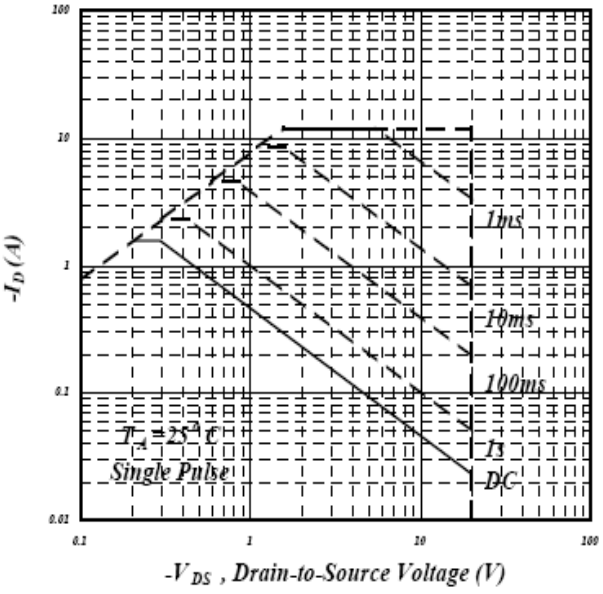


Fig 9. Maximum Safe Operating Area

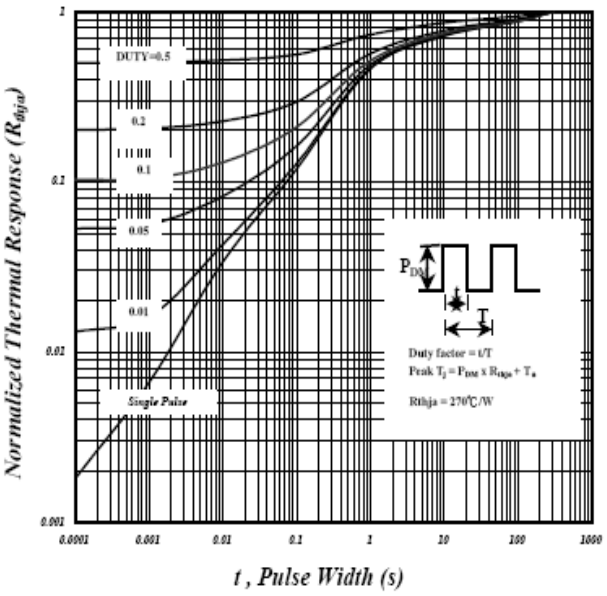
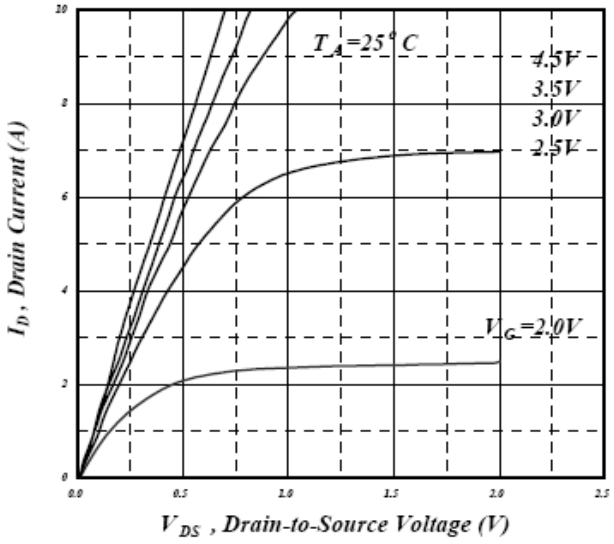


Fig 10. Effective Transient Thermal Impedance

TYPICAL CHARACTERISTICS (N-Channel)



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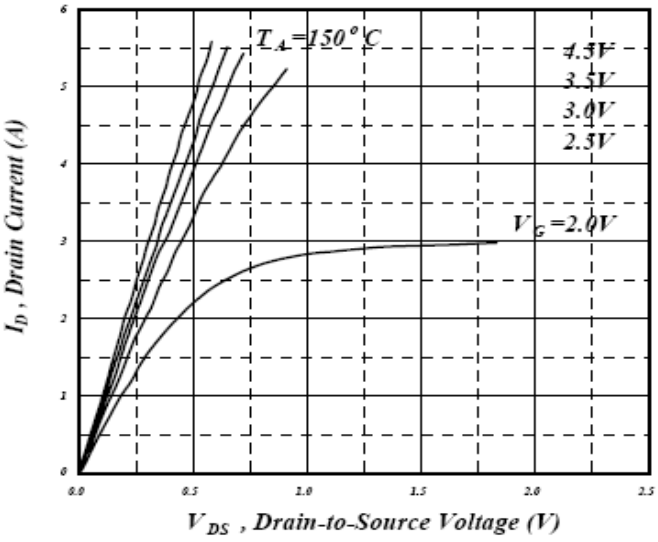


Fig 2. Typical Output Characteristics

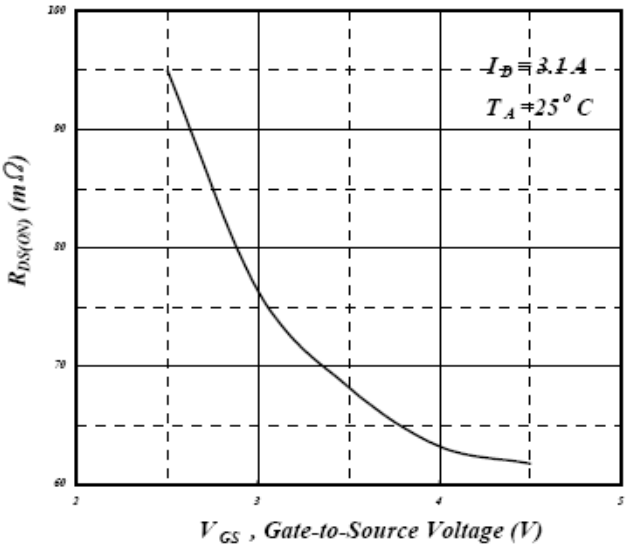


Fig 3. On-Resistance v.s. Gate Voltage

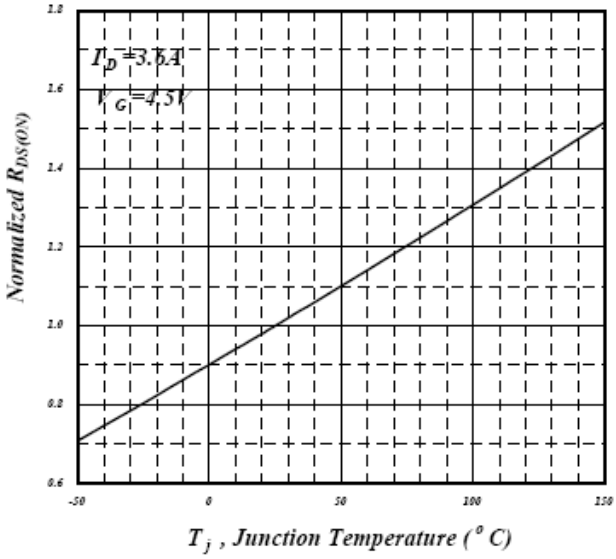
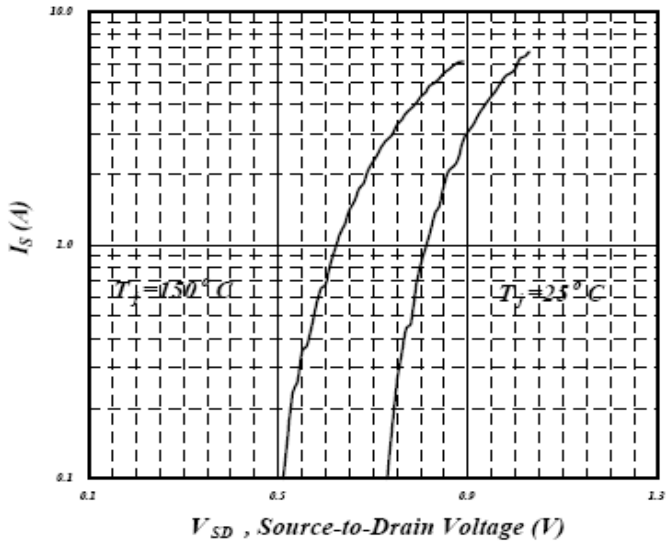


Fig 4. Normalized On-Resistance

TYPICAL CHARACTERISTICS (N-Channel)



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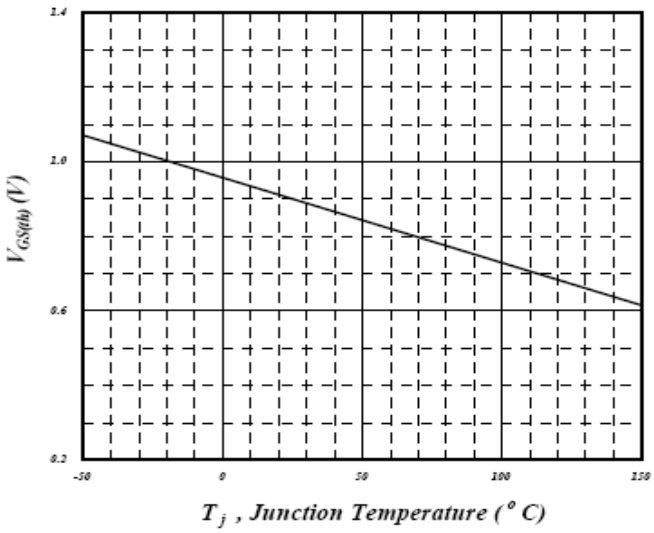


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

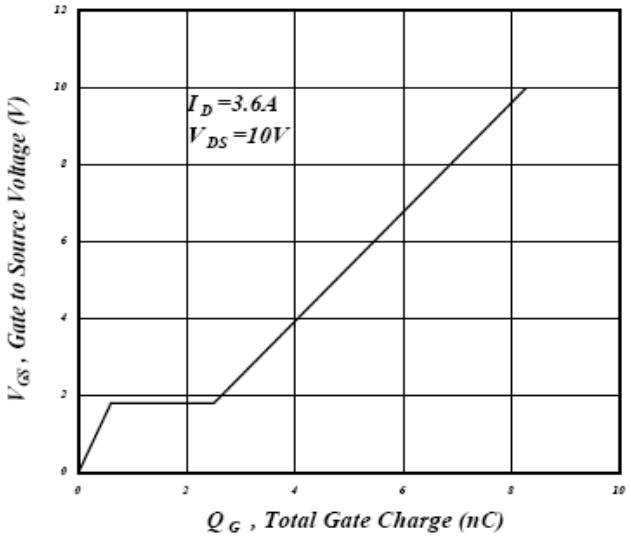


Fig 7. Gate Charge Characteristics

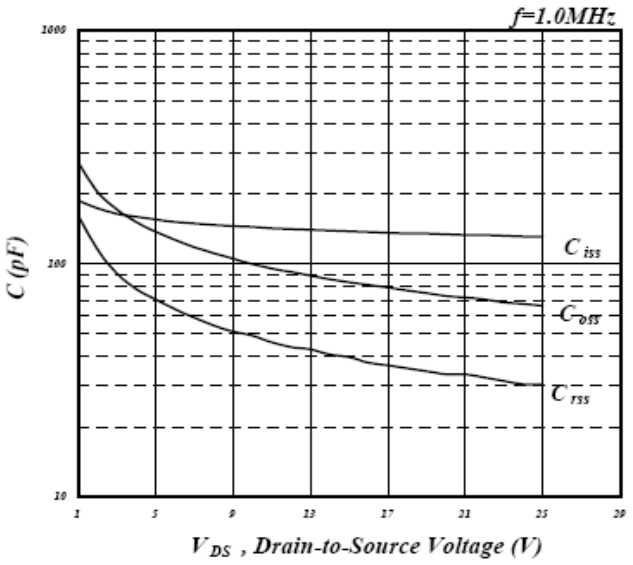
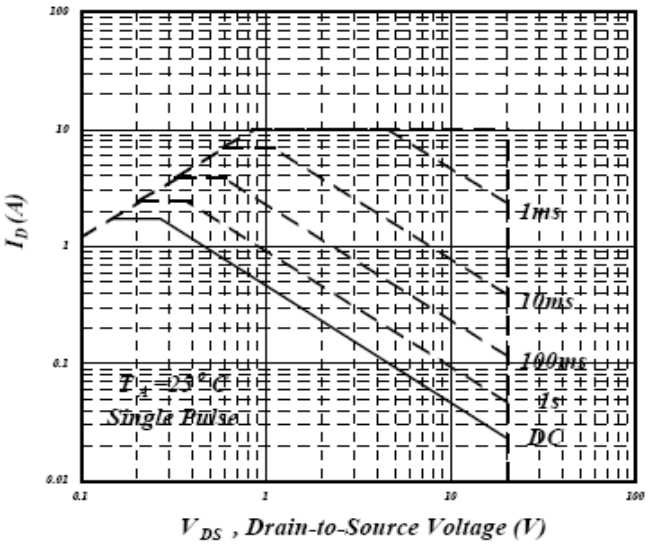


Fig 8. Typical Capacitance Characteristics

TYPICAL CHARACTERISTICS (N-Channel)



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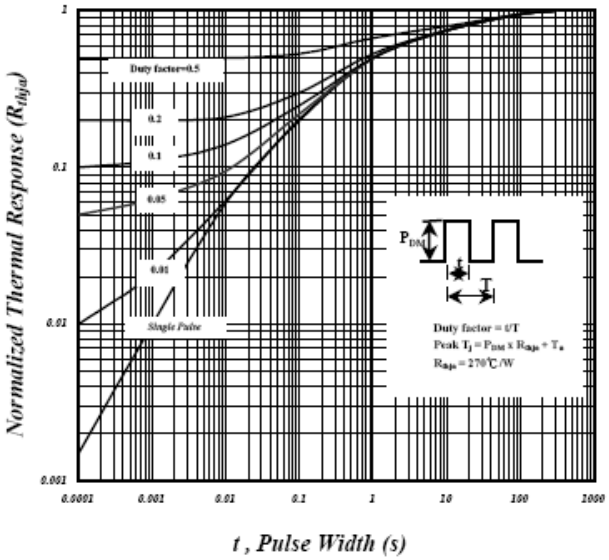

Fig 10. Effective Transient Thermal Impedance

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