SPC6606
N & P Pair Enhancement Mode MOSFET

DESCRIPTION

The SPC6606 is the N-Channel and P-Channel enhancement mode power field effect transistors which are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where high-side switching, low in-line power loss, and resistance to transients are needed.

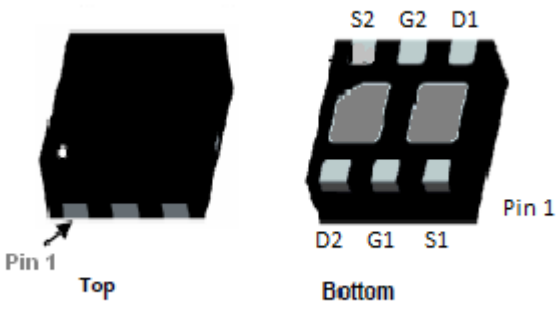
APPLICATIONS

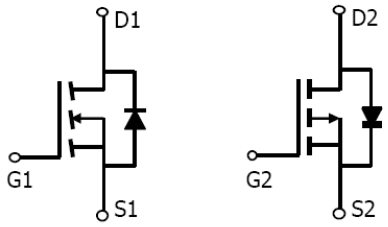
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

FEATURES

- N-Channel
  12V/4.0A,$R_{DS(ON)}$=26mΩ@V_{GS}=4.5V
  12V/3.0A,$R_{DS(ON)}$=35mΩ@V_{GS}=2.5V
  12V/2.0A,$R_{DS(ON)}$=50mΩ@V_{GS}=1.8V
- P-Channel
  -12V/-3.3A,$R_{DS(ON)}$=70mΩ@V_{GS}=-4.5V
  -12V/-2.8A,$R_{DS(ON)}$=85mΩ@V_{GS}=-2.5V
  -12V/-2.3A,$R_{DS(ON)}$=110mΩ@V_{GS}=-1.8V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- TDFN2x2-6L package design

PIN CONFIGURATION(TDFN2x2-6L)





n-channel p-channel

PART MARKING

Y : Year Code
W: Week Code

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PIN DESCRIPTION

Pin	Symbol	Description
1	S1	Source 1
2	G1	Gate 1
3	D2	Drain 2
4	S2	Source 2
5	G2	Gate 2
6	D1	Drain1

ORDERING INFORMATION

Part Number	Package	Part Marking
SPC6606TDN6RGB	TDFN2x2-6L	6606

※ Week Code : A ~ Z(1 ~ 26) ; a ~ z(27 ~ 52)
※ SPC6606TDN6RGB : Tape Reel ; Pb – Free ; Halogen -Free

ABSOULTE MAXIMUM RATINGS
(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical		Unit
			N-Channel	P-Channel	
Drain-Source Voltage		V_{DSS}	12	-12	V
Gate –Source Voltage		V_{GSS}	±8	±8	V
Continuous Drain Current(T_J=150℃)[a, b]	T_A=25℃	I_D	4.5	-4.3	A
	T_A=70℃		4.5	-3.8	
Pulsed Drain Current		I_{DM}	20	-15	A
Continuous Source Current(Diode Conduction)[b] T_A=25℃		I_S	1.6	-1.6	A
Power Dissipation[b]	T_A=25℃	P_D	1.9		W
	T_A=70℃		1.2		
Operating Junction Temperature		T_J	-55/150		℃
Storage Temperature Range		T_{STG}	-55/150		℃
Thermal Resistance-Junction to Ambient	T ≤ 5sec	$R_{\theta JA}$	65	65	℃/W
Thermal Resistance-Junction to Case	Steady State	$R_{\theta JC}$	16	16	

Notes:
A. Package limited.
B. Surface mounted on 1" x 1" FR4 board. t = 5s

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ELECTRICAL CHARACTERISTICS (T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions		Min.	Typ	Max.	Unit
Static							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D= 250uA	N-Ch	12			V
		V_{GS}=0V,I_D=-250uA	P-Ch	-12			
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	N-Ch	0.4		1.0	
		V_{DS}=V_{GS},I_D=-250uA	P-Ch	-0.4		-1.0	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±8V	N-Ch			100	nA
		V_{DS}=0V,V_{GS}=±8V	P-Ch			-100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}= 12V,V_{GS}=0V	N-Ch			1	uA
		V_{DS}=-12V,V_{GS}=0V	P-Ch			-1	
		V_{DS}= 12V,V_{GS}=0V T_J=55℃	N-Ch			10	
		V_{DS}=-12V,V_{GS}=0V T_J=55℃	P-Ch			-10	
On-State Drain Current	$I_{D(on)}$	V_{DS} ≤4.5V,V_{GS} =5V	N-Ch	15			A
		V_{DS}≤ -4.5V,V_{GS} =-5V	P-Ch	-10			
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=4.5V,I_D=4.0A	N-Ch			26	mΩ
		V_{GS}=-4.5V,I_D=-3.3A	P-Ch			70	
		V_{GS}=2.5V,I_D=3.0A	N-Ch			35	
		V_{GS}=-2.5V,I_D=-2.8A	P-Ch			85	
		V_{GS}=1.8V,I_D=2A	N-Ch			50	
		V_{GS}=-1.8V,I_D=-2.3A	P-Ch			110	
Forward Transconductance	gfs	V_{DS}=5V,I_D=3.5A	N-Ch		10		S
		V_{DS}=-5V,I_D=-3.5A	P-Ch		8.5		
Diode Forward Voltage	V_{SD}	I_S=1A,V_{GS}=0V	N-Ch			1	V
		I_S=-1.5A,V_{GS}=0V	P-Ch			-1.2	
Dynamic							
Total Gate Charge	Q_g	N-Channel V_{DS}=6V,V_{GS}=4.5V, I_D≡4.0A P-Channel V_{DS}=-6V,V_{GS}=-4.5V ,I_D≡-3A	N-Ch		8.6		nC
			P-Ch		10.1		
Gate-Source Charge	Q_{gs}		N-Ch		1.37		
			P-Ch		1.21		
Gate-Drain Charge	Q_{gd}		N-Ch		2.3		
			P-Ch		2.5		
Input Capacitance	Ciss	N-Channel V_{DS}=6V,V_{GS}=0V, f=1MHz P-Channel V_{DS}=-6V,V_{GS}=0V ,f=1MHz	N-Ch		510		pF
			P-Ch		595		
Output Capacitance	Coss		N-Ch		165		
			P-Ch		290		
Reverse Transfer Capacitance	Crss		N-Ch		105		
			P-Ch		255		
Turn-On Time	$t_{d(on)}$	N-Channel V_{DD}=6V,I_D=3.0A V_{GEN}=4.5V ,R_G=3.3Ω P-Channel V_{DD}=-6V,I_D=-4.0A V_{GEN}=-4.5V ,R_G=3.3Ω	N-Ch		5.2		nS
			P-Ch		5.6		
	t_r		N-Ch		34		
			P-Ch		32.2		
Turn-Off Time	$t_{d(off)}$		N-Ch		23		
			P-Ch		45.6		
	t_f		N-Ch		9.2		
			P-Ch		29.2		

TYPICAL CHARACTERISTICS (N-Channel)

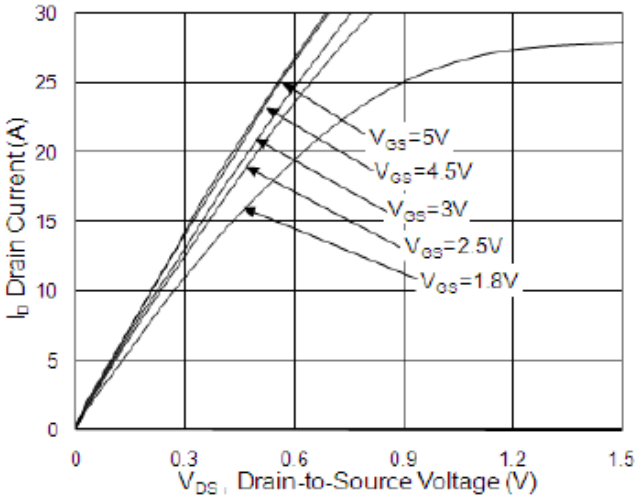

Fig. 1 Typical Output Characteristics

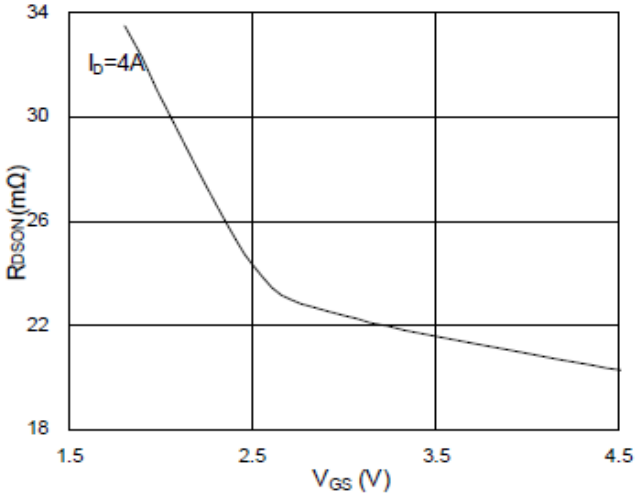

Fig. 2 On-Resistance vs. Gate Voltage

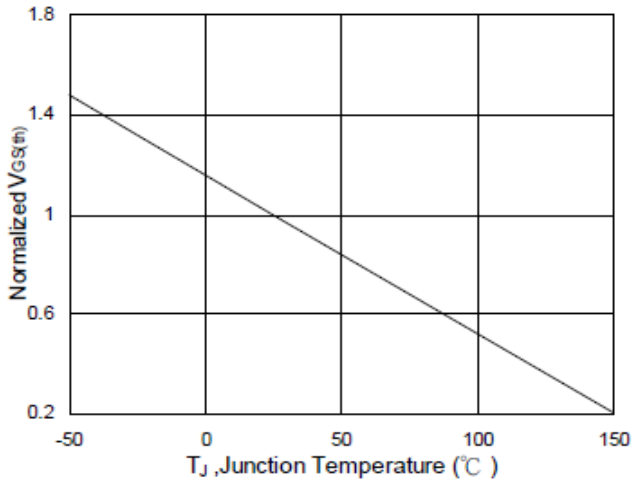

Fig. 3 Normalized Vgs(th) vs. Temperature

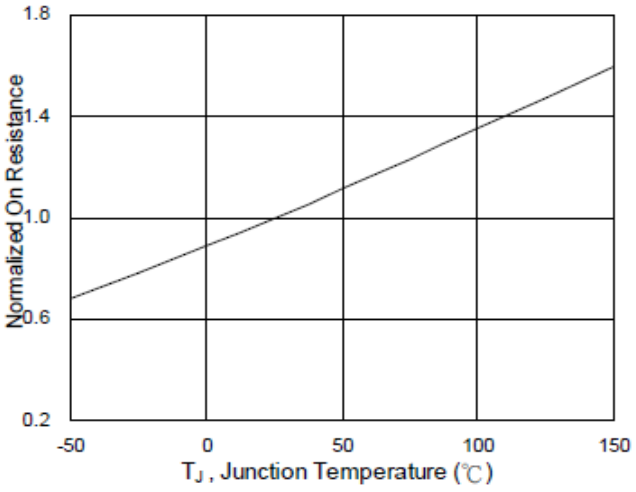

Fig. 4 Normalized On-Resistance vs. Temp

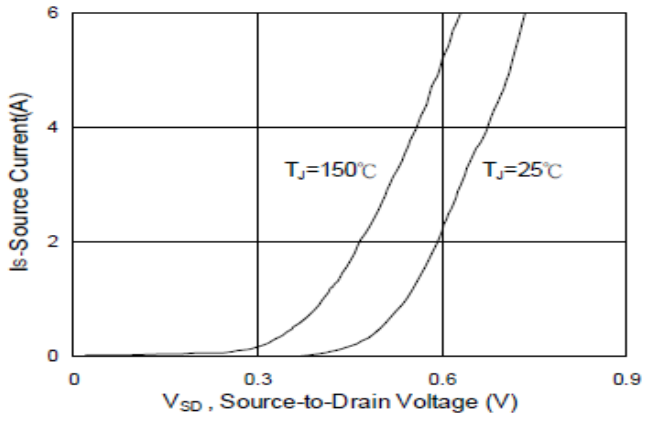

Fig. 5 Output Characteristics

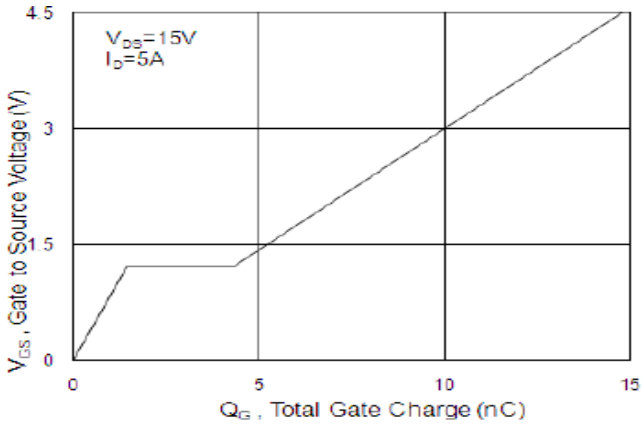

Fig. 6 Gate Charge Characteristics

TYPICAL CHARACTERISTICS (N-Channel)

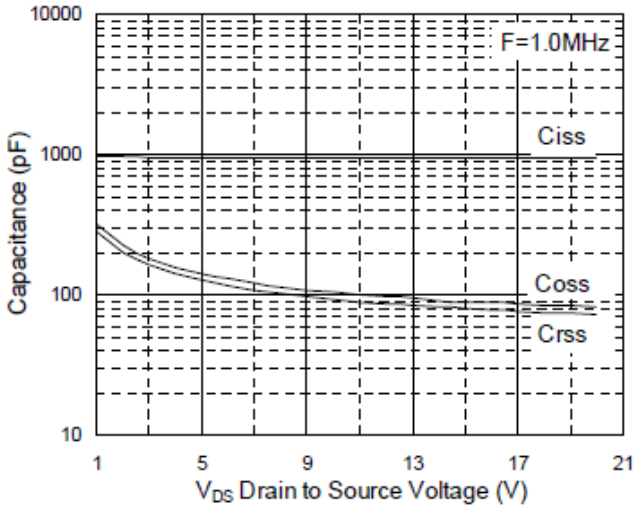

Fig 7 Capacitance vs. Drain Voltage

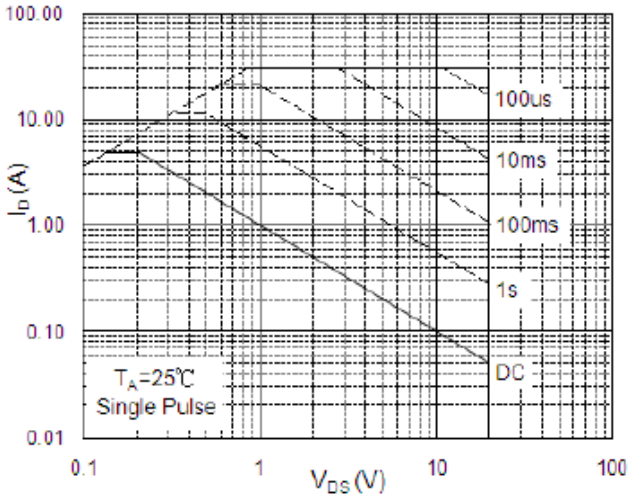

Fig. 8 Safe Operation Area

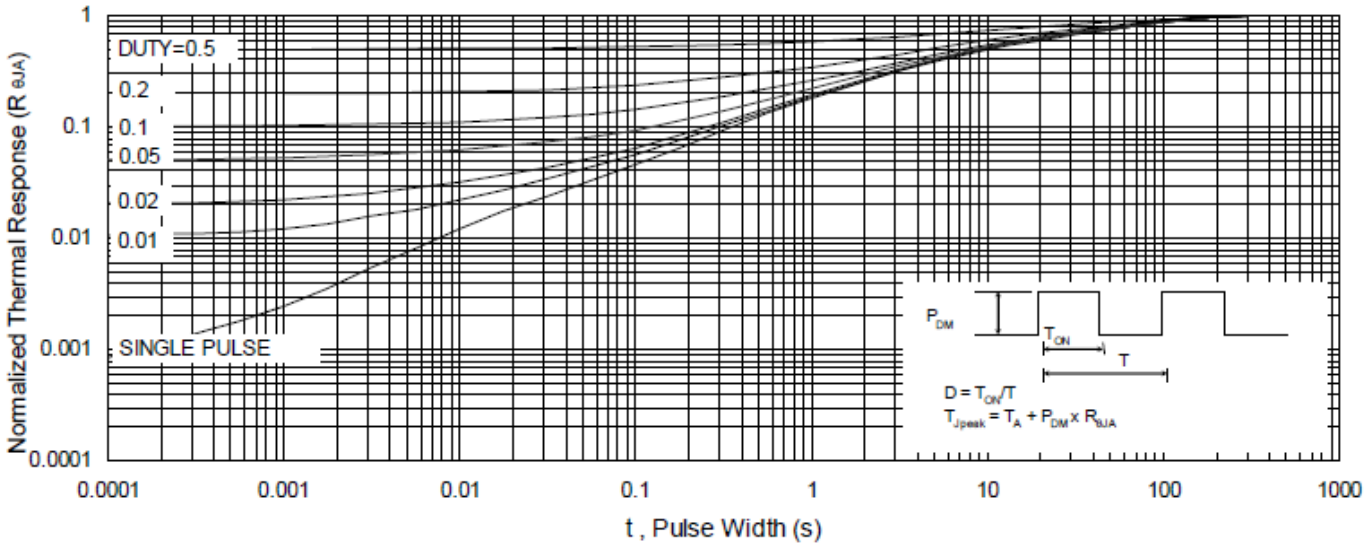

Fig. 9 Normalized Maximum Transient Thermal Impedance

TYPICAL CHARACTERISTICS (P-Channel)

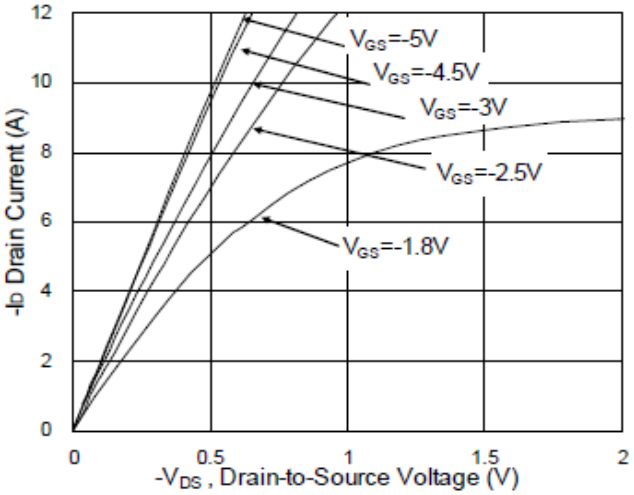

Fig. 10 Typical Output Characteristics

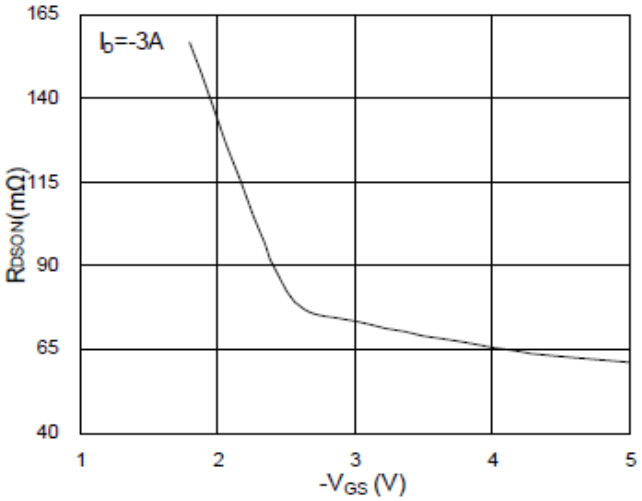

Fig. 11 On-Resistance vs. Gate Voltage

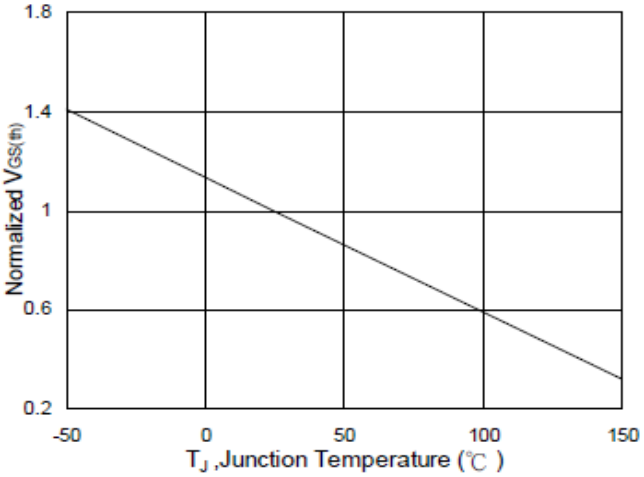

Fig. 12 Normalized Vgs(th) vs. Temp

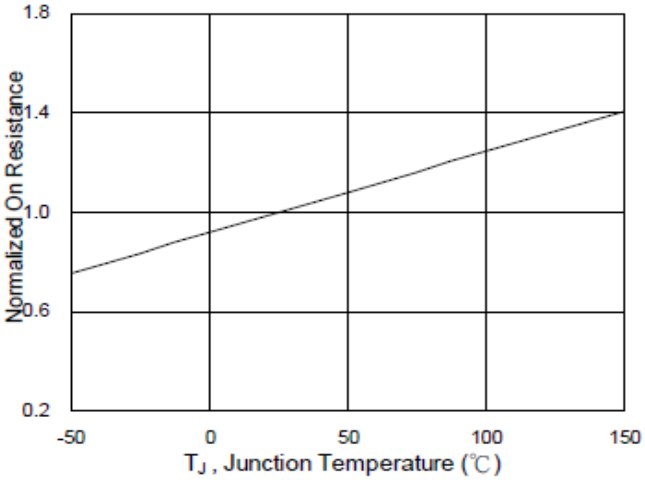

Fig. 13 Normalized On-Resistance vs. Temp

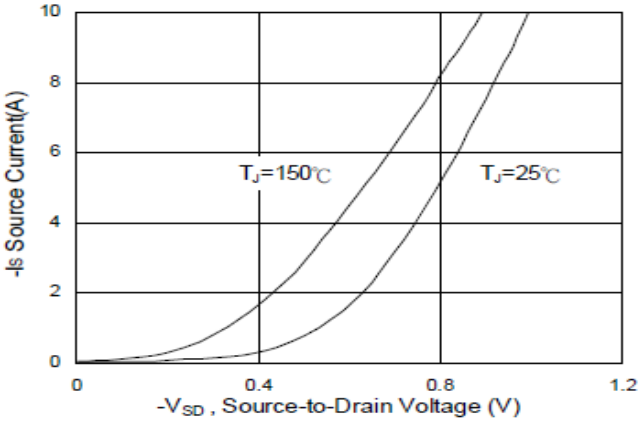

Fig. 14 Output Characteristics

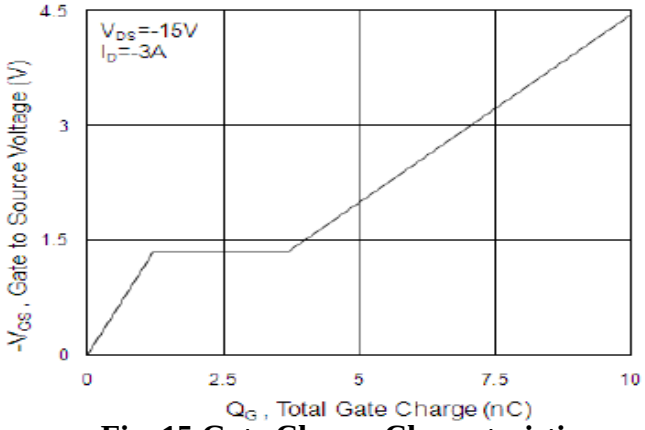

Fig. 15 Gate Charge Characteristics

TYPICAL CHARACTERISTICS (P-Channel)

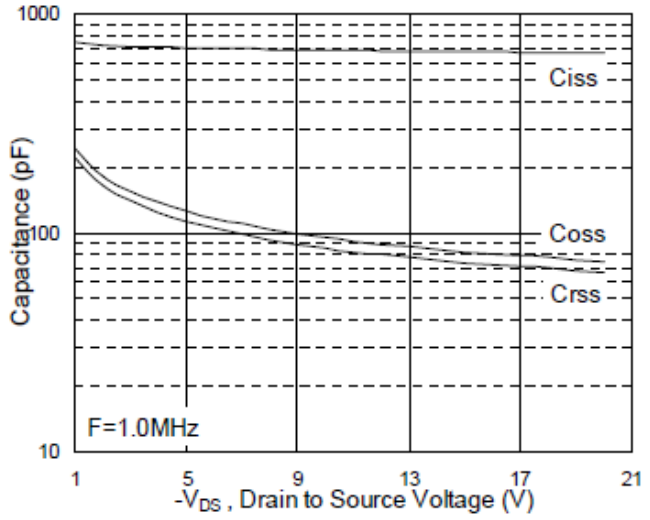

Fig 16 Capacitance vs. Drain Voltage

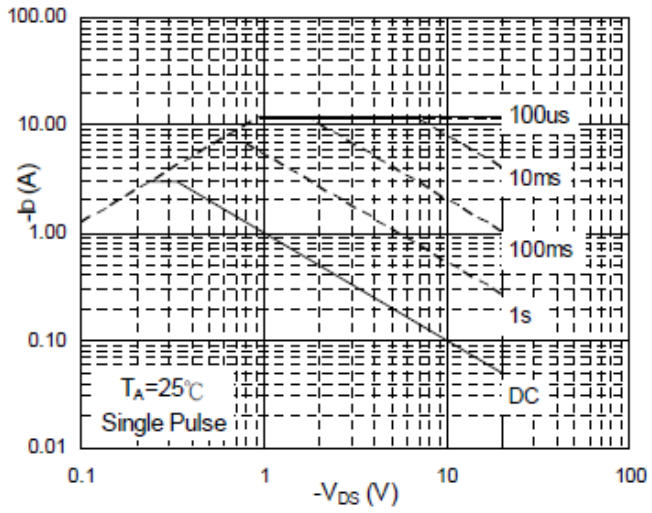

Fig. 17 Safe Operation Area

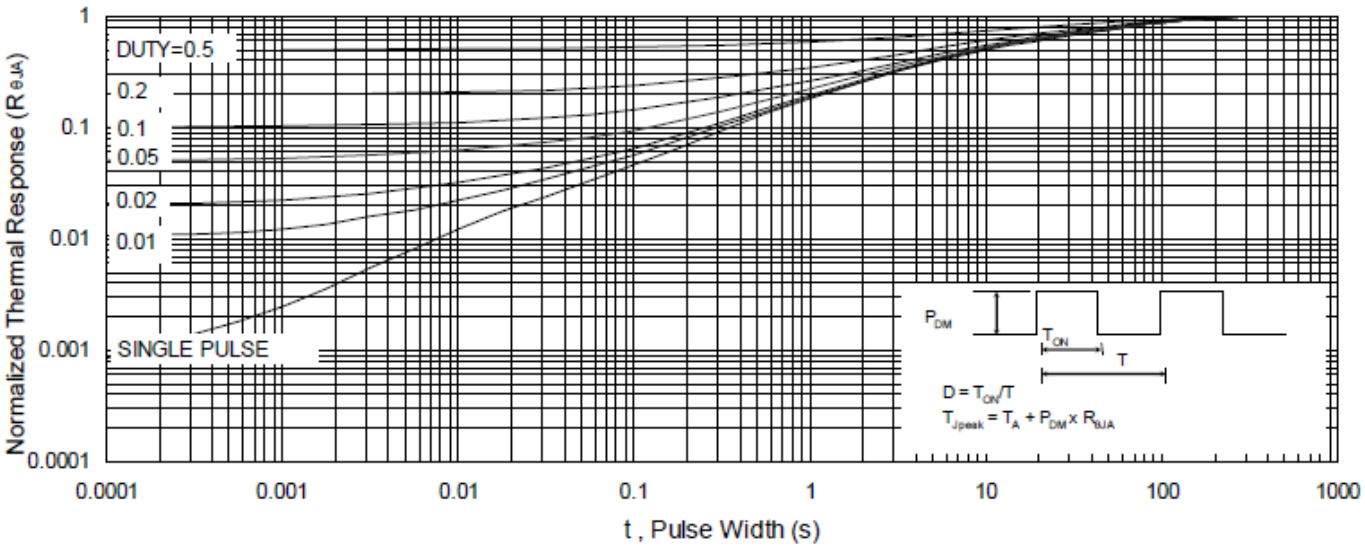

Fig. 18 Normalized Maximum Transient Thermal Impedance

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