

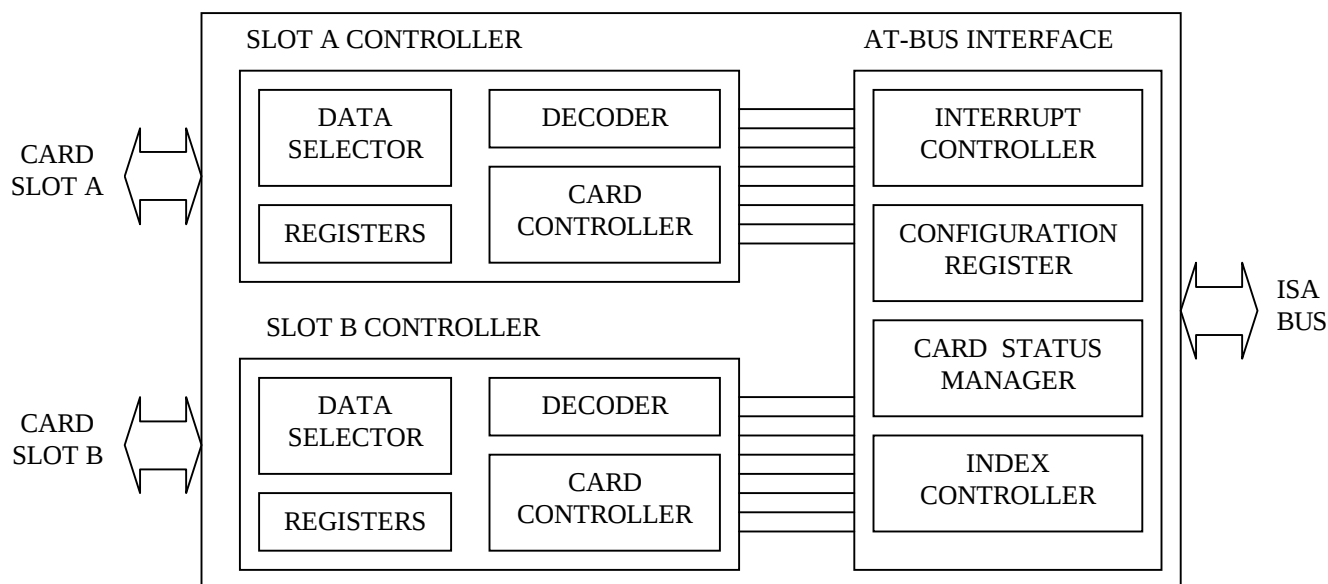
DESCRIPTION

The SPC8282F1A is a PCMCIA to ISA bus host adapter chip capable of controlling two PCMCIA sockets in accordance with PCMCIA-2.1 and JEIDA-4.1 standards. It's internal registers are 82365SL compatible. It supports 8-bit and 16-bit CPU's and PCMCIA devices. It provides programmable memory and I/O windowing as well as support for ATA (IDE) PCMCIA devices. It also incorporates programmable multi-mode power management and supports interrupt steering.

Complete Specification and a reference design (SDU8282#01) are also available.

FEATURES

- All host adapter functions in single chip.
- Direct connection to ISA (PC AT) bus.
- Direct connection to dual PCMCIA sockets.
- Dual socket interface using 208-pin PQFP.
- Five programmable memory windows per socket.
- Two programmable I/O windows per socket.
- 8 or 16 bit CPU interface.
- 8 or 16 bit PCMCIA support.
- Sockets configure-able for ATA disk interface.
- Programmable Interrupt steering.
- 3.3 V or 5.0 V operation.
- Fully compliant with PCMCIA-2.1 and JEIDA-4.1 plus DMA functions.
- Registers compatible with CL-PD7722.

TYPICAL SYSTEM DIAGRAM

SPC8282F1A

FALCONER

December 1997

EPSON**SPC8282F1A****PIN CONFIGURATION**

Pin #	Signal Name	Power	Pin #	Signal Name	Power	Pin #	Signal Name	Power	Pin #	Signal Name	Power
1	AVPPPGM	S	53	AA4	A	105	BA15	B	157	LA23	V
2	AVPPVCC	S	54	AWAIT#	A	106	BA23	B	158	IOCS16#	V
3	VPPVALID#	S	55	AA3	A	107	BA12	B	159	SBHE#	V
4	AVCC3#	S	56	AINPACK#	A	108	BA24	B	160	MEMCS16#	V
5	AVCC5#	S	57	AA2	A	109	BA7	B	161	SA0	V
6	A5VDET	S	58	AA1	A	110	BA25	B	162	SA1	V
7	B5VDET	S	59	ABVD2_SPKR#	A	111	GND	B	163	CLK (8MHz)	V
8	AREG#	A	60	AA0	A	112	BA6	B	164	SA2	V
9	AD3	A	61	ABVD1_STSCG#	A	113	BA5	B	165	SA3	V
10	ACD1#	A	62	AD0	A	114	BRESET	B	166	ALE	V
11	AD4	A	63	AD8	A	115	BA4	B	167	SA4	V
12	AD11	A	64	AD1	A	116	BWAIT#	B	168	SA5	V
13	AD5	A	65	AD9	A	117	BSLOTVCC2	B	169	SA6	V
14	AD12	A	66	AD2	A	118	BA3	B	170	IRQ3	V
15	AD6	A	67	AD10	A	119	BINPACK#	B	171	SA7	V
16	AD13	A	68	AWP_IOCS16#	A	120	BA2	B	172	IRQ4	V
17	AD7	A	69	ACD2#	A	121	BA1	B	173	SA8	V
18	AD14	A	70	GND	A	122	BBVD2_SPKR#	B	174	IRQ5	V
19	ACE1#	A	71	BREG#	B	123	BA0	B	175	SA9	V
20	AD15	A	72	BD3	B	124	BBVD1_STCHG#	B	176	SA10	V
21	AA10	A	73	BCD1#	B	125	BD0	B	177	IRQ7	V
22	ACE2#	A	74	BD4	B	126	BD8	B	178	SA11	V
23	AOE#	A	75	BD11	B	127	BD1	B	179	SA12	V
24	ASLOTVCC2	A	76	BD5	B	128	BD9	B	180	REFRESH#	V
25	AA11	A	77	BD12	B	129	BD2	B	181	SA13	V
26	AIORD#	A	78	BD6	B	130	BD10	B	182	SA14	V
27	VDD (5V)	A	79	GND	B	131	BWP_IOCS16#	B	183	SA15	V
28	AA9	A	80	BD13	B	132	BCD2#	B	184	SA16	V
29	AIOWR#	A	81	BD7	B	133	VDD (5V)	I	185	IOR#	V
30	AA8	A	82	BD14	B	134	SD15	I	186	IOW#	V
31	GND	A	83	BCE1#	B	135	SD14	I	187	AE#	V
32	AA17	A	84	BD15	B	136	SD13	I	188	IOCHRDY	V
33	AA13	A	85	BA10	B	137	SD12	I	189	SD0	V
34	AA18	A	86	BCE2#	B	138	ISAVCC	I	190	SD1	V
35	AA14	A	87	BOE#	B	139	SD11	I	191	OWS#	V
36	AA19	A	88	BSLOTVCC1	B	140	GND	I	192	GND	V
37	AWE#	A	89	BA11	B	141	SD10	I	193	SD2	V
38	AA20	A	90	BIORD#	B	142	SD9	I	194	SD3	V
39	ARDY_IREQ#	A	91	BA9	B	143	SD8	I	195	ISAVCC	V
40	AA21	A	92	BIOWR#	B	144	MEMW#	I	196	SD4	V
41	AA16	A	93	BA8	B	145	MEMR#	I	197	SD5	V
42	AA22	A	94	BA17	B	146	LA17	I	198	IRQ9	V
43	AA15	A	95	BA13	B	147	LA18	I	199	SD6	V
44	AA23	A	96	BA18	B	148	IRQ14	I	200	SD7	V
45	AA12	A	97	BA14	B	149	LA19	I	201	PWRGOOD	V
46	AA24	A	98	BA19	B	150	IRQ15	I	202	SPKOUT#_CSEL	V
47	AA7	A	99	BWE#	B	151	LA20	I	203	INTR#	V
48	AA25	A	100	BA20	B	152	IRQ12	I	204	BVPPPGM	S
49	AA6	A	101	BRDY/IREQ#	B	153	LA21	I	205	BVPPVCC	S
50	AA5	A	102	BA21	B	154	IRQ11	I	206	BVCC3#	S
51	ARESET	A	103	BA16	B	155	LA22	I	207	BVCC5#	S
52	ASLOTVCC1	A	104	BA22	B	156	IRQ10	I	208	SYSTEM VCC(5V)	S

LEGEND

S SYSTEM VCC

A A SLOT VCC

B B SLOT VCC

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RECOMMENDED OPERATING CONDITIONS

The SPC8282F1A has five power supply systems as follows:

System Control:	SYSTEM VCC (+5VDC recommended)
ISA Bus Interface:	ISAVCC (+5VDC recommended for most case)
SLOT A Interface:	A_SLOTVCC
SLOT B Interface:	B_SLOTVCC
Chip Core	VDD (+5VDC only)

SLOT A Interface and SLOT B Interface power supply may operate at LVDD (3.3 V TYP) or HVDD (5.0 V TYP). Recommended operating parameters are shown in the following tables:

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Supply Voltage - high	HVDD	VSS = 0 V	4.5	5.0	5.5	V
Supply Voltage - low	LVDD	VSS = 0 V	3.0	3.3	3.6	V
Input Voltage	VIN	VSS = VSS	VSS		VDD	V
Operating Temperature	TOPR		-40	25	85	°C

7.3 INPUT DC SPECIFICATIONS

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Input High Voltage 1 ^a	V _{IH1}	VDD = HVDD MAX	2.0			V
		VDD = LVDD MAX	1.8			V
Input Low Voltage 1 ^a	V _{IL1}	VDD = HVDD MIN			0.8	
		VDD = LVDD MIN			0.5	V
Input High Voltage 2 ^b	V _{IH2}	VDD = HVDD MAX	3.5			V
		VDD = LVDD MAX	2.2			V
Input Low Voltage 2 ^b	V _{IL2}	VDD = HVDD MIN			1.0	V
		VDD = LVDD MIN			0.8	

^a Specification applies to all input pins and input sections of all I/O pins except for CD2# and CD1#.

^b Specification applies to pins CD2# and CD1# only.

7.4 OUTPUT DC SPECIFICATIONS

Parameter	Symbol	Conditions	MIN	MAX	Unit
Output High Voltage 1 ^a	VOH1	VDD = HVDD MIN, IOH1 = - 4 mA	HVDD - 0.4		V
		VDD = LVDD MIN, IOH1 = - 2 mA	LVDD - 0.3		V
Output Low Voltage 1 ^a	VOL1	VDD = HVDD MIN, IOL1 = 4 mA		VSS + 0.4	V
		VDD = LVDD MIN, IOL1 = 2 mA		VSS + 0.3	V
Output High Voltage 2 ^b	VOH2	VDD = HVDD MIN, IOH1 = - 12 mA	HVDD - 0.4		V
		VDD = LVDD MIN, IOH1 = - 6 mA	LVDD - 0.3		V
Output Low Voltage 2 ^b	VOL2	VDD = HVDD MIN, IOL1 = 12 mA		VSS + 0.4	V
		VDD = LVDD MIN, IOL1 = 6 mA		VSS + 0.3	V

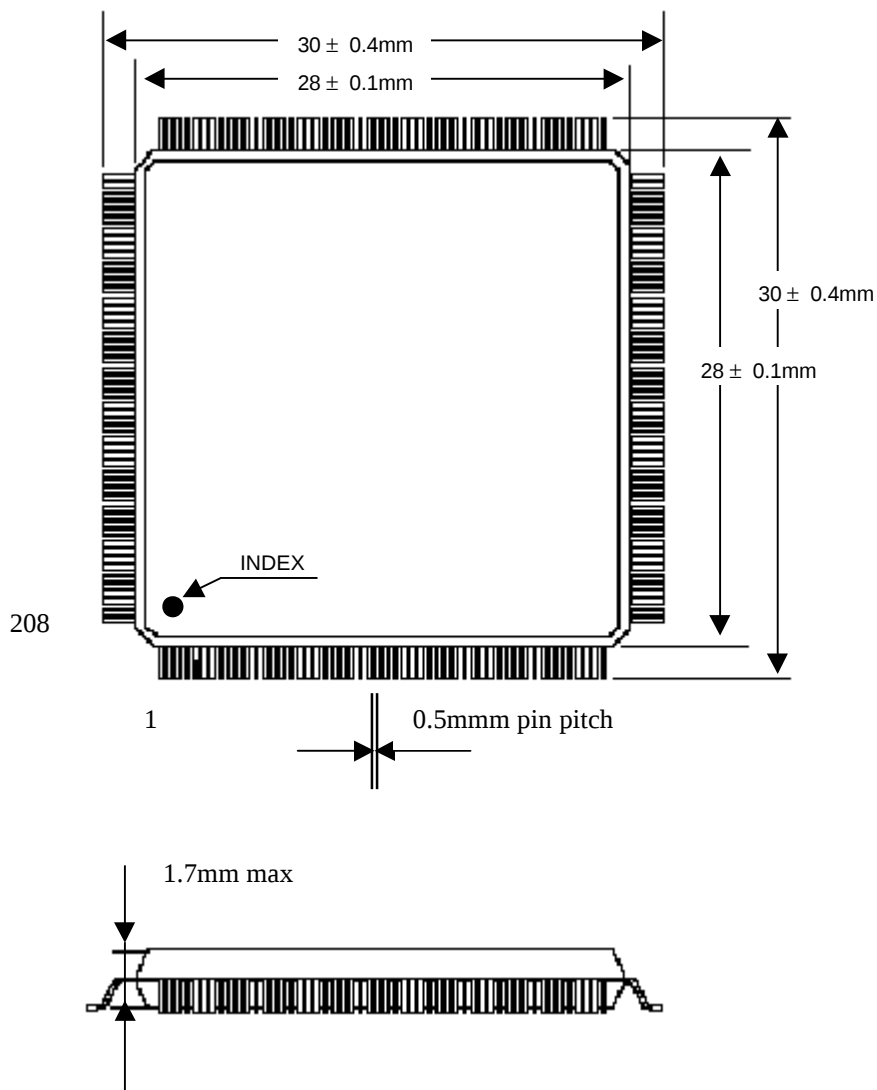
^a Specification applies to all 2/ 4 mA drive output pins and output section of the 16 bit card data bus I/O pins, D[15:0]

^b Specification applies to all 6/12 mA drive output pins and the output section of ISA data bus (SD[15:0]) and SPKROUT# I/O pins.

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MECHANICAL DATA (Package Dimension)

Plastic LQFP 208pin body size 28 x 28 x 1.4mm (LQFP22)



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