DATA SHEET

SPCA1528A

Digital Still Camera Controllers

Preliminary

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Version 0.3 (Draft)

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Digital Still Camera Controllers

1.GENERAL DESCRIPTION

1.1. Introduction

The SPCA1528A is a low cost digital still camera SoC, which features with a full set of components required in a digital still camera system. The SoC has embedded with Sunplus high quality image processing engine, high- speed JPEG CODEC and a wide range of peripheral interfaces, making a low cost DSC easy to be realized.

1.2. Terminology

AE:	Automatic Exposure
AWB:	Automatic White Balance
CODEC:	Encoder and Decoder
Color DSP:	Color image Digital Signal Processor
DMA:	Direct Memory Access
I2C:	Inter IC Control
ISP:	In System Programming
LCM:	Liquid Crystal display Module
MMC:	Multi Media Card
PLL:	Phase Lock Loop
SD:	Secure Digital card
UART:	Universal Asynchronous Receiver Transmitter
USB:	Universal Serial Bus
VGA:	Video Graphics ArrayTV game product

2.FEATURE

2.1. CPU

- 8032 with 8KB Data Memory and 2KB Program Memory
- Support ISP (In-System-Programming) function via USB
- Program code shadowing function to SDRAM
- External NOR-type Flash up to 1MB

2.2. Peripheral

- 1 UART port
- USB 2.0 high speed with on-chip PHY
- Two PWM ports
- Three timers
- 3-channel general purpose ADC
- GPIOs

2.3. Memory Interface

- Support SDRAM with density of 16Mb to 512Mb
- Programmable DRAM operating frequencies up to 96MHz
- Support down grade SDRAM

2.4. Storage Media Interface

- Supports NAND-type flash memory and serial flash memory
- Support MMC and SD memory cards

2.5. Sensor

- Support all popular CMOS image sensors
- Image resolution from 2M pixels to 5 M pixels
- Support Digital TV Input, CCIR601 (8-bit data bus) and CCIR656
- I2C serial control port for sensor parameter settings
- Accurate flash light control at pixel level
- Mechanical shutter control

2.6. Display

- Supports Digital LCD Display Interface for Casio, AUO, Sony, and TOPPOLY
- Supports ITU-R BT 601 digital video output interface
- Built-in TV encoder to support direct output analog NTSC or PAL composite video signals
- Programmable luminance(Contrast, Brightness) and chrominance(Hue, Saturation) control for display
- Support font-based OSD
- Support 8/9 bits LCM interface

2.7. Color DSP

- Support RGB Bayer patterns output and YUV422 output sensor.
- Support both master mode and slave mode CMOS sensors.
- Programmable frame rate.
- On-chip color processing engine
- AWB window statistics
  - 2-D edge enhancement
  - Luminance histogram
  - Hue/Saturation adjustment
- Brightness/Contrast adjustment
  - Programmable edge enhancement
- Bad pixel concealment can be done by hard-wired engine or by the user-defined firmware.
- Fully programmable Gamma table
- Lens shade compensation
- Support special image effects such as negative, Solaris, emboss, binaries, sepia, black/white.

2.8. Still Image and Video Compression

- Motion JPEG 640x480 (VGA) resolution CODEC up to 30 fps

2.9. USB

- USB 2.0 Full/High Speed function with built-in USB2.0 transceiver
- Supports USB mass storage, audio, video, and still image

2.10. Audio

- IMA ADPCM audio CODEC
- Built-in mono audio ADC for microphone input
- Mono PWM DAC with external amplifier to support speaker

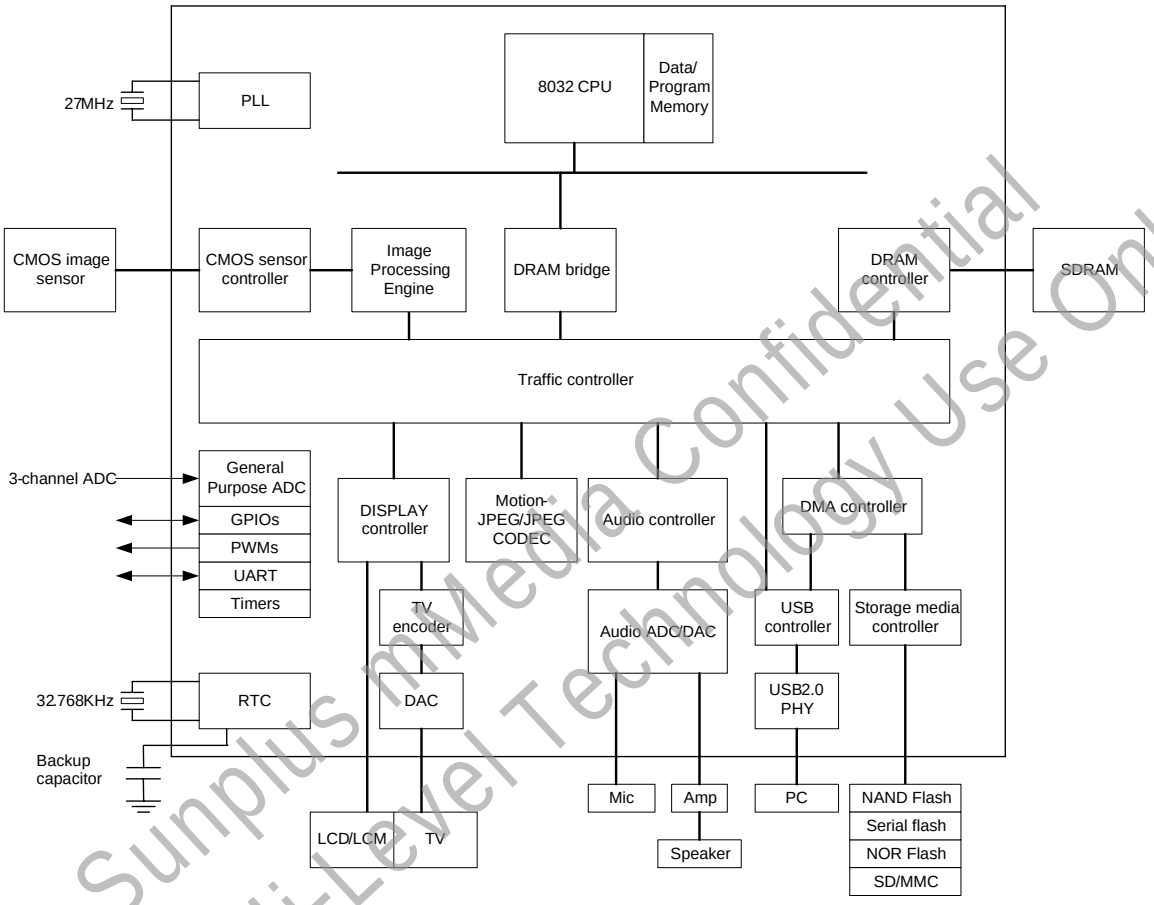
2.11. Package and Power

- 3.3V IO power supply
- 1.8V core power supply
- 128-pin/176-pin LQFP package

3. BLOCK DIAGRAM

3.1. Block Diagram

The following diagram shows the internal structure of SPCA1528A and a typical connection to the external devices.



3.2. Function Description

CMOS Sensor controller

The sensor interface connects to CMOS sensors. It can also connect to a video decoder to capture video. A serial interface is used to program CMOS sensors.

RTC

The RTC module enables the SPCA1528A to maintain the calendar function with minimum power consumption.

PLL

The SPCA1528A has an on-chip PLL that allows the use of a minimum number of crystals in user applications. Major internal clocks can be generated with a single 27MHz crystal.

8032 CPU

The built-in 8032 CPU coordinates camera operation.

DISPLAY Controller

This module has integrated a variety of digital interfaces, which include TFT LCD interface, LCM interface, It also integrates a TV encoder, supporting both NTSC and PAL composite video outputs. The OSD function is also implemented in this module.

Image Processing Engine

The Image processing engine of the SPCA1528A is a very flexible pipeline. It will perform color interpolation, gamma correction, image scaling for digital zoom, and image enhancement filtering. It also has real-time AF/AE/AWB statistic engines to provide data for computing the optimal control parameters. All the functions are controlled by a set of programmable registers, allowing users to fine-tune the image quality.

JPEG CODEC

This image compression engine can generate JPEG compressed

files in JFIF and EXIF format with firmware support. The engine can also decode JPEG compressed images for playback.

DRAM Controller

The DRAM controller provides an access path to the SDRAM for other internal modules of the SPCA1528A. Many special functions are also implemented in this module. For example, image scaling, copy and paste of image parts, image rotation, … etc.

DMA Controller

The DMA controller allows high-speed data transfers between SPCA1528A internal modules.

Storage Media Controller

The storage interface controller is a high efficiency bridge between different storage media protocol and the internal bus. Both DMA data transfers and PIO data transfers are supported.

USB2.0 High Speed Controller

The USB controller supports USB2.0 full speed and high speed data transfer. A high performance USB2.0 PHY is integrated. SPCA1528A supports all types of USB pipes, including control, bulk, ISO and interrupt pipes. Totally, eight USB endpoints are implemented in SPCA1528A controller. The following table summarizes the functions of each endpoint.

Endpoint	Function
0	Control endpoint as default pipe
1	Video ISO IN endpoint
2	Bulk IN endpoint for MSDC
3	Bulk OUT endpoint for MSDC
4	Interrupt IN endpoint for SIDC
5	Interrupt IN endpoint for audio status
6	ISO IN endpoint for audio data
7	Interrupt IN endpoint for debugging

4. PIN DESCRIPTIONS

4.1. Pin Descriptions

4.1.1. CPU Interface

No.	Hex.	Dir.	Description		
1	Psen	B	Program space enable This pin is an output pin when the built-in CPU is enabled. When external CPU is used, this pin is an input pin.		
2	romwrnn	O	External write pulse. This pin is used in the ISP (in-system-programming) function		
3	p00	B	CPU port 0, address/data multiplex pin, bit 0.		
4	p01	B	CPU port 0, address/data multiplex pin, bit 1.		
5	p02	B	CPU port 0, address/data multiplex pin, bit 2.		
6	p03	B	CPU port 0, address/data multiplex pin, bit 3.		
7	p04	B	CPU port 0, address/data multiplex pin, bit 4.		
8	p05	B	CPU port 0, address/data multiplex pin, bit 5.		
9	p06	B	CPU port 0, address/data multiplex pin, bit 6.		
10	p07	B	CPU port 0, address/data multiplex pin, bit 7.		
			Default function	Alternative function	
11	p10	B	CPU address bit 0	CPU port 1, bit 0.	
12	p11	B	CPU address bit 1	CPU port 1, bit 1.	
13	p12	B	CPU address bit 2	CPU port 1, bit 2.	
14	p13	B	CPU address bit 3	CPU port 1, bit 3.	
15	p14	B	CPU address bit 4	CPU port 1, bit 4.	
16	p15	B	CPU address bit 5	CPU port 1, bit 5.	
17	p16	B	CPU address bit 6	CPU port 1, bit 6.	
18	p17	B	CPU address bit 7	CPU port 1, bit 7.	
19	p20	B	CPU port 2, high byte address, bit 0.		
20	p21	B	CPU port 2, high byte address, bit 1.		
21	p22	B	CPU port 2, high byte address, bit 2.		
22	p23	B	CPU port 2, high byte address, bit 3.		
23	p24	B	CPU port 2, high byte address, bit 4.		
24	p25	B	CPU port 2, high byte address, bit 5.		
25	p26	B	CPU port 2, high byte address, bit 6.		
26	p27	B	CPU port 2, high byte address, bit 7.		

4.1.2. Storage media interface

No.	Hex.	Dir.	Description				
			Nand-gate	Serial-Flash	SD/MMC	Alternative function	
1	fmgpio0	B	CE/ (O)	CE(O)		Probe2_0	
2	fmgpio1	B	RDY (I)	SI (I)		Probe2_1	
3	fmgpio2	B	ALE (O)	SCK(O)		Probe2_2	
4	fmgpio3	B	CLE (O)	SO(O)		Probe2_3	
5	fmgpio4	B			CLK (O)	Probe2_4	
6	fmgpio5	B			DAT0 (B)	Probe2_5	
7	fmgpio6	B	WP/ (O)		DAT1 (B)	Probe2_6	
8	fmgpio7	B	RE/ (O)		DAT2 (B)	Probe2_7	

No.	Hex.	Dir.	Description				
9	fmgpio8	B	WE/ (O)		DAT3 (B)		
10	fmgpio9	B			CMD (B)		
11	fmgpio10	B	D0 (B)				
12	fmgpio11	B	D1 (B)				
13	fmgpio12	B	D2 (B)				
14	fmgpio13	B	D3 (B)				
15	fmgpio14	B	D4 (B)				
16	fmgpio15	B	D5 (B)				
17	fmgpio16	B	D6 (B)				
18	fmgpio17	B	D7 (B)				

4.1.3. System

No.	Hex.	Dir.	Description	
1	Testmode	I	testmode	
2	Lvdi	I	Low power detect input	
3	xvss	PG	Crystal pad ground	
4	xtal27i	I	27MHz crystal pad input	
5	xtal27o	O	27MHz crystal pad output	
6	cp	I	RC filter input to audio PLL	
7	xvdd	PG	Crystal pad power	3.3V

4.1.4. AUDIO/SAR

No.	Hex.	Dir.	Description	
1	AVDD	PG	3.3V power for ADC	
2	AVSS	PG	Ground for ADC	
3	VREFF	O	Reference voltage for ADC	
4	MICBIAS	O	Buffered voltage output suitable for electro-microphone-capsule biasing.	
5	SAR0	I	SAR ADC channel I.	
6	SAR1	I	SAR ADC channel II.	
7	SAR2	I	SAR ADC channel III.	3.3V
8	MICINP	I	Microphone positive input.	
9	MICINN	I	Microphone negative input.	
10	ADFLT	O	Anti-aliasing filter cap for ADC.	

4.1.5. SDRAM interface

No.	Hex.	Dir.	Description	
1	sdclk	O	SDRAM clock	
2	rasnn	O	SDRAM raw address strobe signal	
3	casnn	O	SDRAM column address strobe signal	
4	mwenn	O	SDRAM write enable signal	
5	ldqm	O	SDRAM data mask signal, low byte	

No.	Hex.	Dir.	Description				
6	udqm	O	SDRAM data mask signal, high byte				
7	cke	O	SDRAM clock enable signal				3.3V
8	md0	B	SDRAM data bus, bit 0				
9	md1	B	SDRAM data bus, bit 1				
10	md2	B	SDRAM data bus, bit 2				
11	md3	B	SDRAM data bus, bit 3				
12	md4	B	SDRAM data bus, bit 4				
13	md5	B	SDRAM data bus, bit 5				
14	md6	B	SDRAM data bus, bit 6				
15	md7	B	SDRAM data bus, bit 7				
16	md8	B	SDRAM data bus, bit 8				
17	md9	B	SDRAM data bus, bit 9				
18	md10	B	SDRAM data bus, bit 10				
19	md11	B	SDRAM data bus, bit 11				
20	md12	B	SDRAM data bus, bit 12				
21	md13	B	SDRAM data bus, bit 13				
22	md14	B	SDRAM data bus, bit 14				
23	md15	B	SDRAM data bus, bit 15				
24	ma0	B	SDRAM address bus, bit 0. The bus is also used for IO-trap. During IO-trap stage, the “ma” bus is an input bus. After the IO-trap stage, the bus is an output bus.				
25	ma1	B	SDRAM address bus, bit 1				
26	ma2	B	SDRAM address bus, bit 2				
27	ma3	B	SDRAM address bus, bit 3				
28	ma4	B	SDRAM address bus, bit 4				
29	ma5	B	SDRAM address bus, bit 5				
30	ma6	O	SDRAM address bus, bit 6				
31	ma7	O	SDRAM address bus, bit 7				
32	ma8	O	SDRAM address bus, bit 8				
33	ma9	O	SDRAM address bus, bit 9				
34	ma10	O	SDRAM address bus, bit 10				
35	ma11	O	SDRAM address bus, bit 11				
			16M bit	64M bit	128M bit	256M/512M bit	
36	ma12	O	BA	BA0	BA0	BA0	
37	ma13	O	NC	BA1	BA1	BA1	
38	ma14	O	NC	NC	NC	A12	

4.1.6. Digital TV interface

No.	Hex.	Dir.	Description				
			CCIR601	LCD	LCM	PROBE	
1	digtv0	B	DDX0	DDX0	D0	Probe1_0	
2	digtv1	B	DDX1	DDX1	D1	Probe1_1	
3	digtv2	B	DDX2	DDX2	D2	Probe1_2	
4	digtv3	B	DDX3	DDX3	D3	Probe1_3	

No.	Hex.	Dir.	Description				
5	digtv4	B	DDX4	DDX4	D4	Probe1_4	
6	digtv5	B	DDX5	DDX5	D5	Probe1_5	
7	digtv6	B	DDX6	DDX6	D6	Probe1_6	
8	digtv7	B	DDX7	DDX7	D7	Probe1_7	
9	digtv8	B		DEM	RD		
10	digtv9	B	VSYNC	VSD	CS		
11	digtv10	B	HSYNC	HSD	A0		
12	digtv11	B	DCLK	DCLK	WR		
13	digtv12	B	DDX8		D8		

4.1.7. USB interface

No.	Hex.	Dir.	Description	
1	uvdd	PG	USB transceiver analog power.	3.3V
2	dp	B	USB data plus.	
3	dm	B	USB data minus.	
4	uvss	PG	USB transceiver analog ground.	
5	rext	O	External register pin	
6	vddtx	PG	TX power	
7	vsstx	PG	TX ground	

4.1.8. Video DAC interface

No.	Hex.	Dir.	Description	
1	avdd	PG	Analog power	3.3V
2	avss	PG	Analog ground	
3	cout	O	Composite video signal output	
4	rset	I	DAC scale adjustment	
5	cbu	I	Connect to power via a 0.1uF capacitor	

4.1.9. Sensor interface

No.	Hex.	Dir.	Description		
1	rgb0	I	Sensor data input bit 0.		
2	rgb1	I	Sensor data input bit 1.		
3	rgb2	I	Sensor data input bit 2.	TV decoder data input bit0	
4	rgb3	I	Sensor data input bit 3.	TV decoder data input bit1	
5	rgb4	I	Sensor data input bit 4.	TV decoder data input bit2	
6	rgb5	I	Sensor data input bit 5.	TV decoder data input bit3	
7	rgb6	I	Sensor data input bit 6.	TV decoder data input bit4	
8	rgb7	I	Sensor data input bit 7.	TV decoder data input bit5	
9	rgb8	I	Sensor data input bit 8.	TV decoder data input bit6	
10	rgb9	I	Sensor data input bit 9.	TV decoder data input bit7	
11	VD	B	Vertical synchronization signal		

No.	Hex.	Dir.	Description	
12	HD	B	Horizontal synchronization signal	
13	MCLK	B	Sensor master clock	
14	PCLK	B	Sensor pixel clock	
15	sck	O	SSISCL	
16	sd	B	SSISDA	

4.1.10. RTC

No.	Hex.	Dir.	Description	
1	xtalrtco	O	32768 crystal pad output	
2	xtalrtci	I	32768 crystal pad input	
3	xvdd	PG	RTC crystal pad power	3.3V

4.1.11. GPIO

No.	Hex.	Dir.	Description			
1	GPIO0	B	General purpose IO bit 0	Mshutter		
2	GPIO1	B	General purpose IO bit 1	Flashctr		
3	GPIO2	B	General purpose IO bit 2	Card-detect		
4	GPIO3	B	General purpose IO bit 3	RXD	Power hold	
5	GPIO4	B	General purpose IO bit 4	TXD		
6	GPIO5	B	General purpose IO bit 5	PWMDACA		
7	GPIO6	B	General purpose IO bit 6	PWMDACB		
8	GPIO7	B	General purpose IO bit 7	PWM0	LCD_SEN	
9	GPIO8	B	General purpose IO bit 8	PWM1	shutter_en	
10	GPIO9	B	General purpose IO bit 9	SD-WP detect		
11	GPIO10	B	General purpose IO bit 10	trap		
12	GPIO11	B	General purpose IO bit 11	suspend		
13	GPIO12	B	General purpose IO bit 12			
14	GPIO13	B	General purpose IO bit 13			
15	GPIO14	B	General purpose IO bit 14	ROM_A16 (O)		
16	GPIO15	B	General purpose IO bit 15	ROM_A17 (O)		
17	GPIO16	B	General purpose IO bit 16	ROM_A18 (O)		
18	GPIO17	B	General purpose IO bit 17	ROM_A19 (O)		

4.1.12. Power/Ground

No.	Hex.	Dir.	Description	
1~5	Ovdd	PG	IO PAD power	3.3V
6~10	vss	PG	IO/Core ground	
11~15	Dvdd	PG	Core power	1.8V

4.2. IO-TRAP

The IO-TRAP circuit is used to set the hardware configurations of the SPCA1528A. Parts of the MA pins are used for the IO-TRAP function. The IO-TRAP configuration is as below:

Pin Name	IO-trap	Description
MA[6],MA[0]	IOTRAP[6], IOTRAP[0]	External CPU selection. 2'bx0: Enable internal CPU. This is the normal configuration. 2'b10: Disable internal CPU, SPCA1528A is controlled by an external CPU via CPU interface. 2'b11: Disable internal CPU, SPCA1528A is controlled by an external CPU via sensor and digital TV interface.
MA[1]	IOTRAP[1]	Fast reset selection. 1'b0: Normal mode. The internal reset control circuit keeps reseting SPCA1528A core until on chip PLL reaches stable state. 1'b1: Fast reset mode. The reset control circuit resets SPCA1528A core for 32 crystal clocks. This mode is used in chip test only.
MA[5:2]	IOTRAP[5:2]	Boot mode selection. 4'bxx1x: Boot from external NOR-type ROM. 4'b1x0x: Boot from UART. 4'b010x: ISP. 4'b0000: Boot from NAND. 4'b0001: Boot from SPI.
MA[7]	IOTRAP[7]	UART selection. 0: Normal mode. The GPIO [4:3] are used as GPIOs. 1: The GPIO [4:3] are used as UART.

5. ELECTRICAL SPECIFICATION

5.1. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to VSS	V_T	-0.4 to 4.0	V
Supply Voltage relative to VSS	VDD	-0.4 to 4.0	V
Operating temperature	T_{OPT}	0 to +70	°C
Storage temperature	T_{STG}	-55 to 125	°C
HBM	V_{HBM}	> 2000	V
MM	V_{MM}	> 200	V
LatchUp	I_t	> 100	mA

5.2. DC Characteristics

DC Characteristics (T_A=25℃, VDD–VSS=3.3V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	I/O operating voltage	3.0	3.3	3.6	V
	Core operating voltage	1.62	1.8	1.98	V
I_{DD}	I_{core} (Suspend)		T.B.D		mA
I_{DD}	I_{IO} (Preview)	-	T.B.D	-	mA
	I_{core} (Preview)	-	T.B.D	-	
	I_{ddr} (Preview)		T.B.D		
I_{DD}	I_{IO} (Snap)	-	T.B.D	-	mA
	I_{core} (Snap)	-	T.B.D	-	
	I_{ddr} (Snap)		T.B.D		
I_{DD}	I_{IO} (Still Playback)	-	T.B.D	-	mA
	I_{core} (Still Playback)	-	T.B.D	-	
	I_{ddr} (Still Playback)		T.B.D		
I_{DD}	I_{IO} (Video Clip)	-	T.B.D	-	mA
	I_{core} (Video Clip)	-	T.B.D	-	
	I_{ddr} (Video Clip)		T.B.D		
I_{DD}	I_{IO} (Video Playback)	-	T.B.D	-	mA
	I_{core} (Video Playback)	-	T.B.D	-	
	I_{ddr} (Video Playback)		T.B.D		

Table 5.2.2 DC Characteristics (T_A=25℃, VDD–VSS=3.3V)

Symbol	Parameter	Min	Typ.	Max	Unit
V_{IL}	Input low voltage	-0.3	-	0.3 VDD	V
V_{IH}	Input high voltage	0.7 VDD	-	VDD+10%	V
I_{OL}	Output low current	-	4	-	mA
I_{OH}	Output high current	-	-4	-	mA
I_{OL}	Output low current	-	8	-	mA
I_{OH}	Output high current	-	-8	-	mA
I_{OL}	Output low current	-	12	-	mA
I_{OH}	Output high current	-	-12	-	mA
V_{T+}	Schmitt trigger positive-going threshold		1.5		V

Symbol	Parameter	Min	Typ.	Max	Unit
V_{T-}	Schmitt trigger negative-going threshold		1.2		V
V_{HYS}	Hysteresis voltage		0.3		V
I_{IL}	Input leakage current			1	µA

5.3. RTC Parameters

Table 5.3 RTC Current Consumption

Symbol	Parameter	Min	Typ.	Max	Unit
IRTC	Current Consumption, VRTC＝3.3V	-	2	-	µA

RTC accuracy: +/- 2.5 seconds/day

5.4. USB Interface Characteristics

5.4.1. USB DC Characteristics

Symbol	Parameter	Min	Typ.	Max.	Unit
Input Levels (full speed)					
V_{IH}	Input level high (driven)	2.0	-	-	V
V_{IHZ}	Input level high (floating)	2.7	-	3.6	V
V_{IL}	Input level low	-	-	0.8	V
V_{DI}	Differential input sensitivity	0.2	-	-	V
Input Levels (high speed)					
VHSSQ	High-speed squelch detection threshold (differential signal amplitude)	100	-	150	mV
Output Levels (full speed)					
V_{OL}	Output level low	0.0	-	0.3	V
V_{OH}	Output level high	2.8	-	3.6	V
V_{CRS}	Output signal crossover voltage	1.3	-	2.0	V
Output Levels (high speed)					
VHSOI	High-speed idle level	-10.0	-	10.0	mV
VHSOH	High-speed data signaling high	360	-	440	mV
VHSOL	High-speed data signaling low	-10.0	-	10.0	mV
VCHIRPJ	Chirp J level (differential voltage)	700	-	1100	mV
VCHIRPK	Chirp K level (differential voltage)	-900	-	-500	mV

5.4.2. USB AC Characteristics

Full Speed

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Driver Characteristics				
T_{FR}	Rise time	4	-	20	ns
T_{FF}	Fall time	4	-	20	ns
T_{RFM}	Differential Rise and Fall time matching (T_{FR}/T_{FF})	90	-	111.11	%
	Clock Timing				
T_{FDRATE}	Average bit rate		12.00		Mb/s
	Full Speed Data Timing				
T_{FDEOP}	EOP width		166.67	-	ns
Paired JK jitter	Source jitter for paired JK jitter	-	-	1.00	ns
Paired KJ jitter	Source jitter for paired KJ jitter	-	-	1.00	ns

High Speed

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Driver Characteristics				
T_{HSR}	Rise time	500	-	-	ps
T_{HSF}	Fall time	500	-	-	ps
	Clock Timing				
T_{HSDRAT}	High-speed data rate	479.760	-	480.240	b/s
T_{HSFRAM}	Microframe interval	124.9375	-	125.0625	ps

5.5. Analog Audio Interface Characteristics

(T_A =25°C, AVDD=3.3V±10%, DVDD=1.8V±10%)

Audio Analog-to-Digital Converter Electrical Characteristics:

Parameter		Condition	Min.	Typ.	Max.	Unit
Input voltage (MICINP-MICINN)		Boost gain = 20dB PGA gain = 0dB	-	-	$AV_{AVDD33AD}$/13.75	Vpp
Microphone input resistance		Boost gain = 20dB	-	10K	-	Ω
Microphone input capacitance			-	10P	-	F
Frequency response			20		19,200	Hz
Boost amplifier:	Gain Range		0	-	20	dB
	Step Size		-	20	-	dB
	Step Variation		-	2	-	dB
PGA:	Gain Range		-12	-	33	dB
	Step Size		-	1.5	-	dB
	Step Variation		-	0.15	-	dB
Signal to noise ratio (SNR)		F_{IN} = 1kHz, PGA gain = 0dB	-	85	-	dB
Total harmonic distortion + noise (THD+N)		F_{IN} = 1kHz, PGA gain = 0dB	-	-	0.01	%

Microphone Bias Electrical Characteristics:

(T_A=25°C, $AV_{AVDD33AD}$=3.3V±10%, DV_{DVDD18}=1.8V±10%, $Clock_{ADMCLK}$=12.288MHz)

Parameter	Condition	Min.	Typ.	Max.	Unit
Bias voltage		-	0.75*$AV_{AVDD33AD}$	-	V
Bias current source		-	-	3.5	mA
Output noise voltage	1kHz~20kHz	-	25	-	nV/(Hz^0.5)

5.6. Analog Video Interface Characteristics

Video DAC

Parameter	Condition	Min.	Typ.	Max.	Unit
Power supply		3.0	3.0	3.6	V
Resolution		-	9	-	bit
INL		-	±3		LSB
DNL		-	±0.5		LSB
Clock frequency		-	27	-	MHz
Output voltage	R_{set}=390ohm	1.27	1.3	1.43	V

5.7. General-Purpose ADC Characteristics

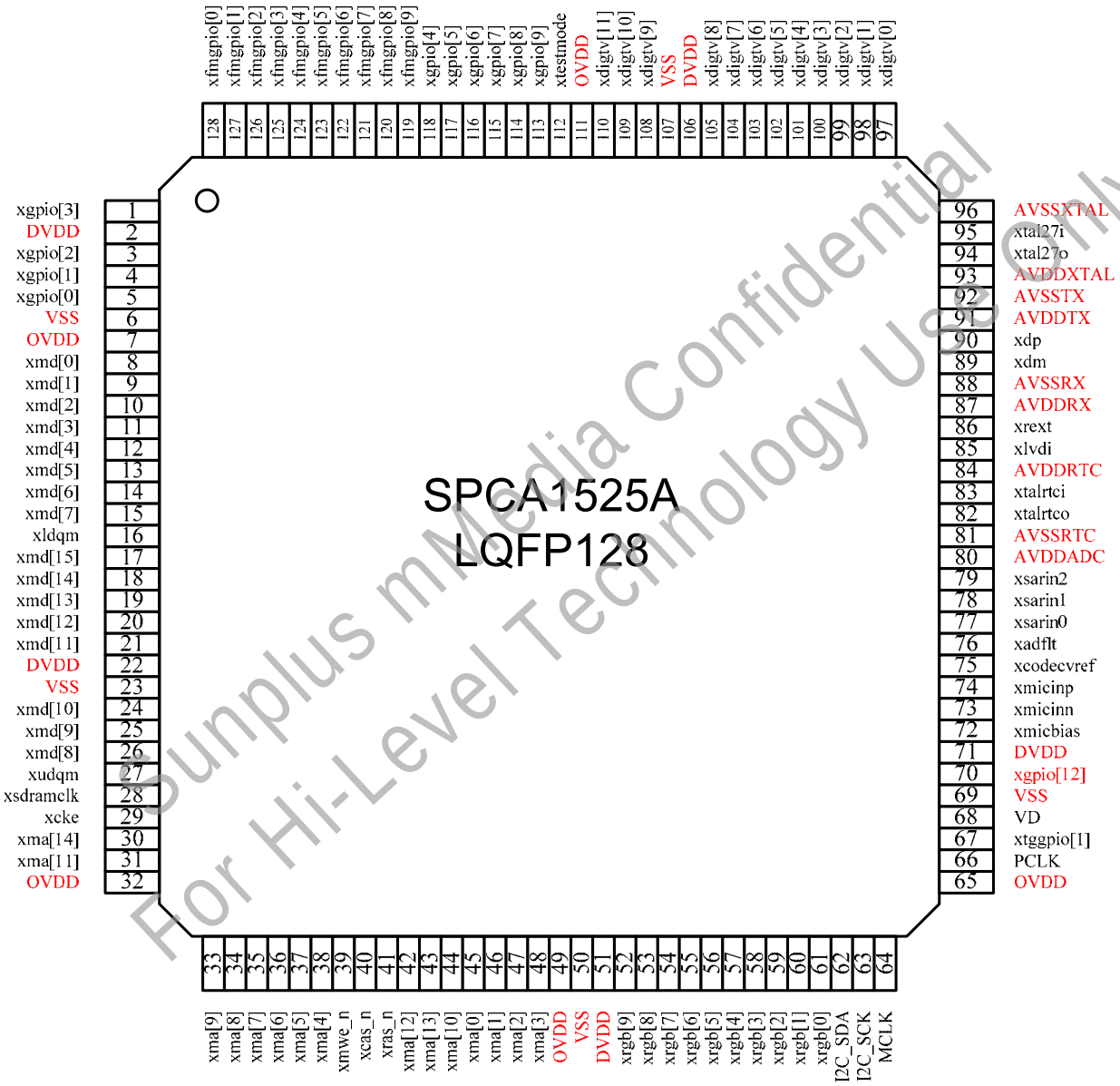
(T_A =25°C, AVDD=3.3V±10%, DVDD=1.8V±10%)

Parameter	Condition	Min.	Typ.	Max.	Unit
Input voltage range		0	-	VDDAUD	V
Input resistance	(SARIN0~SARIN2)	-	-	infinite	Ω
Resolution		-	-	10	bit
No missing codes		-	-	10	bit
Differential Nonlinearity		-	±1	±2	LSB
Integral Nonlinearity		-	±2	±4	LSB

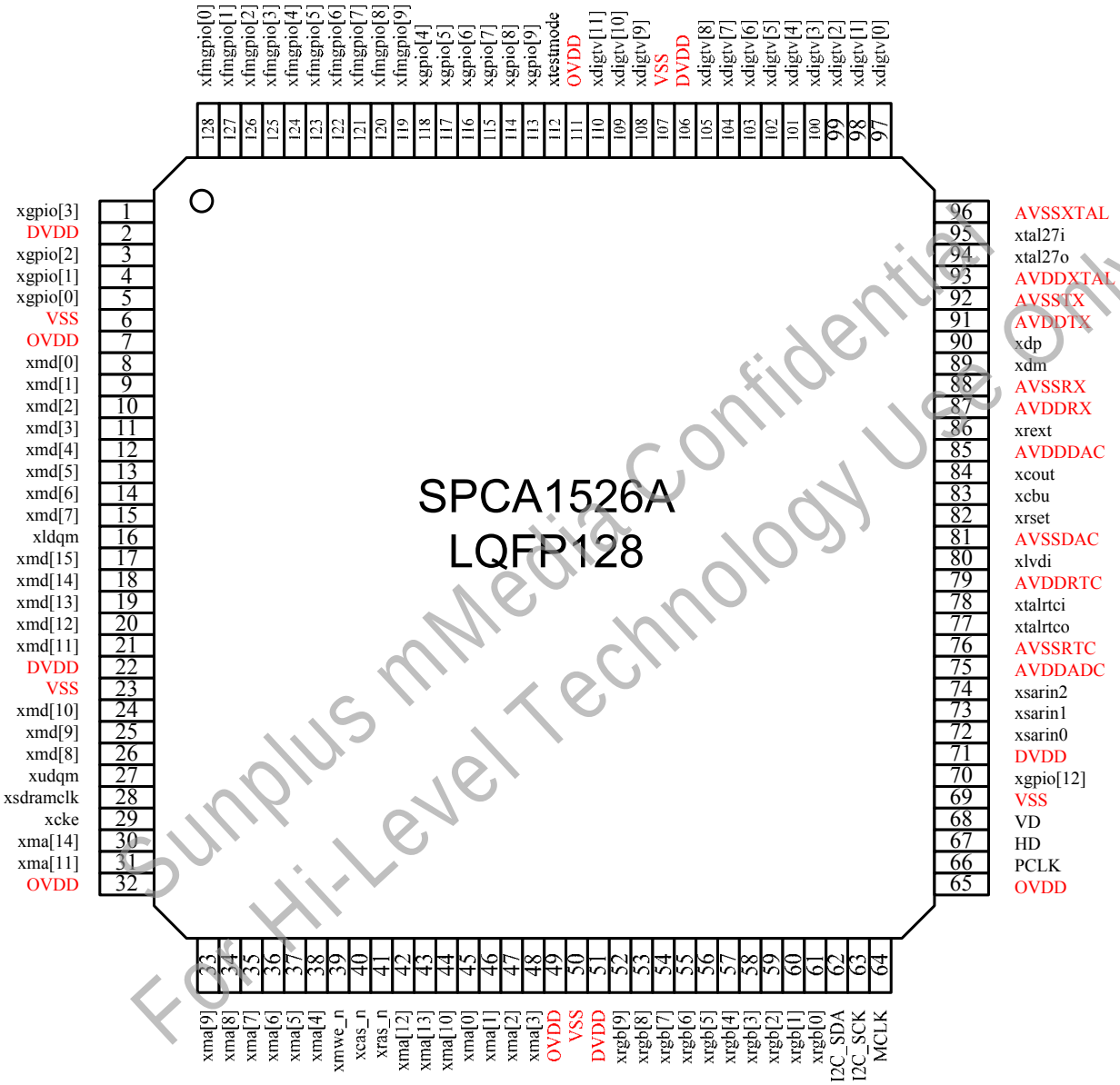
6. PACKAGE INFORMATION

6.1. Package Pin Assignment

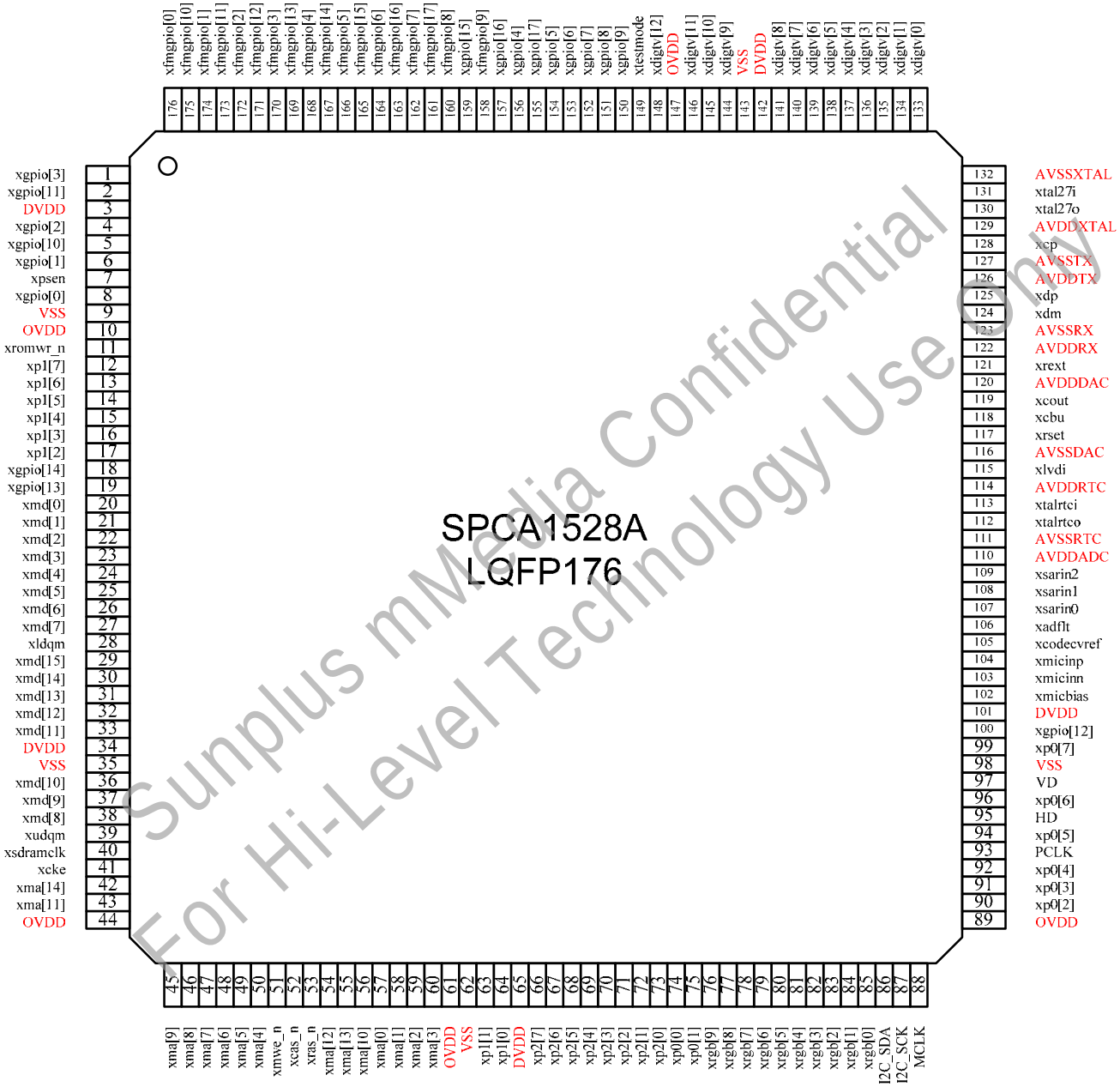
6.1.1. LQFP 128-pin Package 1 (SPCA1525A)



6.1.2. LQFP 128-pin Package 2 (SPCA1526A)



6.1.3. LQFP 176-pin Package



6.2. Pin Name

6.2.1. LQFP 128-pin Package 1 (SPCA1525A)

Pin NO.	Pin Name	Pin NO.	Pin Name	Pin NO.	Pin Name	Pin NO.	Pin Name
1	xgpio[3]	33	xma[9]	65	OVDD	97	xdigtv[0]
2	DVDD	34	xma[8]	66	PCLK	98	xdigtv[1]
3	xgpio[2]	35	xma[7]	67	xtggpio[1]	99	xdigtv[2]
4	xgpio[1]	36	xma[6]	68	VD	100	xdigtv[3]
5	xgpio[0]	37	xma[5]	69	VSS	101	xdigtv[4]
6	VSS	38	xma[4]	70	xgpio[12]	102	xdigtv[5]
7	OVDD	39	xmwe_n	71	DVDD	103	xdigtv[6]
8	xmd[0]	40	xcas_n	72	xmicbias	104	xdigtv[7]
9	xmd[1]	41	xras_n	73	xmicinn	105	xdigtv[8]
10	xmd[2]	42	xma[12]	74	xmicinp	106	DVDD
11	xmd[3]	43	xma[13]	75	xcodecvref	107	VSS
12	xmd[4]	44	xma[10]	76	xadflt	108	xdigtv[9]
13	xmd[5]	45	xma[0]	77	xsarin0	109	xdigtv[10]
14	xmd[6]	46	xma[1]	78	xsarin1	110	xdigtv[11]
15	xmd[7]	47	xma[2]	79	xsarin2	111	OVDD
16	xldqm	48	xma[3]	80	AVDDADC	112	xtestmode
17	xmd[15]	49	OVDD	81	AVSSRTC	113	xgpio[9]
18	xmd[14]	50	VSS	82	xtalrtco	114	xgpio[8]
19	xmd[13]	51	DVDD	83	xtalrtci	115	xgpio[7]
20	xmd[12]	52	xrgb[9]	84	AVDDRTC	116	xgpio[6]
21	xmd[11]	53	xrgb[8]	85	xlvdi	117	xgpio[5]
22	DVDD	54	xrgb[7]	86	xrext	118	xgpio[4]
23	VSS	55	xrgb[6]	87	AVDDRX	119	xfmgpio[9]
24	xmd[10]	56	xrgb[5]	88	AVSSRX	120	xfmgpio[8]
25	xmd[9]	57	xrgb[4]	89	xdm	121	xfmgpio[7]
26	xmd[8]	58	xrgb[3]	90	xdp	122	xfmgpio[6]
27	xudqm	59	xrgb[2]	91	AVDDTX	123	xfmgpio[5]
28	xsdramclk	60	xrgb[1]	92	AVSSTX	124	xfmgpio[4]
29	xcke	61	xrgb[0]	93	AVDDXTAL	125	xfmgpio[3]
30	xma[14]	62	I2C_SDA	94	xtal27o	126	xfmgpio[2]
31	xma[11]	63	I2C_SCK	95	xtal27i	127	xfmgpio[1]
32	OVDD	64	MCLK	96	AVSSXTAL	128	xfmgpio[0]

6.2.2. LQFP 128-pin Package 2 (SPCA1526A)

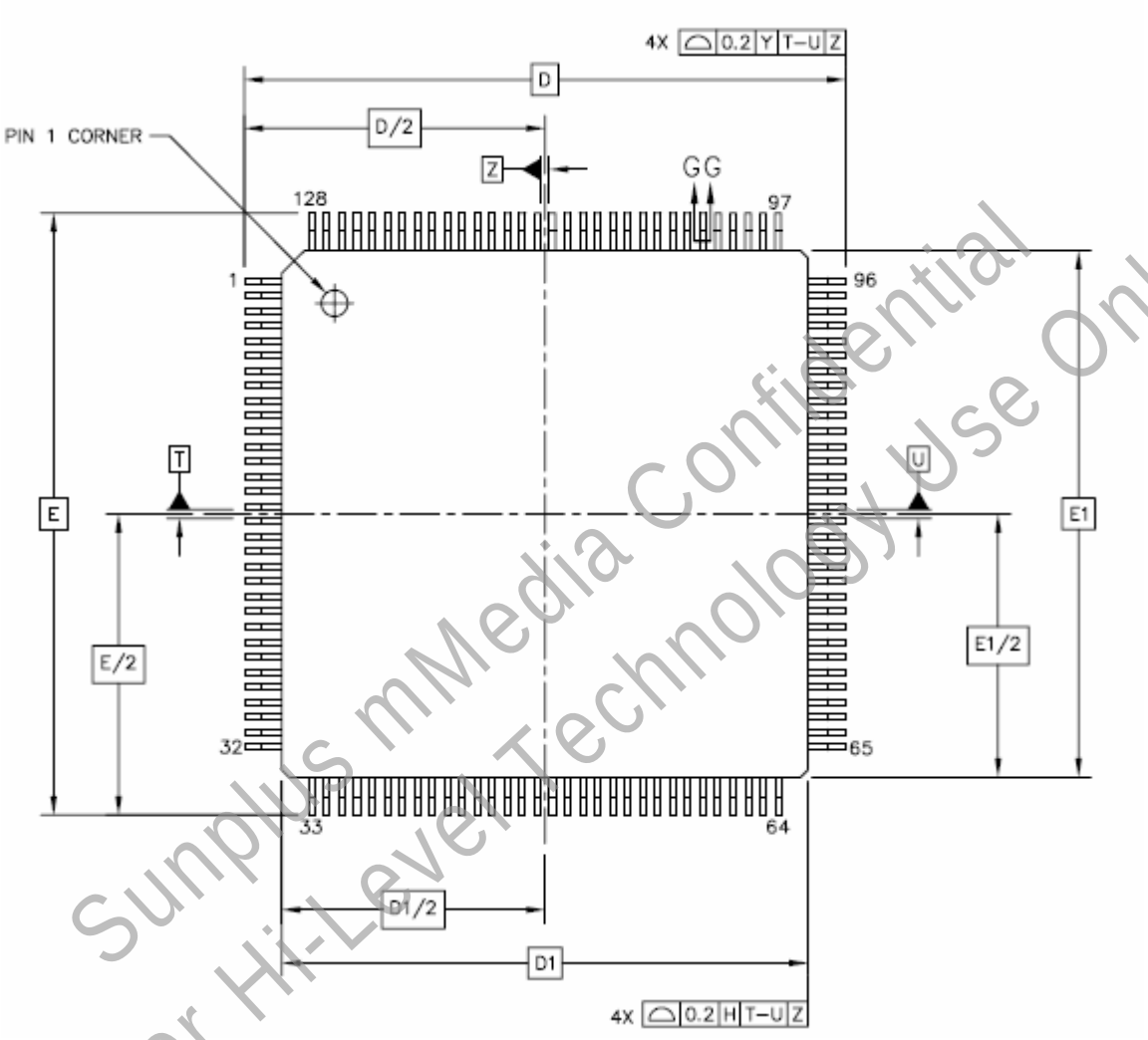
Pin NO.	Pin Name	Pin NO.	Pin Name	Pin NO.	Pin Name	Pin NO.	Pin Name
1	xgpio[3]	33	xma[9]	65	OVDD	97	xdigtv[0]
2	DVDD	34	xma[8]	66	PCLK	98	xdigtv[1]
3	xgpio[2]	35	xma[7]	67	HD	99	xdigtv[2]
4	xgpio[1]	36	xma[6]	68	VD	100	xdigtv[3]
5	xgpio[0]	37	xma[5]	69	VSS	101	xdigtv[4]
6	VSS	38	xma[4]	70	xgpio[12]	102	xdigtv[5]
7	OVDD	39	xmwe_n	71	DVDD	103	xdigtv[6]
8	xmd[0]	40	xcas_n	72	xsarin0	104	xdigtv[7]
9	xmd[1]	41	xras_n	73	xsarin1	105	xdigtv[8]
10	xmd[2]	42	xma[12]	74	xsarin2	106	DVDD
11	xmd[3]	43	xma[13]	75	AVDDADC	107	VSS
12	xmd[4]	44	xma[10]	76	AVSSRTC	108	xdigtv[9]
13	xmd[5]	45	xma[0]	77	xtalrtco	109	xdigtv[10]
14	xmd[6]	46	xma[1]	78	xtalrtci	110	xdigtv[11]
15	xmd[7]	47	xma[2]	79	AVDDRTC	111	OVDD
16	xldqm	48	xma[3]	80	xlvdi	112	xtestmode
17	xmd[15]	49	OVDD	81	AVSSDAC	113	xgpio[9]
18	xmd[14]	50	VSS	82	xrset	114	xgpio[8]
19	xmd[13]	51	DVDD	83	xcbu	115	xgpio[7]
20	xmd[12]	52	xrgb[9]	84	xcout	116	xgpio[6]
21	xmd[11]	53	xrgb[8]	85	AVDDDAC	117	xgpio[5]
22	DVDD	54	xrgb[7]	86	xrext	118	xgpio[4]
23	VSS	55	xrgb[6]	87	AVDDRX	119	xfmgpio[9]
24	xmd[10]	56	xrgb[5]	88	AVSSRX	120	xfmgpio[8]
25	xmd[9]	57	xrgb[4]	89	xdm	121	xfmgpio[7]
26	xmd[8]	58	xrgb[3]	90	xdp	122	xfmgpio[6]
27	xudqm	59	xrgb[2]	91	AVDDTX	123	xfmgpio[5]
28	xsdramclk	60	xrgb[1]	92	AVSSTX	124	xfmgpio[4]
29	xcke	61	xrgb[0]	93	AVDDXTAL	125	xfmgpio[3]
30	xma[14]	62	I2C_SDA	94	xtal27o	126	xfmgpio[2]
31	xma[11]	63	I2C_SCK	95	xtal27i	127	xfmgpio[1]
32	OVDD	64	MCLK	96	AVSSXTAL	128	xfmgpio[0]

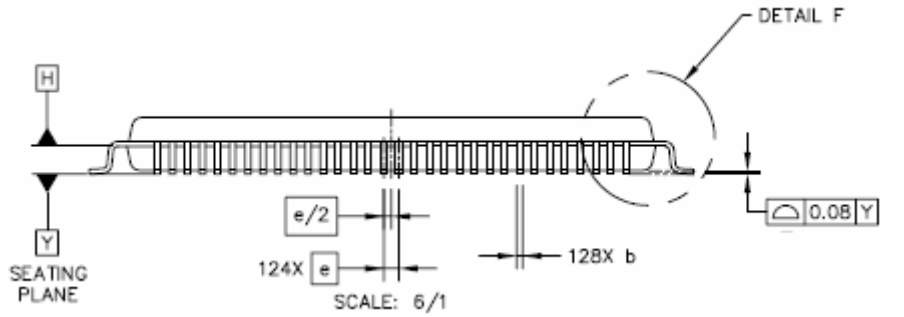
6.2.3. LQFP 176-pin Package

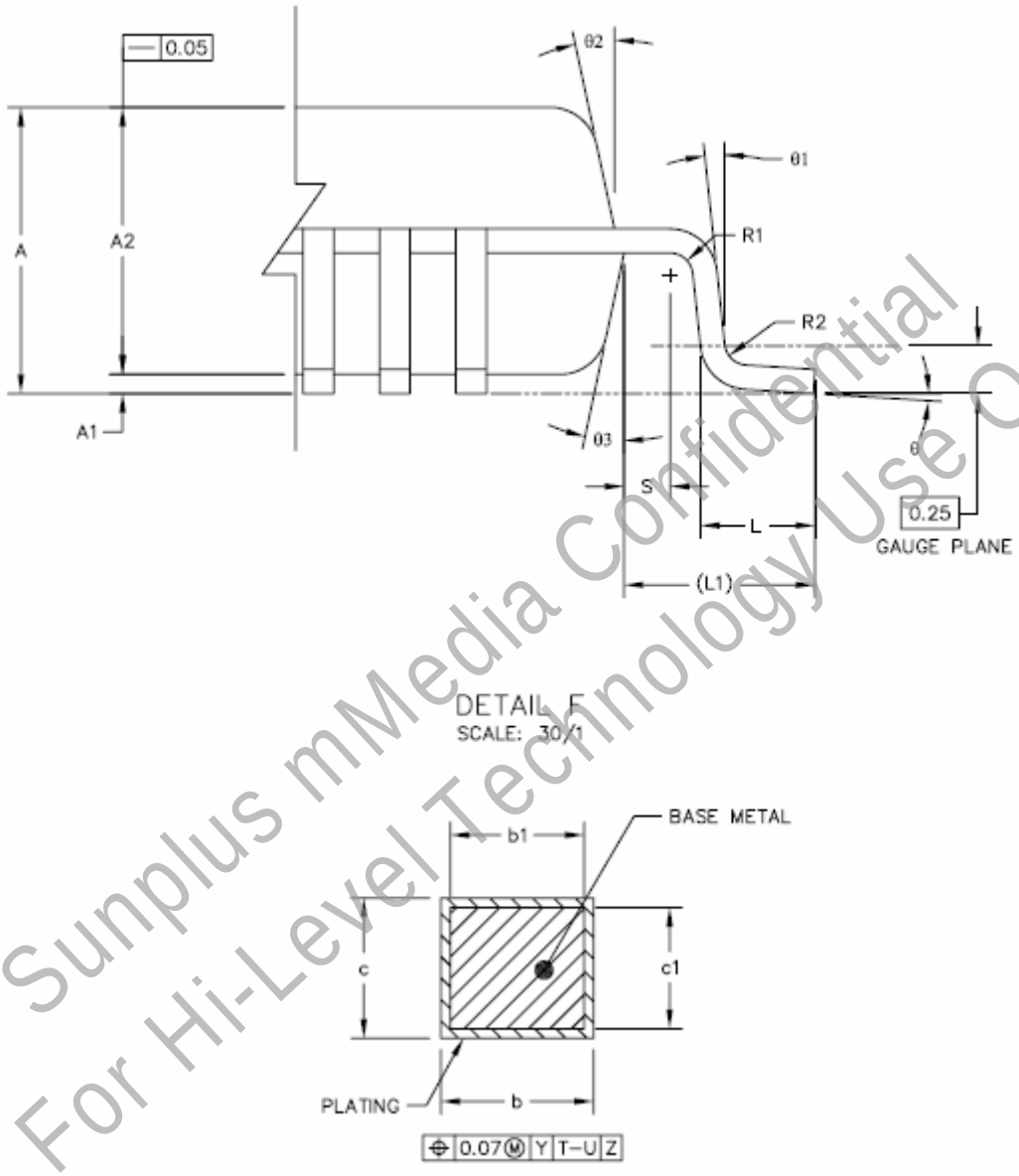
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	xgpio[3]	45	xma[9]	89	OVDD	133	xdigtv[0]
2	xgpio[11]	46	xma[8]	90	xp0[2]	134	xdigtv[1]
3	DVDD	47	xma[7]	91	xp0[3]	135	xdigtv[2]
4	xgpio[2]	48	xma[6]	92	xp0[4]	136	xdigtv[3]
5	xgpio[10]	49	xma[5]	93	PCLK	137	xdigtv[4]
6	xgpio[1]	50	xma[4]	94	xp0[5]	138	xdigtv[5]
7	xpsen	51	xmwe_n	95	HD	139	xdigtv[6]
8	xgpio[0]	52	xcas_n	96	xp0[6]	140	xdigtv[7]
9	VSS	53	xras_n	97	VD	141	xdigtv[8]
10	OVDD	54	xma[12]	98	VSS	142	DVDD
11	xromwr_n	55	xma[13]	99	xp0[7]	143	VSS
12	xp1[7]	56	xma[10]	100	xgpio[12]	144	xdigtv[9]
13	xp1[6]	57	xma[0]	101	DVDD	145	xdigtv[10]
14	xp1[5]	58	xma[1]	102	xmicbias	146	xdigtv[11]
15	xp1[4]	59	xma[2]	103	xmicinn	147	OVDD
16	xp1[3]	60	xma[3]	104	xmicinp	148	xdigtv[12]
17	xp1[2]	61	OVDD	105	xcodecvref	149	xtestmode
18	xgpio[14]	62	VSS	106	xadflt	150	xgpio[9]
19	xgpio[13]	63	xp1[1]	107	xsarin0	151	xgpio[8]
20	xmd[0]	64	xp1[0]	108	xsarin1	152	xgpio[7]
21	xmd[1]	65	DVDD	109	xsarin2	153	xgpio[6]
22	xmd[2]	66	xp2[7]	110	AVDDADC	154	xgpio[5]
23	xmd[3]	67	xp2[6]	111	AVSSRTC	155	xgpio[17]
24	xmd[4]	68	xp2[5]	112	xtalrtco	156	xgpio[4]
25	xmd[5]	69	xp2[4]	113	xtalrtci	157	xgpio[16]
26	xmd[6]	70	xp2[3]	114	AVDDRTC	158	xfmgpio[9]
27	xmd[7]	71	xp2[2]	115	xlvdi	159	xgpio[15]
28	xldqm	72	xp2[1]	116	AVSSDAC	160	xfmgpio[8]
29	xmd[15]	73	xp2[0]	117	xrset	161	xfmgpio[17]
30	xmd[14]	74	xp0[0]	118	xcbu	162	xfmgpio[7]
31	xmd[13]	75	xp0[1]	119	xcout	163	xfmgpio[16]
32	xmd[12]	76	xrgb[9]	120	AVDDDAC	164	xfmgpio[6]
33	xmd[11]	77	xrgb[8]	121	xrext	165	xfmgpio[15]
34	DVDD	78	xrgb[7]	122	AVDDRX	166	xfmgpio[5]
35	VSS	79	xrgb[6]	123	AVSSRX	167	xfmgpio[14]
36	xmd[10]	80	xrgb[5]	124	xdm	168	xfmgpio[4]
37	xmd[9]	81	xrgb[4]	125	xdp	169	xfmgpio[13]
38	xmd[8]	82	xrgb[3]	126	AVDDTX	170	xfmgpio[3]
39	xudqm	83	xrgb[2]	127	AVSSTX	171	xfmgpio[12]
40	xsdramclk	84	xrgb[1]	128	xcp	172	xfmgpio[2]
41	xcke	85	xrgb[0]	129	AVDDXTAL	173	xfmgpio[11]
42	xma[14]	86	I2C_SDA	130	xtal27o	174	xfmgpio[1]
43	xma[11]	87	I2C_SCK	131	xtal27i	175	xfmgpio[10]
44	OVDD	88	MCLK	132	AVSSXTAL	176	xfmgpio[0]

6.3. Package Size

6.3.1. LQFP128

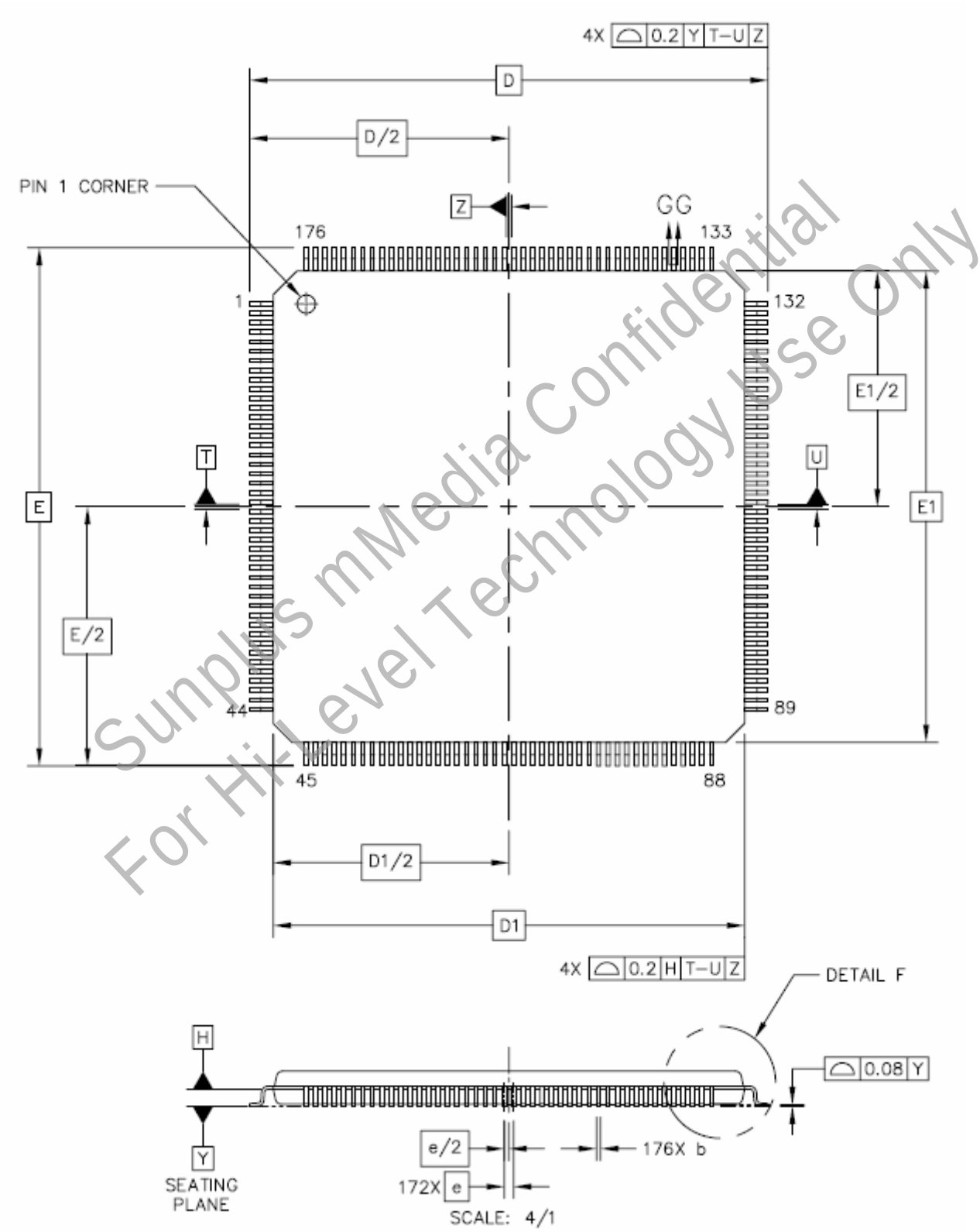


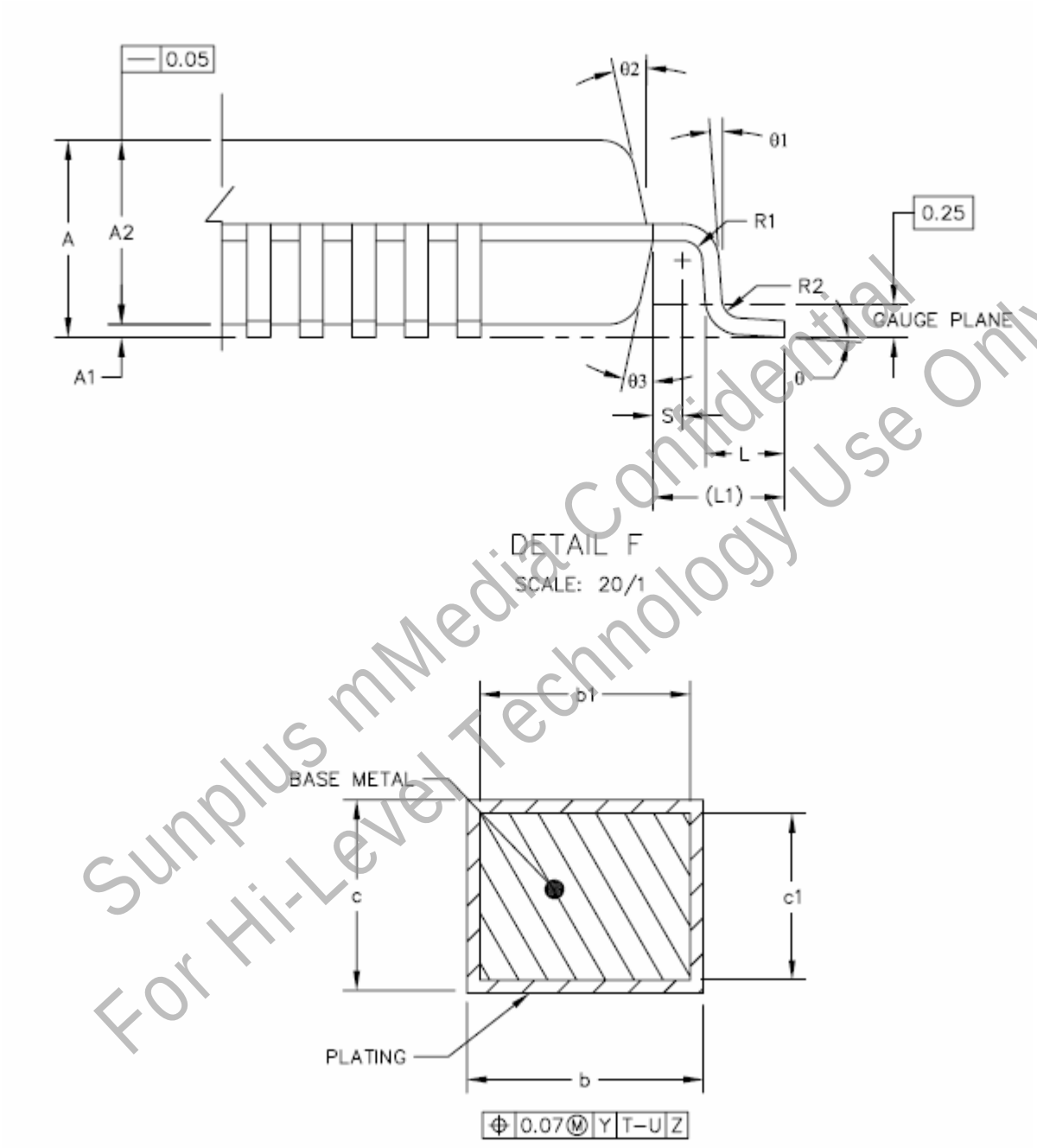




DIM	MIN	NOM	MAX
A	----		1.6
A1	0.05		0.15
A2	1.35	1.4	1.45
b	0.13	0.18	0.23
b1	0.13	0.16	0.19
c	0.09		0.2
c1	0.09		0.16
D		16 BSC	
D1		14 BSC	
e		0.4 BSC	
E		16 BSC	
E1		14 BSC	
L	0.45	0.6	0.75
L1		1 REF	
R1	0.08		---
R2	0.08		0.2
S	0.2		---
θ	0°	3.5°	7°
θ1	0°		---
θ2	11°	12°	13°
θ3	11°	12°	13°

6.3.2. LQFP176





DIM	MIN	NOM	MAX
A	----		1.6
A1	0.05		0.15
A2	1.35	1.4	1.45
b	0.13	0.18	0.23
b1	0.13	0.16	0.19
c	0.09		0.2
c1	0.09		0.16
D		22 BSC	
D1		20 BSC	
e		0.4 BSC	
E		22 BSC	
E1		20 BSC	
L	0.45	0.6	0.75
L1		1 REF	
R1	0.08		---
R2	0.08		0.2
S	0.2		---
θ	0°	3.5°	7°
θ1	0°		---
θ2	11°	12°	13°
θ3	11°	12°	13°

6.4. Ordering Information

Product Number	Package Type	Memo
SPCA1528A_HL141	LQFP176 Pin, Green Package	
SPCA1525A_HL091	LQFP128 Pin, Green Package	With Audio
SPCA1526A_HL091	LQFP128 Pin, Green Package	With TV-Out

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

6.5. Storage Condition and Period for Package

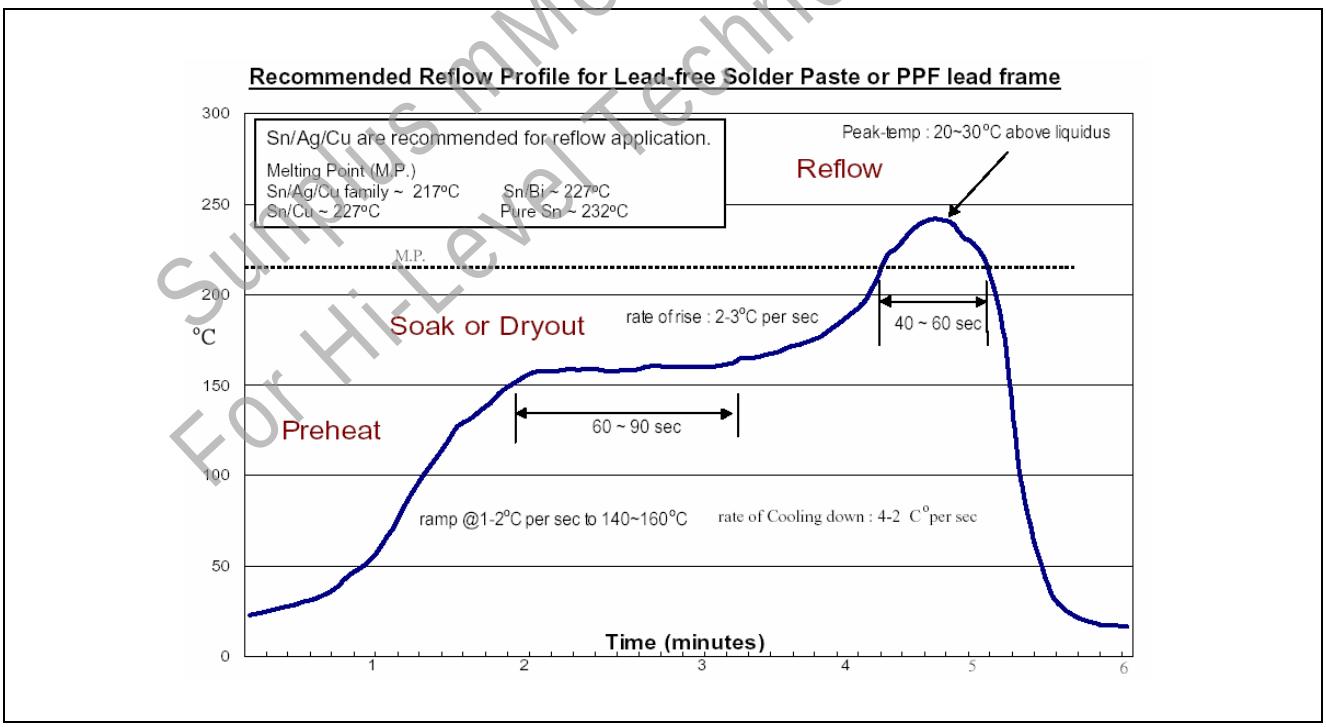
For Green Packages:

Package	Moisture sensitivity level	Max. Reflow temperature	Floor life storage condition	Dry pack
LQFP	LEVEL 3	255 +5/-0℃	168Hrs @ ≦30℃/ 60% R.H.	Yes

Note1: Please refer to IPC/JEDEC standard J-STD-020A and EIA JEDEC stand JESD22-A112, or the "CAUTION Note" on dry pack bag.

6.6. Recommended SMT Temperature Profile

This "Recommended" temperature profile is a rough guideline for SMT processing reference. Most of SUNPLUS MMEDIA leadframe-based products choose Matte Tin and Sn/Bi for plating recipe. For PPF(Pre-Plated Frame) products with 63/37 solder paste, we recommend 240℃~245℃ for peak temperature.



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8. REVISION HISTORY

Date	Revision #	Description	Page
2007.12.13	0.1	Original	26
2008.06.16	0.2	Modify SPCA1525A pin list on page 18, 21 (1) Remove pin ”xcp” (original NO. 92) (2) Add pin “xgpio[12]” (revised NO. 70) (2) Original pin sequence 70~91 is revised to sequence 71~92.	18,21
2008.07.10	0.3	(1) Add ordering information (2) Add package size	30 24~29