DATA SHEET

SUNPLUS

SPCA536A

Advanced Imaging Controller

MAR. 23, 2004

Version 1.0

Table of Contents

PAGE

ADVANCED IMAGING CONTROLLER

1.GENERAL DESCRIPTION

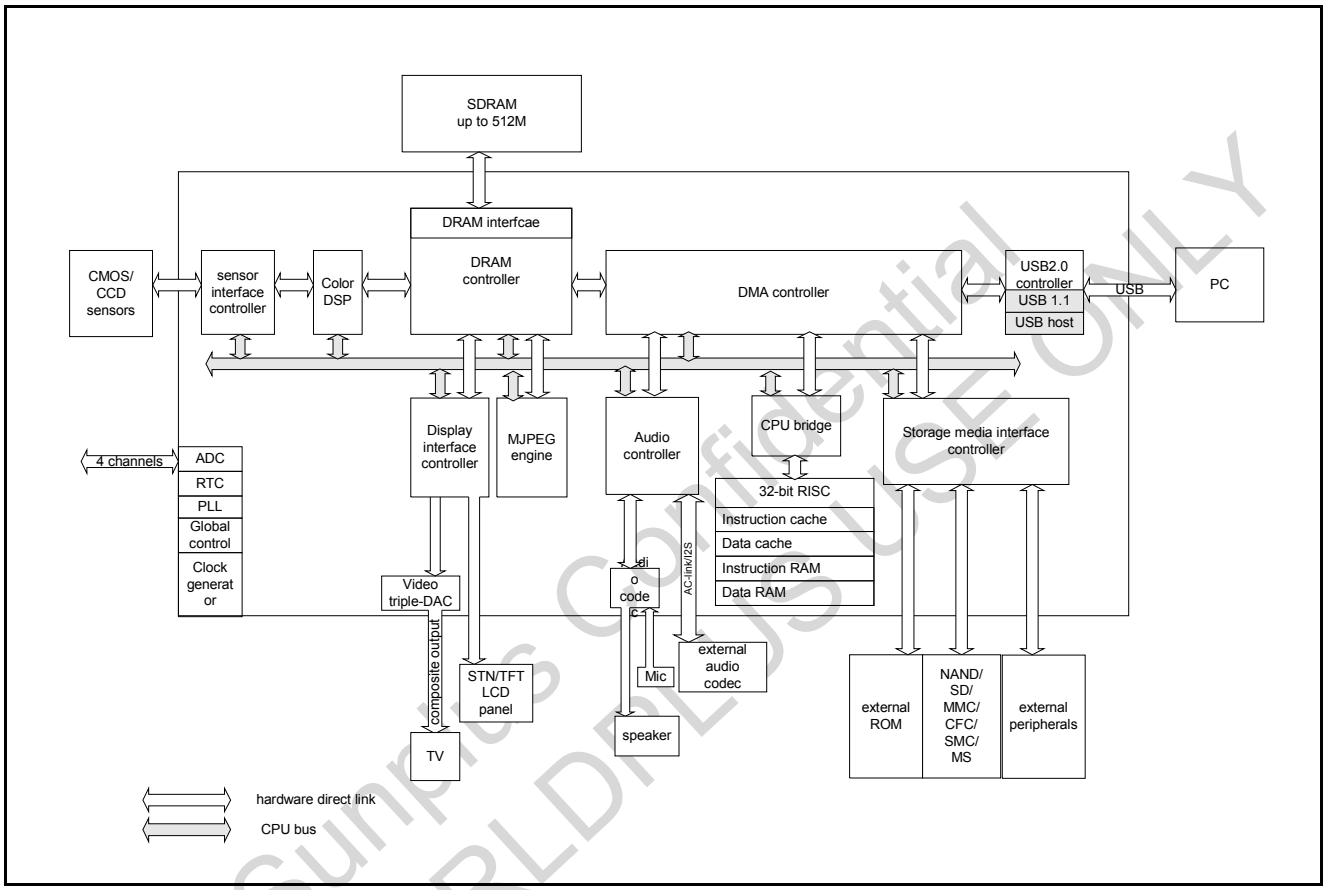
SPCA536A is designed for the advanced imaging applications, including multi-mega pixel digital still cameras and digital video recorders. It integrates a rich set of components required by complex imaging products. Its peripheral interfaces are so flexibly designed that it is easy to implement many different applications. This chip can support both CCD and CMOS image sensors up to 16M pixels. SPCA536A has built in USB2.0 high-speed device controller and USB2.0 full-speed embedded host controller. The embedded high quality color processing engine, powerful 32-bit RISC CPU and real time MPEG codec engines make SPCA536A an ideal solution to implement a high-end digital still camera.

2.FEATURES

- Support image sensors up to 16M-pixel resolution.
- Support dual-sensor application.
- Interface to CCD sensors from Sony, Sharp and Matsushita.
- Support mega-pixel CMOS sensors from Omnivision, IC Media-Micron, ST Microelectronic and many other major vendors in US, Japan, Korea and Taiwan.
- Built-in Timing generator for progressive, 2-field, 3-field and 4-field CCD sensors.
- Support both master mode and slave mode CMOS sensors.
- Accurate flash light control.
- Excellent color processing engine
  - AE window statistics
  - AWB window statistics
  - 2-D edge enhancement
  - Luminance histogram
  - Hue/Saturation adjustment
  - Brightness/Contrast adjustment
  - Programmable edge enhancement
  - Bad pixel concealment can be done by Hard-wired engine or by the user-defined firmware.
  - Fully programmable Gamma table
  - Lens shade compensation
- Support 16M, 64M, 128M, 256M, and 512M SDRAM.
- Extended interface to communicate with external devices, such as an Ethernet controller.
- Support SMC, MMC, SD, xD, Memory stick (Pro) and CF flash memory cards.
- EJTAG debugging interface with complete debugging tools.
- Two RS-232 ports.
- Hard-wired JPEG/MPEG engine to speedup the image compression. Support JPEG, Motion JPEG, MPEG-1 and MPEG-4. QVGA resolution (320x240) real time (30 fps) codec.
- Up to 4X digital zoom.
- Built-in 32-bit RISC with 14K-byte cache.
- Shadow memory architecture to enhance the system performance.
- 4M bytes programming space.
- On chip 16K-byte boot ROM.
- Programmable CPU operating frequency from 375kHz to 96MHz.
- USB2.0 full-speed and high speed.
- Build-in USB full speed transceiver.
- Build-in USB host controller.
- USB MSDC compatible.
- Graphic-based OSD.
- Built-in TV encoder with triple DACs, supporting both NTSC/PAL composite video and analog RGB output.
- Digital TV output interface, conform to CCIR601 (8-bit/16-bit data bus) and CCIR656 standard.
- Digital TV input interface covers CCIR601 (8-bit data bus) and CCIR656.
- Digital TFT LCD output interface, Unipac, Epson, Casio
- Digital STN LCD panel interface for GiantPlus panels.
- Interface to micro display devices.
- Built-in 8-bit audio ADC.
- PWM audio output.
- Built-in 4-channel 8-bit ADC
- Built-in RTC
- AC97 interface to external audio codec.
- I2S interface to external DAC.
- In-system-programming for firmware update.
- 1.8V/3.3V dual power supply.
- Package TFBGA288 16x16 mm or 12x12 mm

3.ARCHITECTURE BLOCK DIAGRAM

The heart of SPCA536A is a powerful 32-bit RISC CPU and a rich set of hardware engines. All the engines can work simultaneously to achieve the highest performance. The interfaces to external components are flexible enough, allowing SPCA536A to work with a variety of sensors, LCD panels and storage media.



Sensor interface controller The sensor interface controller generates the timing required by the CMOS sensors or CCD sensors. SPCA536A supports dual sensor inputs. It also embeds a serial interface to control the CMOS sensors or the CDS/AGC chips.

PLL SPCA536's requires only an external crystal. All the required clocks are generated by the on-chip PLL. If the application supports composite TV output, the frequency of the crystal must be 27MHz. Otherwise, 6MHz, 12MHz, 24MHz, 48MHz are all applicable. SPCA536A uses IO-trap for crystal frequency selection.

Global control and clock generator These module controls the reset sequence, suspend/resume and clock frequency adjustments. It also performs power management by turning off the unused clock.

CPU The 32-bit RISC CPU coordinates the camera operation. The CPU can be disabled and release the control to an external CPU. The CPU handles audio compression and decompression. It can also perform image post-processing. The CPU integrates 2K-byte instruction cache, 2K-byte data cache, 2K-byte instruction RAM and 8K-byte data RAM. The instruction RAM allows the CPU to execute the firmware with the cache-access speed without slowing down by the cache-miss. The data RAM allows the CPU to access data without cache-miss, too. The SPCA536A's DMA controller can swap data between external SDRAM and the data RAM at the extremely high speed. SPCA536A can process the image either by a build-in ColorDSP, by the RISC CPU or combination of both.

Color DSP Image processing engine of the SPCA536.

DRAM controller The DRAM controller provides access path to the SDRAM for the other internal modules of the SPCA536. SPCA536A supports SDRAM. The DRAM controller also integrates acceleration engines for a variety of graphic function, such as image scaling, rotation, mirror, BitBlit,…etc. Depending on

the application requirement, the operating frequency of the DRAM interface can programmed to be 48MHz, 72MHz or 96 MHz.

TV/LCD interface controller This module has integrated a variety of digital interfaces, which includes TFT LCD interface, STN LCD interface, micro display interface, and the digital TV outputs. It also integrates a TV encoder, supporting both NTSC and PAL outputs. Also, a triple-DAC is integrated, allowing SPCA536A to interface with analog RGB TFT panels. The graphic-based OSD function is also integrated in this module. SPCA536A has a dedicated scaling engine in the display interface, which adjusts the image resolution to fit a variety of display resolution.

MJPEG engine This is a MPEG and JPEG combo codec. It supports JPEG, Motion JPEG, MPEG1 and MPEG4 still image/video compression and decompression. The MJPEG engine is a high-performance codec capable of compressing (decompressing) 320x240 resolution video at 30 fps. The bit-rate can be controlled by the hardware automatically or programmed by the RISC dynamically.

DMA controller The DMA controller allows high-speed data transfer between SPCA536A's internal modules. SPCA536A has three DMA channels. One channel is dedicated to transfer data within SDRAM. The other channel is dedicated to data transfer between the SDRAM and the storage media. The last channel is a general-purpose channel, which allows data transfer between the SDRAM, USB FIFO, the storage media, the CPU data RAM, and the audio buffer.

Storage media controller The storage controller is a high-efficiency bridge between different storage media and the internal modules. Both DMA data transfer and PIO data transfer are supported. SPCA536A supports all major storage media, including memory stick Pro. The storage media interface also serves as an interface to communicate with off-chip peripherals, such as Ethernet controller and wireless LAN controller.

Audio control It embeds a hardwired IMA-ADPCM codec engine. The audio controller also integrates an internal ADC and a PWM circuitry for audio recording and playback respectively. SPCA536A can also interface to an external audio codec to handle stereo audio. It supports AC-97 codecs and external I2S DAC.

USB2.0 controller The USB controller supports USB2.0 full-speed and high-speed device functions. It also includes a USB2.0 full-speed embedded host function. The on-chip USB2.0 full speed transceiver saves the application from extra cost of external transceiver. In the USB2.0 configuration, SPCA536A supports the standard UTMI bus to interface with an external transceiver. The USB controller supports all types of pipes defined in the USB specification (isochronous, bulk, control and interrupt pipes).

RTC The RTC module enables the SPCA536A to maintain the calendar function with the minimum power consumption.

ADC The on chip 4-channel ADC can be used as audio input source, user interface control, battery power detection, ……etc. The sampling frequency is programmable.

3.1. The CCD Sensors Supported

CCD	Vendors and Part Numbers		
Resolutions	Sony	Sharp	Panasonic
1.3 M	ICX202AQ, ICX205AK ICX442AQ, ICX232BQ	LZ23J3V, RJ23J3A, RJ24J3A	
2.1 M	ICX224AQ, ICX284AQ ICX434,	LZ21N3V, RJ23N3AB, RJ24N3AA	MN39470, MN39472
3.0 M	ICX262AQ, ICX432DQ (3f)	RJ21P3A, RJ23P3AA (3f)	MN39592, MN39480 (3f)
4.0 M	ICX406AQF,	RJ21R3A, RJ23R3AA	MN39482 (3f)
5.0 M	ICX452 (3f)	RJ21S3AA	MN39593 (3f), MN39594, NM39620 (3f)
6.0 M			MN39595 (3f)

3.2. The Display Panels Supported

Vendors	Size	Part Number	Interface
AU Optronics	1.5-inch	A015AN02, A015AN02-1, A015AN04 V1, A015BL01, A015BL02	Digital
	1.8-inch	A018AN01, A018AN02, A018AN03 V1	Digital
	2.0-inch	A020BL01	Digital
Topploy	1.5-inch	TC015TREA1, TC015TREB1	Digital
	1.8-inch	TP018A	Digital
Sharp	1.5-inch	SL015A8GS01	Digital
	3.5-inch	LQ035Q7DB02	Digital
	3.8-inch	LM038QC1T10	Digital
CASIO	1.4-inch	COM14T1163	Digital
	1.5-inch	COM15T1815, COM15T1181	Digital
	1.6-inch	COM16T1151	Digital
	1.8-inch	COM18T1160, COM18T1195	Digital
Samsung	1.6-inch	LTS160Q1-SF1	Digital
Giantplus (STN)	1.4-inch	GPG24163IS3	Digital
	0.9-inch	GPG16121IS1	Digital
Sony	1.5-inch	ACX306BKU, ACX313EKM, ACX318EKM, ACX321AKM	Digital
Kopin	180K	CyberDisplay 180K	Analog
DisplayTech	QVGA	QDM-0076-MV5	Digital
MED		ME3203	Digital

4.SIGNAL DESCRIPTIONS

The SPCA535A is shipped in TFBGA288 package. TFBGA288 package supports the full functions. The following table is a summary of the chip features.

Features	TFBGA 288 (P1)
CCD sensor	Up to 16M pixels
CMOS sensor	Up to 4M pixels
Digital TV input (CCIR656/CCIR601-8bit)	√
Digital Zoom	Up to 4x
Analog TV (NTSC/PAL)	√
Digital Video Output	CCIR656/601 at 8/16-bit
LCD output (GiantPlus/AUO)	√
LCD output (EPSON/CASIO)	√
LCD output (Analog RGB for LTPS)	√
Graphic-based OSD Function	√
Dedicated GPIO	11 pins
Multi-function GPIO	Up to 140 pins
RTC	√
Embedded RISC Controller	√
EJTAG probe debug interface	√
Program Space	Up to 4M
Access to external memory	√
Maximum SDRAM Support	512M-bit
AC-97/MP3 Digital Audio Interface	√
Build in ADC	8-bit, 4 channels
Embedded USB 1.1 Transceiver	√
USB 2.0 UTMI interface	√
USB 1.1 (host) support	√
ISP Function	√
UART	2x
Flash Light Control	√
Storage Media (NAND Flash, SMC, MMC, SD, CFA, MS, xD)	√

4.1. Pin List

The following table summarizes all the functional pins of SPCA536A. Many of them are multi-function pins and most of the pins can be used as GPIO when its corresponding function is not used.

Pin No.	Pin Name	Dir.	Description	Memo
SDRAM Interface (41 Pins)				
SPCA536A supports both SDRAM. Depending on the size and type of the SDRAM, some DRAM interface pins can be used as GPIO's. Note that the IO power (OVDD1 and OVDD2) are 3.3V for SDRAM.				
1	md0	B	SDRAM data bus, bit 0.	
2	md1	B	SDRAM data bus, bit 1.	
3	md2	B	SDRAM data bus, bit 2.	
4	md3	B	SDRAM data bus, bit 3.	
5	md4	B	SDRAM data bus, bit 4.	
6	md5	B	SDRAM data bus, bit 5.	
7	md6	B	SDRAM data bus, bit 6.	
8	md7	B	SDRAM data bus, bit 7.	
9	Md8	B	SDRAM data bus, bit 8.	
10	Md9	B	SDRAM data bus, bit 9.	
11	Md10	B	SDRAM data bus, bit 10.	
12	md11	B	SDRAM data bus, bit 11.	
13	md12	B	SDRAM data bus, bit 12.	
14	md13	B	SDRAM data bus, bit 13.	
15	Md14	B	SDRAM data bus, bit 14.	
16	Md15	B	SDRAM data bus, bit 15.	
17	Sdclk	O	SDRAM clock	
18	Rasnn	O	SDRAM raw address strobe signal	
19	Casnn	O	SDRAM column address strobe signal	
20	Cke	O	SDRAM clock enable signal	
21	mwenn	O	SDRAM write enable signal	
22	Ldqm	O	SDRAM data mask signal, low byte	
23	Udqm	O	SDRAM data mask signal, high byte	
24	ma0	B	SDRAM address bus, bit 0. The DRAM address bus is also used for IO-trap. During IO-trap stage, the "ma" bus is an input bus. After the IO-trap stage, the bus is an output bus.	
25	ma1	B	SDRAM address bus, bit 1.	
26	ma2	B	SDRAM address bus, bit 2.	
27	ma3	B	SDRAM address bus, bit 3.	
28	ma4	B	SDRAM address bus, bit 4.	
29	ma5	B	SDRAM address bus, bit 5.	
30	ma6	B	SDRAM address bus, bit 6.	
31	ma7	B	SDRAM address bus, bit 7.	
32	ma8	B	SDRAM address bus, bit 8.	
33	ma9	B	SDRAM address bus, bit 9.	
34	ma10	B	SDRAM address bus, bit 10.	
35	ma11	B	SDRAM address bus, bit 11.	
			16M x1 / 16M x2 / 64M/128M / 256M/512M / GPIO	

Pin No.	Pin Name	Dir.	Description					Memo
36	ma12	B	Dramgpio0	LDQM1	BA0	A12	Dramgpio0	
37	ma13	B	Dramgpio1	UDQM1	BA1	BA0	Dramgpio1	
38	ma14	B	Dramgpio2	Dramgpio2	Dramgpio2	BA1	Dramgpio2	
39	sdclknn	O	Reserved 1			Dramgpio3 (default)		
40	ldqs	B	Reserved 2			Dramgpio4 (default)		
41	udqs	B	Reserved 3			Dramgpio5 (default)		
Sensor Interface Controller (44 Pins)								
			CCD interface	*CMOS interface*	*Digital TV input*	*Tggpio*		
1	Sg1a	B	Sg1a			TGgpio14		
2	Sg1b	B	Sg1b			TGgpio15		
3	Sg3a	B	Sg3a			TGgpio16		
4	Sg3b	B	Sg3b			TGgpio17		
5	Sg5a	B	Sg5a			TGgpio18		
6	Sg5b	B	Sg5b			TGgpio19		
7	Sg7a	B	Sg7a			TGgpio20		
8	Sg7b	B	Sg7b			TGgpio21		
9	V10	B	V10			TGgpio22		
10	V9	B	V9			TGgpio23		
11	V8	B	V8			TGgpio24		
12	V7	B	V7			TGgpio25		
13	V6	B	V6			TGgpio26		
14	V5	B	V5			TGgpio27		
15	V4	B	V4			TGgpio28		
16	V3	B	V3			TGgpio29		
17	V2	B	V2	Exthd (B)	Exthd (I)	TGgpio30		
18	V1	B	V1	Extvd (B)	Extvd (I)	TGgpio31		
19	fh1	B	fh1			TGgpio32		
20	fh2	B	fh2			TGgpio33		
21	fr	B	fr			TGgpio34		
22	sub	B	sub	sub	Extdvalid (I)	TGgpio35		
23	mshutter	B	mshutter	mshutter	Extfield (I)	TGgpio36		
			3-wire bus	***Synchronus bus***				
24	sen	B	sen			TGgpio37		
25	Sck	B	Clock	SSISCL		TGgpio38		
26	sda	B	data	SSISDA		TGgpio39		
27	vsubctrl	B	vsubctrl			TGgpio40		
28	adclp	B	adclp	2XCK		TGgpio41		
29	obclp	B	obclp			TGgpio42		
30	adck	B	adck	adck		TGgpio43		
31	pblk	B	pblk			TGgpio44		
32	fs	B	fs			TGgpio45		
33	fcds	B	fcds			TGgpio46		
34	Flightctr	B	Flash strobe			TGgpio47		
35	rgb0	I	Sensor data0		vertical valid			

Pin No.	Pin Name	Dir.	Description					Memo
36	rgb1	I	Sensor data1		horizontal valid			
37	rgb2	I	Sensor data2		Data0			
38	rgb3	I	Sensor data3		Data1			
39	rgb4	I	Sensor data4		Data2			
40	rgb5	I	Sensor data5		Data3			
41	rgb6	I	Sensor data6		Data4			
42	rgb7	I	Sensor data7		Data5			
43	rgb8	I	Sensor data8		Data6			
44	rgb9	I	Sensor data9		Data7			
			Single sensor	Dual sensor				
45	Tggpio0	B	Tggpio0	S2_exthd				
46	Tggpio1	B	Tggpio1	S2_extvd				
47	Tggpio2	B	Tggpio2	S2_adck				
48	Tggpio3	B	Tggpio3	S2_sen				
49	Tggpio4	B	Tggpio4	S2_sck				
50	Tggpio5	B	Tggpio5	S2_sdo				
51	Tggpio6	B	Tggpio6	S2_rgb0				
52	Tggpio7	B	Tggpio7	S2_rgb1				
53	Tggpio8	B	Tggpio8	S2_rgb2				
54	Tggpio9	B	Tggpio9	S2_rgb3				
55	Tggpio10	B	Tggpio10	S2_rgb4				
56	Tggpio11	B	Tggpio11	S2_rgb5				
57	Tggpio12	B	Tggpio12	S2_rgb6				
58	Tggpio13	B	Tggpio13	S2_rgb7				
Global Control Pins								
1	Xtali	I	Crystal pad input (6MHz/12MHz/24MHz/27MHz/48MHz). Default 27MHz					
2	Xtalo	O	Crystal pad output					
3	xtalrtci	I	32768Hz crystal pad input					
4	xtalrtco	O	32768Hz crystal pad output					
5	suspend	O	USB suspend signal					
6	trap	O	IO-trap control signal.					
7	prstnn	I	Power-on reset to SPCA536					
8	testmode	I	Test mode. This pin must be at low state during normal operation.					
ADC Interface								
1	CHD	I	For flash-light cut-off					
2	CHC	I	For UI interface					
3	CHB	I	For battery power detection					
4	AGCOUT	O	1st stage Amplifier Output					
5	ADCVREF	O	ADC voltage reference. It must connect to ground via a 0.1uF capacitor.					
6	OPO	O	2nd stage Amplifier output					
7	OPI	I	2nd stage Amplifier input					
8	AGC	I	AGC Gain Control					
9	MICN	I	Micro-phone input-					
10	MICP	I	Micro-phone input+					

Pin No.	Pin Name	Dir.	Description	Memo
			Video DAC	
1	DACVREF	I	DAC voltage reference. It must connect to ground via a 0.1uF capacitor.	
2	COUT	O	Composite video signal output (composite video/G)	
3	ROUT	O	Composite video signal output (R)	
4	BOUT	O	Composite video signal output (B)	
5	RSET	I	DAC scale adjustment	
6	CBL	I	Connect to power via a 0.1uF capacitor	
7	CBU	I	Connect to power via a 0.1uF capacitor	
			Display Interface Controller	
			The digital TV interface supports a variety of display interfaces including CCIR601, CCIR656, EPSON, CASIO, GraintPlus and AU Optronics interface. Many of the interface pins can be used as GPIO's when their corresponding function is not implemented in the final application.	

			CCIR 656	CCIR 601 (8-bit)	CCIR 601 (16-bit)	UNIPAC AU CASIO 2G	Epson LCD	STN LCD	VGA TFT LCD	CASIO	Analog RGB panel
1	digtv0	B	DDX0	DDX0	DDX0	DDX0	DYIO	DI3	B0	DA0	
2	digtv1	B	DDX1	DDX1	DDX1	DDX1	FRYS	DI2	B1	DA1	
3	digtv2	B	DDX2	DDX2	DDX2	DDX2	FRYP	DI1	B2	DA2	
4	digtv3	B	DDX3	DDX3	DDX3	DDX3	YSCL	DI0	B3	DA3	
5	digtv4	B	DDX4	DDX4	DDX4	DDX4	YSCLD	Frame	B4	DA4	
6	digtv5	B	DDX5	DDX5	DDX5	DDX5	XSCL	DF	B5	DA5	
7	digtv6	B	DDX6	DDX6	DDX6	DDX6	DA0	LP	G0	STBYB	
8	digtv7	B	DDX7	DDX7	DDX7	DDX7	DA1	XCK	G1	RIT	
9	digtv8	B	DCLK	FIELD	DDX8	DEM	DA2		G2	GSRT	
10	digtv9	B		HVLD	DDX9	VSD	DA3		G3	GRES	
11	digtv10	B		VVLD	DDX10	HSD	DA4		G4	POL	
12	digtv11	B		HSYNC	DDX11	DCLK	DA5		G5	STB	
13	digtv12	B		VSYNC	DDX12		RES		R0	STH	
14	digtv13	B		DCLK	DDX13		LP		R1	GPCK	
15	digtv14	B			DDX14		FRX		R2	CP	
16	digtv15	B			DDX15		GCP		R3	DCLK	
17	digtv16	B			FIELD				R4		
18	digtv17	B			HVLD				R5		
19	digtv18	B			VVLD				DVLD		
20	digtv19	B			HSYNC				HS		
21	digtv20	B			VSYNC				VS		
22	digtv21	B			DCLK				DCLK		

Storage Media Interface
The storage media interface supports most commonly used storage devices, including NAND-gate flash, SMC, MMC, SD, CFA and MS interface. Only one card (SMC, MMC, SD, CFA or MS) can be accessed at a time. The program ROM (NOR-type) is also accessed via this interface. Also, the extended memory interface allows SPCA536A to communicate with other external devices via an ISA-like protocol, such as and ISA Ethernet controller. When the extended memory interface is not used in the application, fmgpio[43:42] can be used as the secondary UART port.

Pin No.	Pin Name	Dir.	Description									Memo
		Dir	ROM	NAND-flash	External memory	SMC	SPI	SD	CFA (memory)	CFA (IDE)	MS/ MS-Pro	MS/SD
1	Fmgpio0	B	romoen									
2	Fmgpio1	B	romwrn	WP (O)								
3	Fmgpio2	B		CE/ (O)								
4	Fmgpio3	B		RDY (I)								
5	Fmgpio4	B	rom_d0	ALE (O)	IORB (O)	ALE (O)			CE1/ (O)	CS1/ (O)		
6	Fmgpio5	B	rom_d1	CLE (O)	IOWB (O)	CLE (O)			REG/ (O)	CS2/ (O)		
7	Fmgpio6	B				CD1 (I)	SCK (O)	SDAT3 (B)	CD1 (I)	CD1 (I)	MSDIO3(B)	SDDAT3 (B)
8	Fmgpio7	B				RDY (I)	RDY (I)	SDCLK (O)	WAIT/ (I)	IORDY (I)	MSDIO1(B)	SDCLK (O)
9	Fmgpio8	B				WP/ (O)	SI (I)	SDDAT0 (B)	RDY/ (I)	IRQ (I)	MSDIO0 (B)	SDDAT0 (B)
10	Fmgpio9	B		RE/ (O)		RE/ (O)	WP/ (O)	SDDAT1 (B)	RST/ (O)	RST/ (O)	MSCLK (O)	SDDAT1 (B)
11	Fmgpio10	B		WE/ (O)		WE/ (O)	SO/ (O)					MSCLK(O)
12	Fmgpio11	B				CE/ (O)	CS/ (O)	SDDAT2 (B)	WE/ (O)	WR/ (O)	MSDIO2 (B)	SDDAT2 (B)
13	Fmgpio12	B					RST/ (O)	SDCMD (B)	OE/ (O)	RD/ (O)	MSBS (O)	SDCMD/MSBS
14	Fmgpio13	B	rom_d2		SD0				A0 (O)	A0 (O)		
15	Fmgpio14	B	rom_d3	D0 (B)	SD1	D0 (B)			A1 (O)	A1 (O)		
16	Fmgpio15	B	rom_d4	D1 (B)	SD2	D1 (B)			A2 (O)	A2 (O)		
17	Fmgpio16	B	rom_d5	D2 (B)	SD3	D2 (B)			D0 (B)	D0 (B)		
18	Fmgpio17	B	rom_d6	D3 (B)	SD4	D3 (B)			D1 (B)	D1 (B)		
19	Fmgpio18	B	rom_d7	D4 (B)	SD5	D4 (B)			D2 (B)	D2 (B)		
20	Fmgpio19	B	rom_a0	D5 (B)	SD6	D5 (B)			D3 (B)	D3 (B)		
21	Fmgpio20	B	rom_a1	D6 (B)	SD7	D6 (B)			D4 (B)	D4 (B)		
22	Fmgpio21	B	rom_a2	D7 (B)	SD8	D7 (B)			D5 (B)	D5 (B)		
23	Fmgpio22	B	rom_a3		SD9				D6 (B)	D6 (B)		
24	Fmgpio23	B	rom_a4		SD10				D7 (B)	D7 (B)		
25	Fmgpio24	B	rom_a5		SD11				A3 (O)	D8 (B)		
26	Fmgpio25	B	rom_a6		SD12				A4 (O)	D9 (B)		
27	Fmgpio26	B	rom_a7		SD13				A5 (O)	D10 (B)		
28	Fmgpio27	B	rom_a8		SD14				A6 (O)	D11 (B)		
29	Fmgpio28	B	rom_a9		SD15				A7 (O)	D12 (B)		
30	Fmgpio29	B	rom_a10		SA0				A8 (O)	D13 (B)		
31	Fmgpio30	B	rom_a11		SA1				A9 (O)	D14 (B)		

Pin No.	Pin Name	Dir.	Description									Memo
32	Fmgpio31	B	rom_a12		SA2				A10 (O)	D15 (B)		
33	Fmgpio32	B	rom_a13		SA3							
34	Fmgpio33	B	rom_a14		SA4							
35	Fmgpio34	B	rom_a15		SA5							
36	Fmgpio35	B	rom_a16		SA6							
37	Fmgpio36	B	rom_a17		SA7							
38	Fmgpio37	B	rom_a18		SA8							
39	Fmgpio38	B	rom_a19		SA9							
40	Fmgpio39	B	rom_a20		SA10							
41	Fmgpio40	B	rom_a21		SA11							
					External memory	UART						
42	Fmgpio41				ANE (O)	Rxd1						
43	Fmgpio42				IORDY	Txd1						
EJTAG Interface (5 Pins)												
1	Jtagrstn	B	Test Reset Input					GPIO11				
2	Jtagclk	B	Test Clock Input					GPIO12				
3	Jtagtms	B	Test Mode Select Input					GPIO13				
4	Jtagtdi	B	Test Data Input					GPIO14				
5	Jtagtdo	B	Test Data Output					GPIO15		Audclk (O) (12/13.5/24/27MHz)		
UART Interface												
1	Rxd0	B	UART RX data 0					GPIO16			MSDIO2 (B)	
2	Txd0	B	UART TX data 0					GPIO17			MSDIO3 (B)	
USB2.0/External CPU Interface												
The USB2.0 UTMI interface, USB1.1 transceiver interface and the external CPU interface share the same physical pins. The function is determined by IO-trap values. Only one interface face can be activated for a specific application.												
			External CPU		USB2.0 UTMI			USB1.1		GPIO		
1	Utmi00	B	extcpu_csn		utmiclk			suspend11		Ugpio0		
2	Utmi01	B	extcpu_rdn		utmireset			usboe_n		Ugpio1		
3	Utmi02	B	extcpu_wrn		utmixverselect			Dpo		Ugpio2		
4	Utmi03	B	int_n		utmitermselect			Dmo		Ugpio3		
5	Utmi04	B	extcpu_a0		utmisuspendm			Dpi		Ugpio4		
6	Utmi05	B	extcpu_a1		utmilinestate0			Dmi		Ugpio5		
7	Utmi06	B	extcpu_a2		utmilinestate1			Din		Ugpio6		
8	Utmi07	B	extcpu_a3		utmiopmode0			pswon		Ugpio7		
9	Utmi08	B	extcpu_a4		utmiopmode1			Cpen		Ugpio8		
10	Utmi09	B	extcpu_a5		utmid0			Vcen		Ugpio9		
11	Utmi10	B	extcpu_a6		utmid1			Vbusd0		Ugpio10		
12	Utmi11	B	extcpu_a7		utmid2			Vbusd1		Ugpio11		
13	Utmi12	B	extcpu_a8		utmid3			Vbusd2		Ugpio12		
14	Utmi13	B	extcpu_a9		utmid4			Dpu		Ugpio13		
15	Utmi14	B	extcpu_a10		utmid5			hpd0		Ugpio14		
16	Utmi15	B	extcpu_a11		utmid6			hpd1		Ugpio15		
17	Utmi16	B	extcpu_a12		utmid7			vbuspu		Ugpio16		

Pin No.	Pin Name	Dir.	Description				Memo
18	Utmi17	B	extcpu_a13	utmid8	vbuspd	Ugpio17	
19	Utmi18	B	extcpu_a14	utmid9	otgaen	Ugpio18	
20	Utmi19	B	extcpu_a15	utmid10	Ugpio19	Ugpio19	
21	Utmi20	B	extcpu_d0	utmid11	Ugpio20	Ugpio20	
22	Utmi21	B	extcpu_d1	utmid12	Ugpio21	Ugpio21	
23	Utmi22	B	extcpu_d2	utmid13	Ugpio22	Ugpio22	
24	Utmi23	B	extcpu_d3	utmid14	Ugpio23	Ugpio23	
25	Utmi24	B	extcpu_d4	utmid15	Ugpio24	Ugpio24	
26	Utmi25	B	extcpu_d5	utmitxv	Ugpio25	Ugpio25	
27	Utmi26	B	extcpu_d6	utmivh	Ugpio26	Ugpio26	
28	Utmi27	B	extcpu_d7	utmitxrdy	Ugpio27	Ugpio27	
29	Utmi28	B	Ugpio28	utmirxv	Ugpio28	Ugpio28	
30	Utmi29	B	Ugpio29	utmirxa	Ugpio29	Ugpio29	
31	Utmi30	B	Ugpio30	utmirxer	Ugpio30	Ugpio30	
Digital Audio Interface							
SPCA536A support Digital AC-97 codec interface (AC-link), IIS interface and PWM outputs. The feature is decided by register.							
			AC-97 interface	IIS interface	PWM function	GPIO	
1	Audp0	B	Aurst_n (O)	IIS_CLK (O)	PWMLP (O)	Agpio0	
2	Audp1	B	Ausync (O)	LRCK (O) (The Left/Right clock)	PWMLM (O)	Agpio1	
3	Audp2	B	Audout (O)	IIS_DATA (O) (serial data)	PWMRP(O)	Agpio2	
4	Audp3	B	Aubclk (I)	Agpio3	PWMRM (O)	Agpio3	
5	Audp4	B	Audin (I)	Agpio4	Agpio4	Agpio4	
6	Audp5	B	Agpio5	Agpio5	Agpio5	Agpio5	
GPIO							
			GPIO	PWM Pattern Generator	MS/SD mode		
1	Gpio0	B	General purpose IO pin	PG0			
2	Gpio1	B	General purpose IO pin	PG1			
3	Gpio2	B	General purpose IO pin	PG2			
4	Gpio3	B	General purpose IO pin	PG3	MSDIO0 (B)		
5	Gpio4	B	General purpose IO pin	PG4	MSDIO1 (B)		
6	Gpio5	B	General purpose IO pin	PG5			
7	Gpio6	B	General purpose IO pin	PG6			
8	Gpio7	B	General purpose IO pin	PG7			
9	Gpio8	B	General purpose IO pin				
10	Gpio9	B	General purpose IO pin				
11	Gpio10	B	General purpose IO pin				
USB1.1 Interface							
1	Dp	B	USB data plus.				
2	dm	B	USB data minus.				
Power/Ground Pins							
1	Dvdd1		Core power 1.8V				
2	Dvdd2		Core power 1.8V				
3	Dvdd3		Core power 1.8V				

Pin No.	Pin Name	Dir.	Description	Memo
4	Dvdd4		Core power 1.8V	
5	Dvdd5		Core power 1.8V	
6	Dvdd6		Core power 1.8V	
7	Ovdd1		IO power 3.3V for SDRAM	
8	Ovdd2		IO power 3.3V for SDRAM	
9	Ovdd3		IO power 3.3V	
10	Ovdd4		IO power 3.3V	
11	Ovdd5		IO power 3.3V	
12	Ovdd6		IO power 3.3V	
13	Ovdd7		IO power 3.3V	
14	Ovdd8		IO power 3.3V (PLL)	
15	Ovdd9		IO power 3.3V	
16	Ovdd10		IO power 3.3V	
17	Dvss1		Ground	
18	Dvss2		Ground	
19	Dvss3		Ground	
20	Dvss4		Ground	
21	Dvss5		Ground	
22	Dvss6		Ground	
23	Ovss1		Ground	
24	Ovss2		Ground	
25	Ovss3		Ground	
26	Ovss4		Ground	
27	Ovss5		Ground	
28	Ovss6		Ground	
29	Ovss7		Ground	
30	Ovss8		Ground	
31	Ovss9		Ground	
32	Ovss10		Ground	
33	Add1		Analog power 3.3V for Video DAC	
34	Avss1		Analog ground	
35	Avdd2		Analog power 3.3V for ADC	
36	Avss2		Analog ground	
37	Uvdd		USB transceiver power 3.3V	
38	Uvss		USB transceiver ground	
39	Xvdd1		Main crystal power 3.3V	
40	Xvss1		Main crystal ground	
41	Xvdd2		RTC power 3.3V	
42	Xvss2		RTC ground	

4.2. IO-trap

While most configurations of the SPCA536A can be programmed by the firmware, there are some configurations those must be determined right after the chip is powered-on. The SPCA536A adopts IO-trap mechanism to set these configurations. These configurations are not changed for he entire power-up cycle of the SPCA536A. SPCA536A samples SDRAM address bus states

when the reset signal goes from low to high. In the application circuit, pull-up or pull-low resistors must be connected to the SDRAM address pins to set the IO-trap configuration. The “trap” pin is driven high during the IO-trap period. After the trapped values are latched internally, SPCA536A drives the “trap” signal low. The “trap” pin can be used to control the power of the pull-up resistors attached to the SDRAM address. The application circuit should make sure the pull-up resistors are only powered during the trap period to prevent from current leakage.

	Name	Description	Note
MA[1:0]	utmictrl[1:0]	“00”: UTMI[31:0] are used as GPIOs. In this setting, both internal CPU and on-chip USB transceiver are enabled. “01”: UTMI[31:0] are partly used as GPIOs. The internal CPU is enabled in this configuration. Whether to enable the on-chip transceiver is optional (programmable). “10”: UTMI[31:0] is used to interface with an off-chip UTMI transceiver. Internal CPU is enabled in this configuration. The on-chip USB transceiver is disabled. “11”: UTMI[31:0] is used as interface to an external CPU. In this configuration, The internal CPU is disabled. The on-chip USB transceiver is enabled.	
MA[2]	romdef	“0”: enable internal 16K-byte boot ROM “1”: SPCA536A boots from external (NOR-type) ROM	
MA[5:3]	xtal27i	”xx0”: SPCA536A is connected to a 27 MHz crystal “001”: SPCA536A is connected to a 6 MHz crystal “011”: SPCA536A is connected to a 12 MHz crystal “101”: SPCA536A is connected to a 24 MHz crystal “111”: SPCA536A is connected to a 48 MHz crystal Note that a 27MHz crystal must be connected to SPCA536A when composite TV output function is implemented.	
MA[6]	Fastrsten	“0”: Normal mode (10 ms reset), The internal circuit reset the SPCA536A core for 10ms to ensure the phase lock loop is stable. “1”: Fast reset (32 crystal clock), used for chip test only.	
MA[7]	EJTAGen	”0”: disable EJ probe interface “1”: enable EJ probe interface	
MA[8]	reserved		
MA[9]	nandfw	This bit is check by the boot code “0”: ISP function “1”: Firmware code is in NAND-type flash memory	
MA[12:10]	Dramtype[2:0]	The boot code checks these bits and set the corresponding SDRAM interface control registers so that the SDRAM can be accessed by the boot code when necessary. “000”: SDR, 16M bits x 1 (or x2) “001”: SDR, 64M bits x 1, 4 banks “010”: SDR, 128M bits x 1, 4 banks “011”: SDR, 256M bits x 1, 4 banks “100”: 512M bits x 1, 4 banks	
MA[14:13]	spare	These spare IO-trap signals are reserved for future function extension	

Note1: If I/O trap selects booting firmware code from NAND, the GPIO13 & GPIO14 shall be set to high. These two pins are used for power hold of camera and LED indicator for boot up.

Note2: If I/O trap selects executing ISP from internal ROM or executing the EJTAG function, the GPIO13 & GPIO14 shall be set to high and the UTMI01 shall be set to high to pull up the external 1.5K resistor on USB D+ signal.

5.ELECTRICAL SPECIFICATIONS

5.1. Absolute Maximum Rating

Table 5.1 Absolute Maximum Rating

Parameter	Symbol	Value	Unit
Voltage on any pin relative to VSS	VT	-0.4 to 4.0	V
Supply Voltage relative to VSS	VDD	-0.4 to 4.0	V
Operating Temperature	TOPT	0 to +70	°C
Storage Temperature	TSTG	-55 to 125	°C

5.2. DC Characteristics (T_A＝25℃, VDD＝3.3V±5%, VSS＝0V)

Table 5.2.1 DC Characteristics (T_A＝25℃, VDD–VSS＝3.3V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	I/O operating voltage	3.0	3.3	3.6	V
VDD	Core operating voltage	1.7	1.8	2.0	V
I_{DD}	$I_{I/O}$ (Unconfigured)	-	20.5	-	mA
	I_{Core} (Unconfigured)	-	57.6	-	
I_{DD}	$I_{I/O}$ (Suspend)	-	23.64	50	μA
	I_{Core} (Suspend)				
I_{DD}	$I_{I/O}$ (PC Camera)	-	26.16	-	mA
	I_{Core} (PC Camera)	-	122.37	-	
I_{DD}	$I_{I/O}$ (Preview)	-	31.56	-	mA
	I_{Core} (Preview)	-	94.37	-	
I_{DD}	$I_{I/O}$ (Analog TV)	-	65.4	-	mA
	I_{Core} (Analog TV)	-	136.73	-	
I_{DD}	$I_{I/O}$ (Video Clip)	-	29.46	-	mA
	I_{Core} (Video Clip)	-	136.17	-	

Table 5.2.2 DC Characteristics (T_A＝25℃, VDD–VSS＝3.3V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Input low voltage	-0.3	-	0.3 VDD	V
V_{IH}	Input high voltage	0.7 VDD	-	VDD+10%	V
I_{OL}	Output low current	-	4	-	mA
I_{OH}	Output high current	-	-4	-	mA
I_{OL}	Output low current	-	8	-	mA
I_{OH}	Output high current	-	-8	-	mA
I_{OL}	Output low current	-	12	-	mA
I_{OH}	Output high current	-	-12	-	mA
V_{T+}	Schmitt trigger positive-going threshold		1.5		V
V_{T-}	Schmitt trigger negative-going threshold		1.2		V
V_{HYS}	Hysteresis voltage		0.3		V
I_{IL}	Input leakage current			1	μA

5.3. RTC Parameters

Table 5.3 RTC Current Consumption

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{RTC}	Current Consumption, V_{RTC} =3.3V	-	2	-	μA

RTC accuracy: +/- 2.5 seconds/day

5.4. USB Interface

5.4.1. USB DC characteristics

Table 5.4.1 USB DC Electrical Characteristic

Symbol	Parameter	Min.	Typ.	Max.	Unit
Input Levels					
V_{IH}	Input level high (driven)	2.0	-	-	V
V_{IHZ}	Input level high (floating)	2.7	-	3.6	V
V_{IL}	Input level low	-	-	0.8	V
V_{DI}	Differential input sensitivity	0.2	-	-	V
Output Levels					
V_{OL}	Output level low	0.0	-	0.3	V
V_{OH}	Output level high	2.8	-	3.6	V
V_{CRS}	Output signal crossover voltage	1.3	-	2.0	V

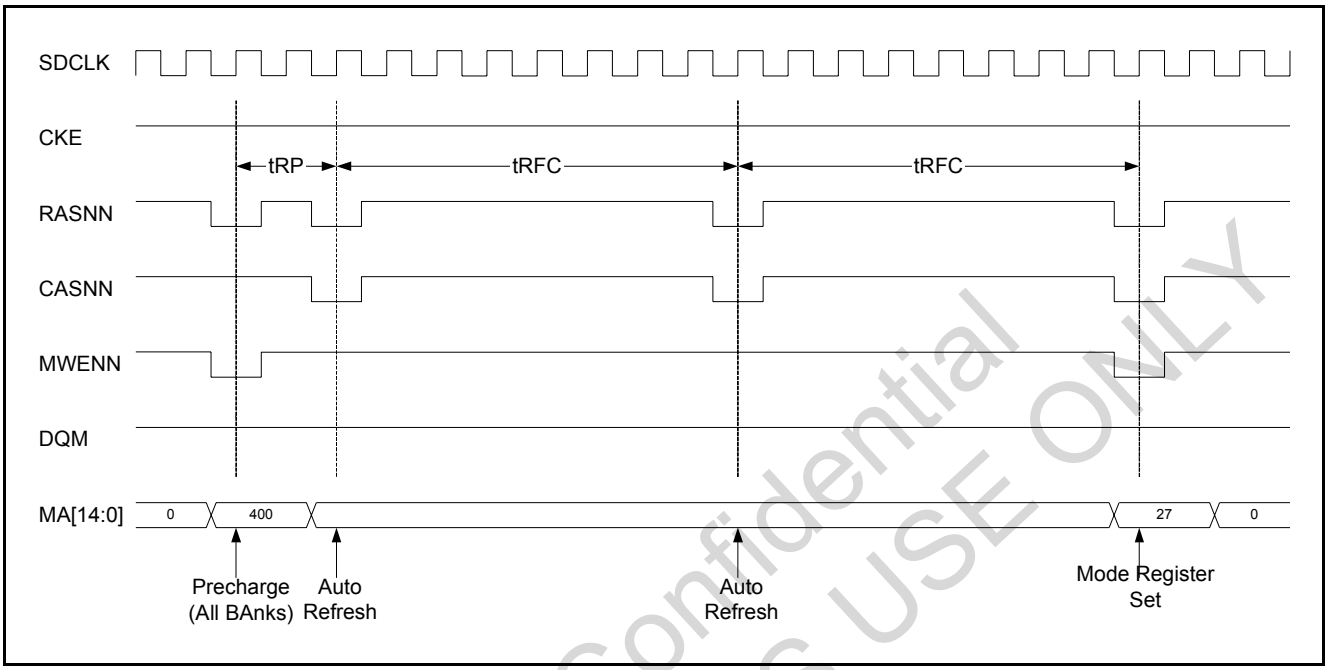
5.4.2. USB AC Characteristics

Table 5.4.2 USB AC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
Driver Characteristics					
T_{FR}	Rise time	4	-	20	ns
T_{FF}	Fall time	4	-	20	ns
T_{RFM}	Differential rise and fall time matching (T_{FR}/T_{FF})	90	-	111.11	%
Clock Timing					
T_{FDRATE}	Average bit rate	11.97	-	12.03	Mb/s
Full Speed Data Timing					
T_{DJ1}	Source jitter to next transition	-3.5	-	3.5	ns
T_{DJ2}	Source jitter for paired transition	-4	-	4	ns
T_{FDEOP}	Source jitter for differential transition to SE0 transition	-2	-	5	ns
T_{JR1}	Receiver jitter to next transition	-18.5	-	18.5	ns
T_{JR2}	Receiver jitter for paired transition	-9	-	9	ns
T_{FEOPT}	Source SE0 interval of EOP	160	-	175	ns
T_{FEOPR}	Receiver SE0 interval of EOP	82	-	-	ns

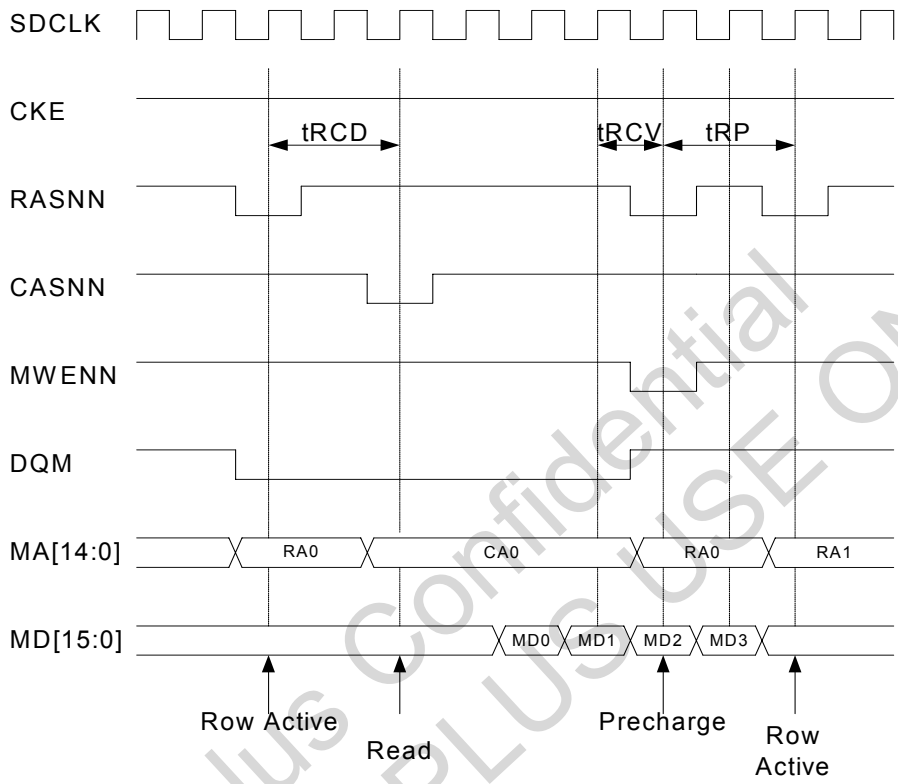
5.5. SDRAM Interface Timing

5.5.1. SDRAM initialization timing



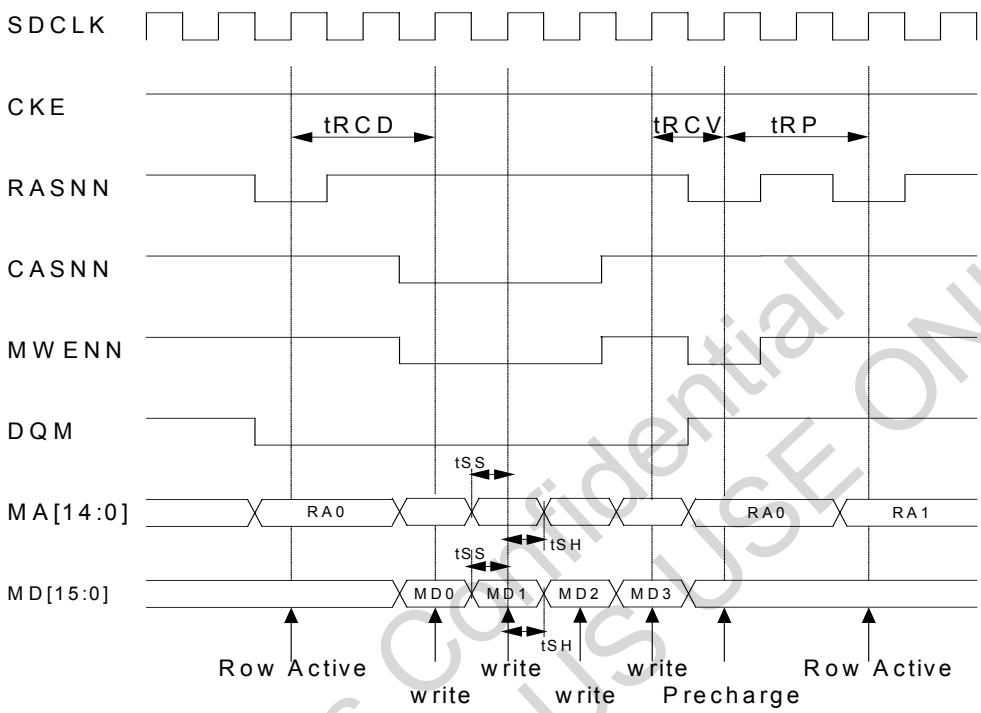
Parameter	Description	Min.	Typ.	Max.	Units
tRP	Row pre-charge time	80.0	83.3	--	ns
tRFC	Auto refresh cycle time	160.0	166.7	--	ns

5.5.2. SDRAM Page mode read timing



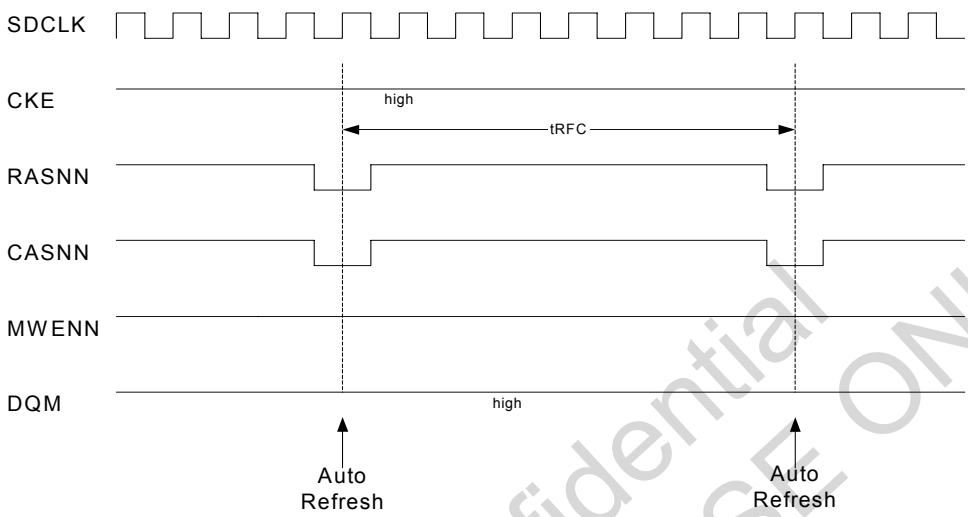
Parameter	Description	Min.	Typ.	Max.	Units
tRCD	RAS to CAS delay	20.0	20.8	--	ns
tRCV	Recovery time	20.0	20.8	--	ns
tRP	Row pre-charge time	40.0	41.7	--	ns

5.5.3. SDRAM Page mode write timing



Parameter	Description	Min.	Typ.	Max.	Units
tRCD	RAS to CAS delay	20.0	20.8	--	ns
tRCV	Recovery time	20.0	20.8	--	ns
Trp	Row pre-charge time	40.0	41.7	--	ns
MA tSS	Input Setup time	--	8.0	--	ns
MA tSH	Input Hold time	--	10.5	--	ns
MD tSS	Input Setup time	--	9.0	--	ns
MD tSH	Input Hold time	--	10.0	--	ns

5.5.4. SDRAM Auto Refresh Timing

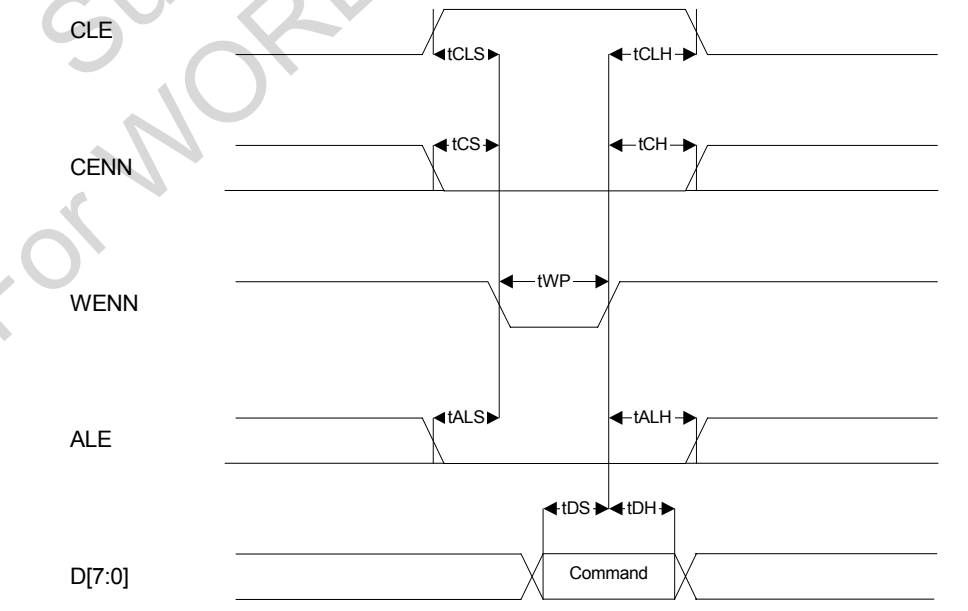


Parameter	Description	Min.	Typ.	Max.	Units
tRFC	Auto refresh cycle time	160.0	166.7	---	ns

5.6. Flash Memory Interfaces

5.6.1. NAND gate flash timing

5.6.1.1. NAND gate flash command latch cycle

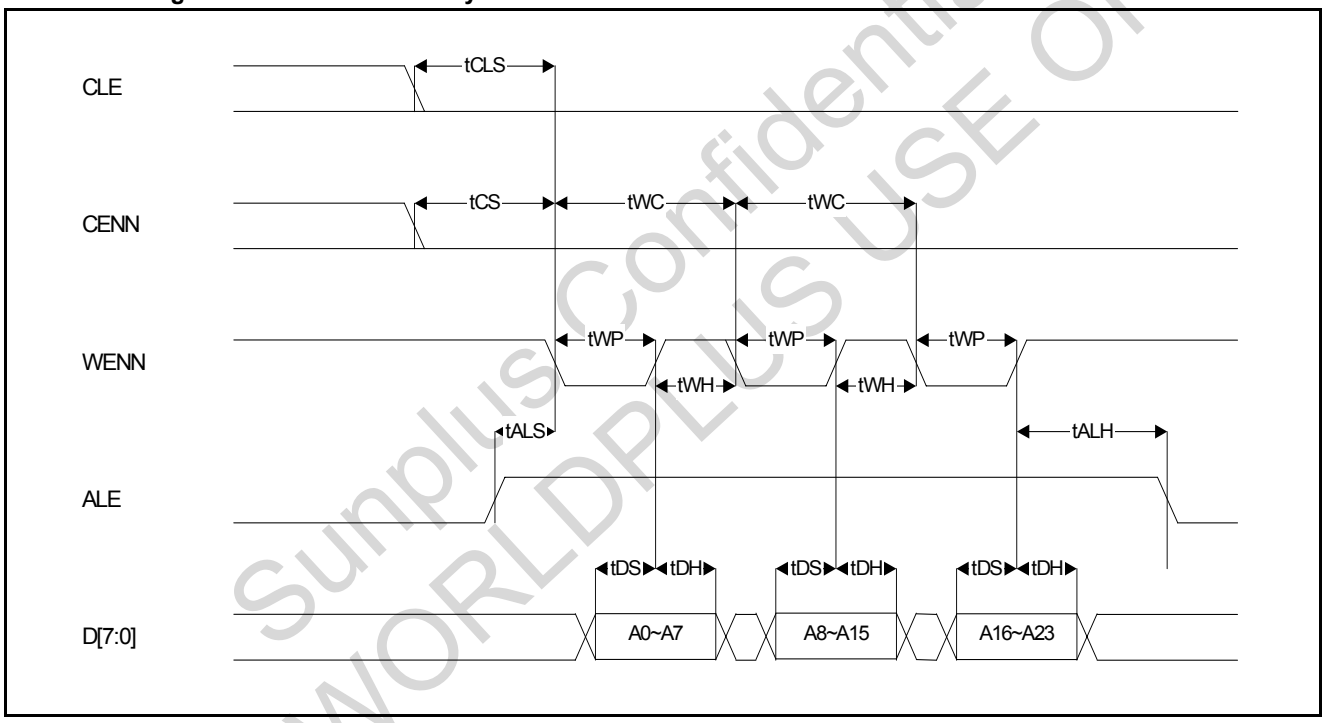


NAND Gate Flash Timing, Command Latch Cycle

Symbol	Parameter	Min.	Typ.	Max.	Unit
tCLS	CLE setup time	1120	-	-	ns
tCLH	CLE hold time	1120	-	-	ns
tCS	CENN setup time	1120	-	-	ns
tCH	CENN hold time	1120	-	-	ns
tWP	WENN pulse width	80	-	-	ns
tALS	ALE setup time	1120	-	-	ns
tALH	ALE hold time	1120	-	-	ns

Note: Timings are programmable

5.6.1.2. NAND gate flash address latch cycle



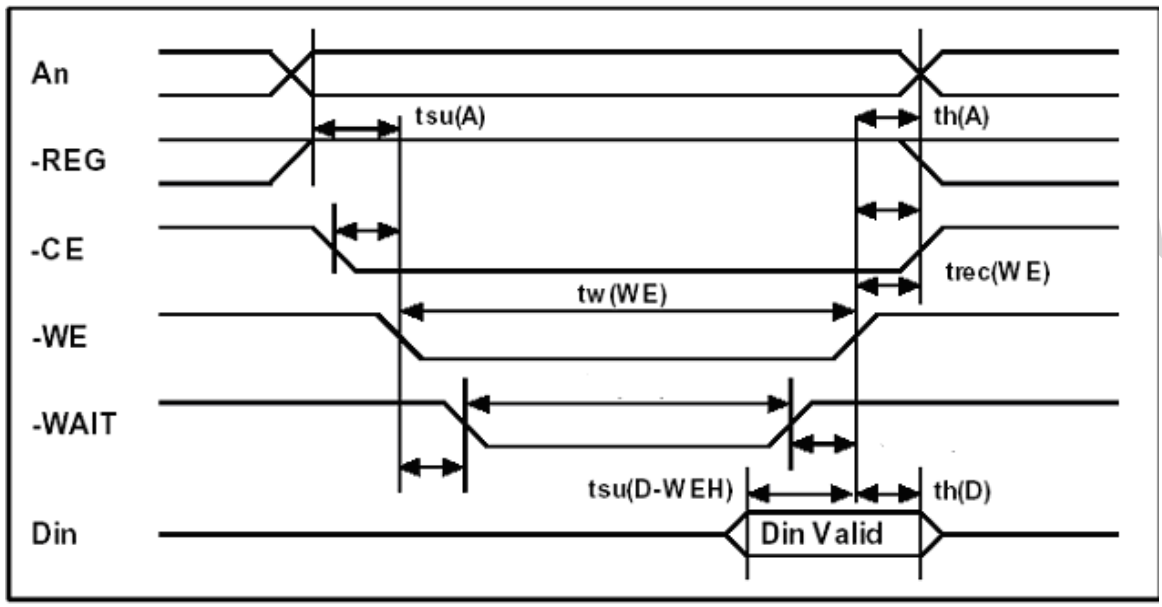
NAND Gate Flash Timing, Address Latch Cycle

Symbol	Parameter	Min.	Typ.	Max.	Unit
tCLS	CLE setup time	1120	-	-	ns
tCS	CENN setup time	1120	-	-	ns
tWC	Write cycle time	320	-	-	ns
tWP	WENN pulse width	80	-	-	ns
tWH	WENN high hold time	240	-	-	ns
tALS	ALE setup time	1120	-	-	ns
tALH	ALE hold time	1120	-	-	ns
tDS	D[7:0] setup time	45	-	-	ns
tDH	D[7:0] hold time	20	-	-	ns

Note: Timings are programmable

5.6.2. Compact flash card interface

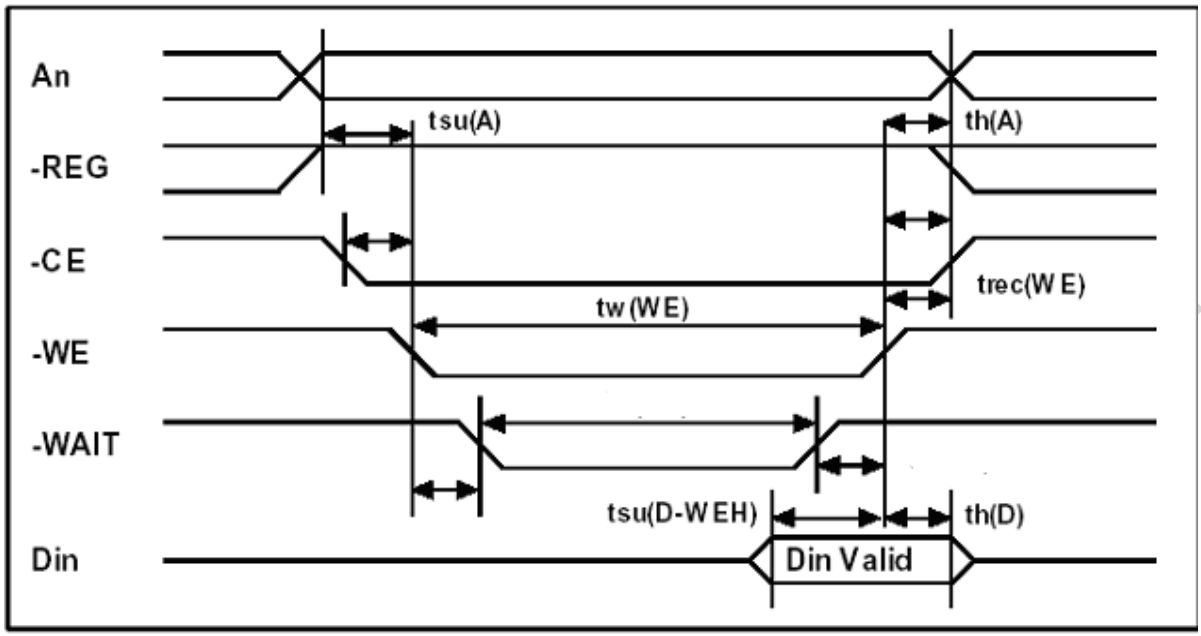
5.6.2.1. Common memory read



Symbol	Parameter	Min.	Typ.	Max.	Unit
ta(OE)	Output enable access time	-	44.0	125	ns
tdis(OE)	Output disable time from OE	0	292.0	-	ns
tsu(A)	Address setup time	1000	-	-	ns
th(A)	Address hold time	1000	-	-	ns
tsu(CE)	CE setup before OE	1000	-	-	ns
th(CE)	CE hold following OE	1000	-	-	ns

Note: Timings are programmable

5.6.2.2. Common Memory Write

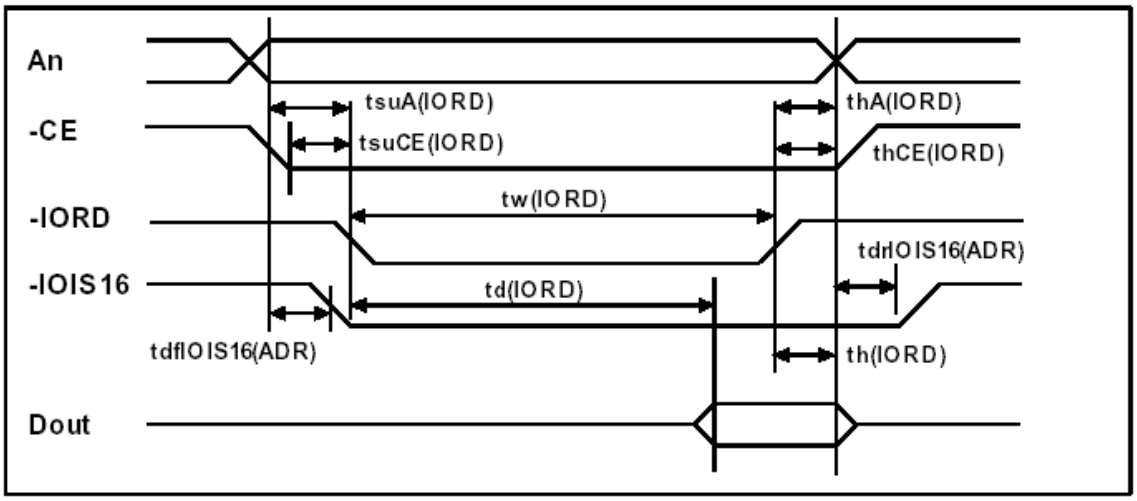


Compact Flash Timing - Attribute Memory Write

Symbol	Parameter	Min.	Typ.	Max.	Unit
tsu (D-WEH)	Data setup before WE	180	84.0	-	ns
th(D)	Data hold following WE	150	442.6	-	ns
tw(WE)	WE pulse width	150	80.0	-	ns
tsu(A)	Address setup time	1000	268.0	-	ns
tsu(CE)	CE setup before WE	1000	442.6	-	ns
th(A)	Address hold time	0	440.0	-	ns
th(CE)	CE hold following WE	1000	-	-	-

Note: Timings are programmable

5.6.2.3. Compact flash - True IDE Mode I/O Input (Read)

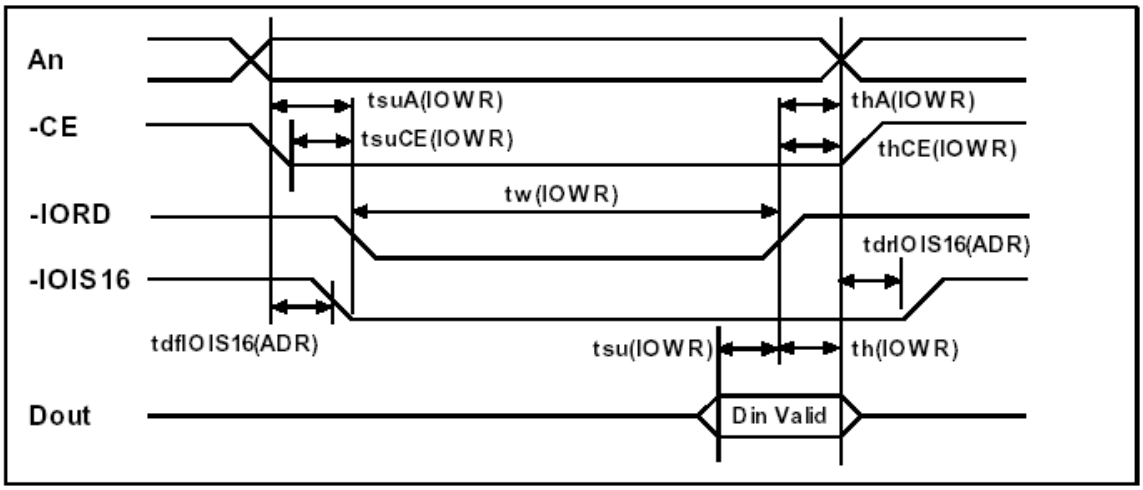


Compact Flash Timing True IDE Mode I/O Input (Read)

Symbol	Parameter	Min.	Typ.	Max.	Unit
td(IORD)	Data delay after IORD	-	41.3	100	ns
th(IORD)	Data hold following IORD	0	58.6	-	ns
tw (IORD)	IORD width time	165	165.0	-	ns
tsuA (IORD)	Address setup before IORD	1000	-	-	ns
thA (IORD)	Address hold following IORD	1000	-	-	ns
tsuCE (IORD)	CE setup before IORD	1000	-	-	ns
thCE (IORD)	CE hold following IORD	1000	-	-	ns

Note: Timings are programmable

5.6.2.4. Compact flash timing true IDE mode I/O output (write)

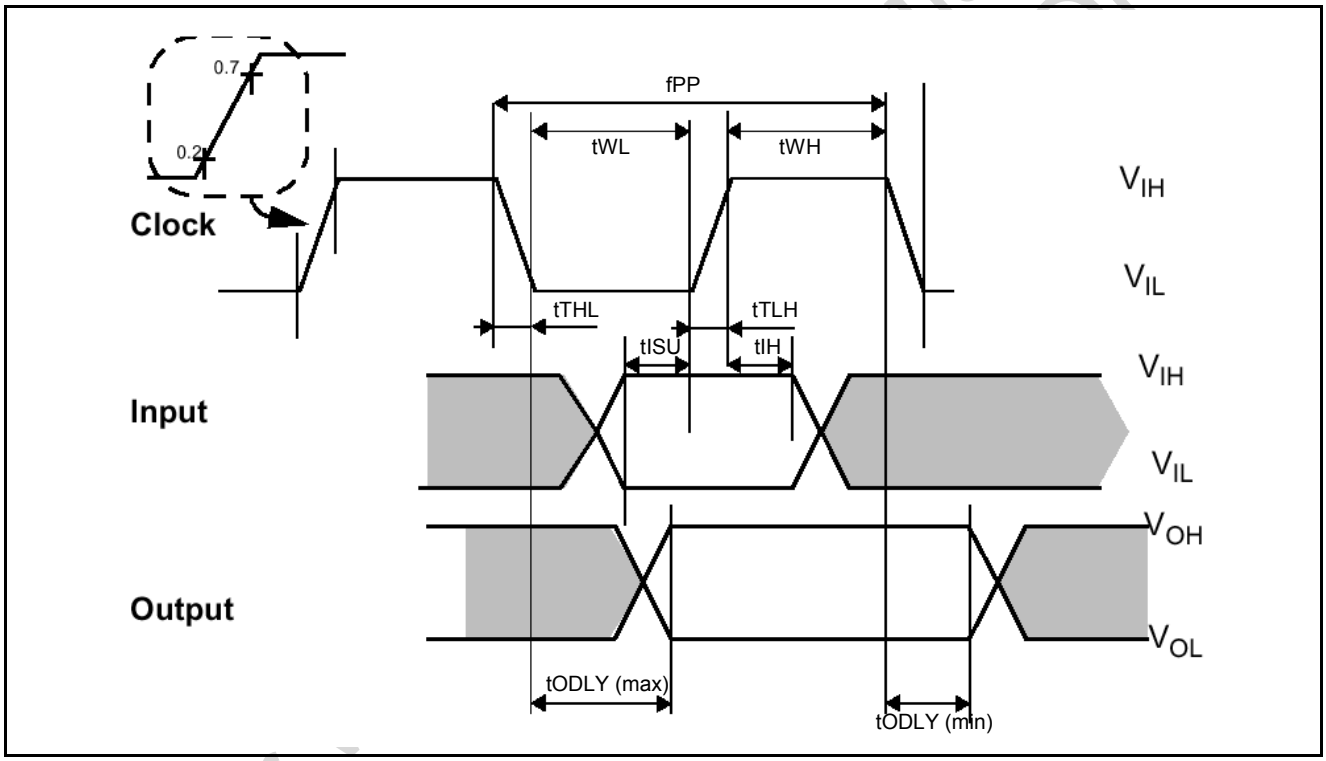


Compact Flash Timing True IDE Mode I/O Output (Write)

Symbol	Parameter	Min.	Typ.	Max.	Unit
tsu(IOWR)	Data setup before IOWR	1000	-	-	ns
th(IOWR)	Data hold following IOWR	1000	-	-	ns
tw(IOWR)	IOWR width time	0	-	-	ns
tsuA (IOWR)	Address setup before IOWR	1000	-	-	ns
thA (IOWR)	Address hold following IOWR	1000	-	-	ns
tsuCE (IOWR)	CE setup before IOWR	1000	-	-	ns
thCE (IOWR)	CE hold following IOWR	1000	-	-	ns

Note: Timings are programmable

5.6.3. Security digital memory card interface

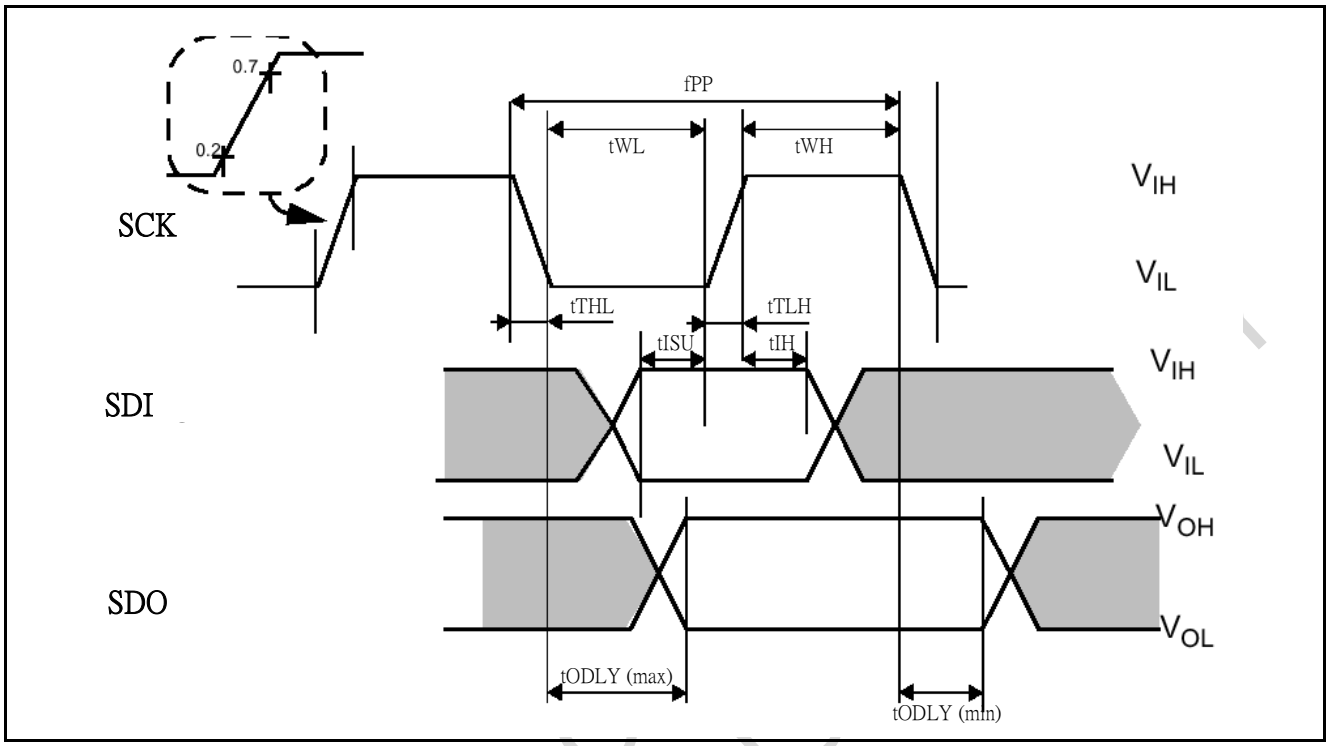


Security Digital Memory Card Interface Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
fPP	Clock frequency data transfer mode	0	24.0	-	MHz
tWL	Clock low time	10	12.7	-	ns
tWH	Clock high time	10	15.6	-	ns
tTLH	Clock rise time	-	5.8	-	ns
tTHL	Clock fall time	-	7.6	-	ns
Tisu	Input setup time	5	8.0	-	ns
tIH	Input hold time	0	14.4	-	ns
tODLY	Output delay time	0	7.6~8.4	-	ns

Note: ※ note CL≤100pF (7 Cards), ∗ note CL≤25pF (1 Card)

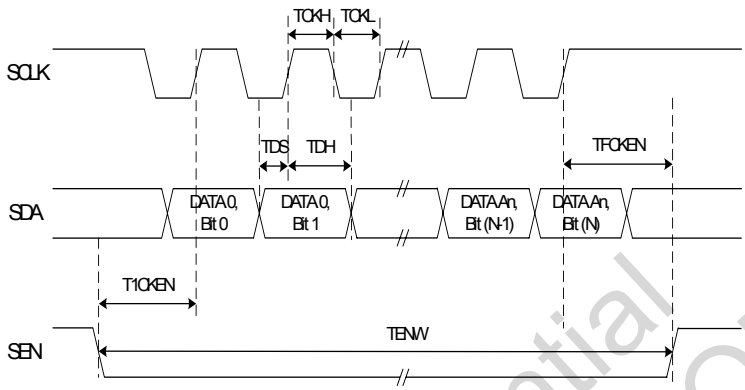
5.6.4. SPI-mode0



Symbol	Parameter	Min.	Typ.	Max.	Unit
fPP	Clock frequency data transfer mode	0	24.0	-	MHz
tWL	Clock low time	10	12.7	-	ns
tWH	Clock high time	10	15.6	-	ns
tTLH	Clock rise time	-	5.8	-	ns
tTHL	Clock fall time	-	7.6	-	ns
tISU	Input setup time	5	8.0	-	ns
tIH	Input hold time	0	14.4	-	ns
tODLY	Output delay time	0	7.6~8.4	-	ns

5.7. Synchronous Serial Interface Timing

5.7.1. Synchronous serial interface three-wire timing

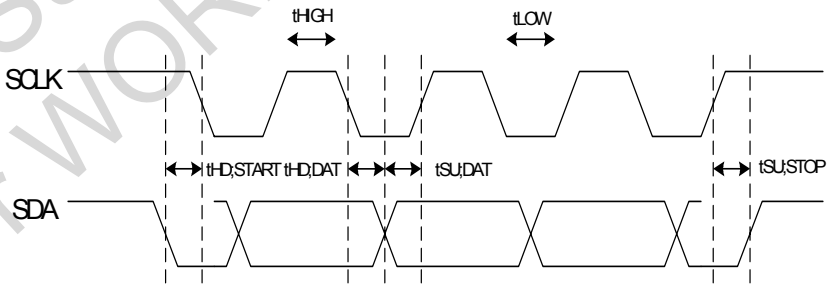


Synchronous Serial Interface Three-wire Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
TCKH	High Period of SCLK	-	2.04	-	µs
TCKL	Low Period of SCLK	-	2.04	-	µs
TDS	Data Set-up time	-	1.00	-	µs
TDH	Data Hold time	-	3.08	-	µs
T1CKEN	First Clock High before SEN	-	14.79	-	µs
TFCKEN	Final Clock High before SEN High	-	10.67	-	µs
TENW	SEN Plus Width	-	86.70	-	µs

Note: Default Value of Cntdiv [2904]＝0x30, Timings are programmable

5.7.2. Synchronous serial interface two-wire timing



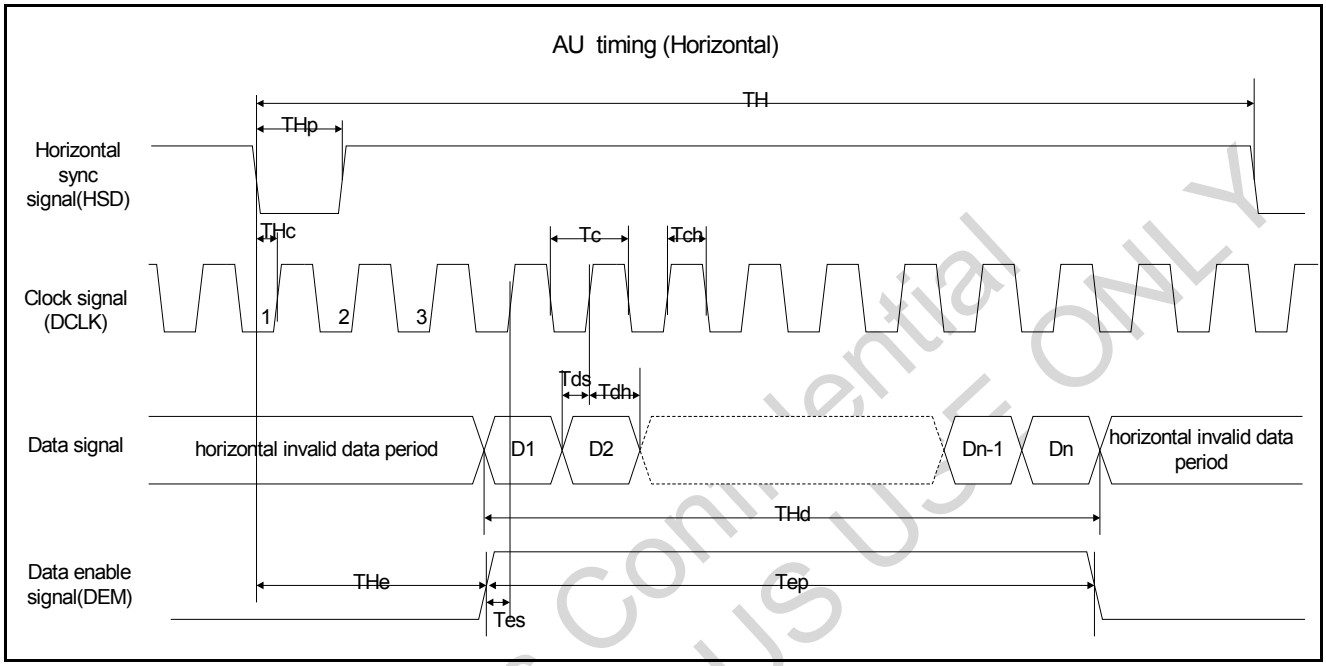
Synchronous Serial Interface Two-wire Timing

Symbol	Parameter	Min	Typ	Max	Unit
THIGH	High period of SCLK	-	2.58	-	µs
tLOW	Low period of SCLK	-	2.75	-	µs
THD; DAT	Data hold time	-	1.40	-	µs
TSU; DAT	Data set-up time	-	1.36	-	µs
THD; START	Hold time for start condition	-	1.34	-	µs
TSU; STOP	Set-up time for stop condition	-	1.37	-	µs

Note: Timings are programmable

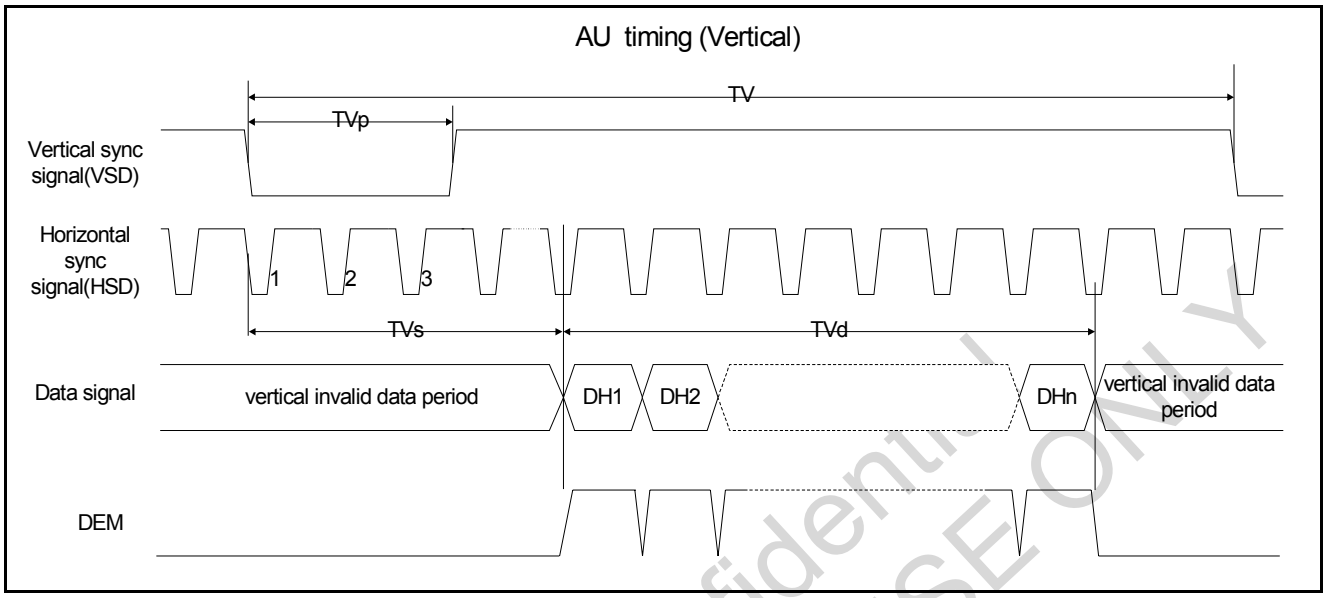
5.8. LCD Interface Timing

5.8.1. Horizontal



Symbol	Description		Min	TYP	Max	Unit
TH	HSD period		-	64.9	-	ms
			-	1477	-	Clk
THd	HSD display period		-	52.2	-	ms
			-	1185	-	Clk
THp	HSD pulse width		-	4	-	Clk
THc	HSD hsync-CLK timing		-	22.6	-	ns
Tc	DCLK period	Max	40.0	--	44.0	ns
		Min				
Tch	DCLK high time	Max	20.0	--	24.0	ns
		Min				
Tdh	CLK-DATA timing	Max	16.0	--	24.0	ns
		Min				
Tds	DATA-CLK timing	Max	16.0	-	21.3	ns
		Min				
THe	Goal timing		-	250	-	Clk
Tep	DEM pulse width		-	1185	-	Clk
Tes	DEM setup timing		-	22.7	-	ns

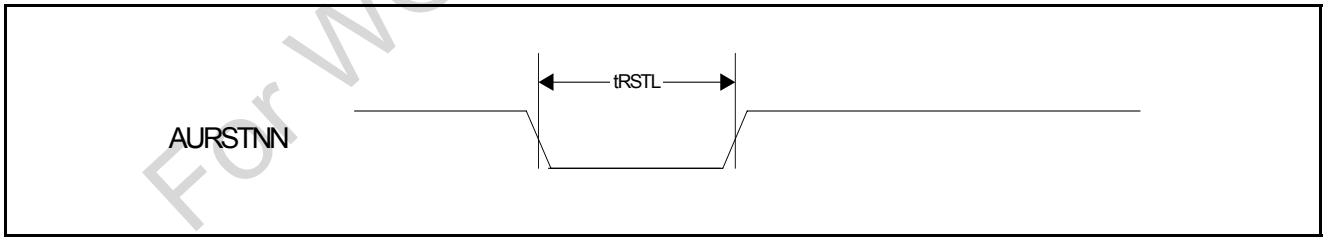
5.8.2. Vertical



Symbol	Description	Min.	Typ.	Max.	Unit
TV	VSD period	-	17.0	-	ms
TVd	VSD display period	-	14.4	-	ms
TVP	VSD pulse width	-	200.0	-	μs
TVS	Vertical display position	-	1.5	-	ms

5.9. AC97 Audio Interface Timing

5.9.1. AC97 cold reset timing

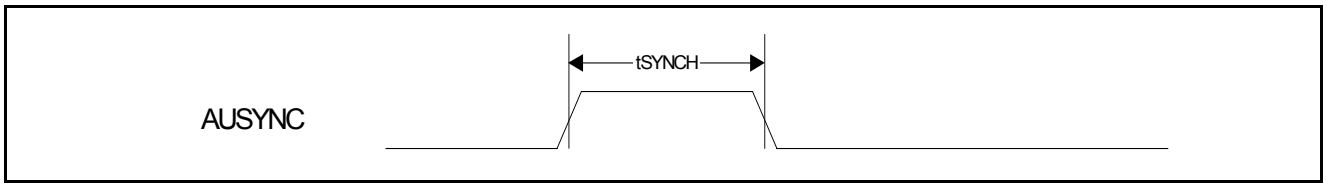


AC97 Cold Reset Timing

Symbol	Parameter	Min	Typ.	Max	Unit
TRSTL	Active low pulse width	1.0	-	-	μs

Note: Timings are programmable

5.9.2. AC97 Warm reset timing

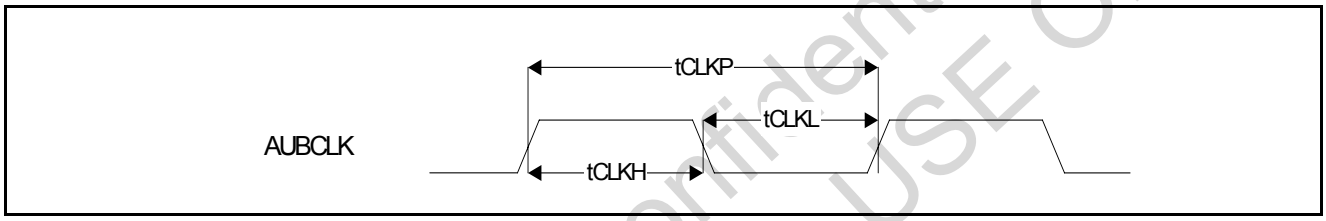


AC97 Warm Reset Timing

Symbol	Parameter	Min	Typ.	Max	Unit
tSYNCH	Active high pulse width	-	1.30	-	ms

Note: Timings are programmable

5.9.3. AC97 Clock Timing

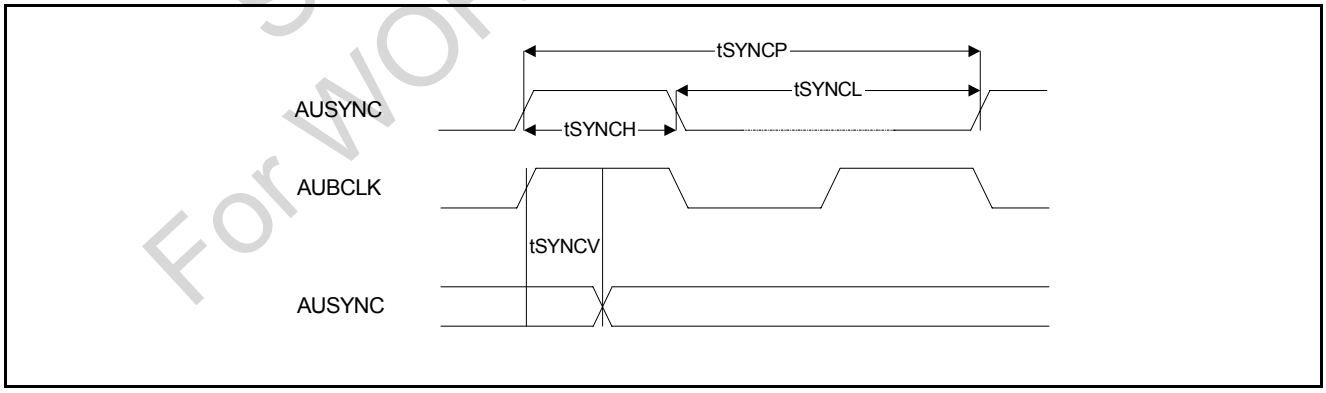


AC97 Clock Timing

Symbol	Parameter	Min	Typ	Max	Unit
tCLKH	Clock high pulse width	32.56	40.7	48.84	ns
tCLKL	Clock low pulse width	32.56	40.7	48.84	ns
tCLKP	Clock cycle time	-	81.4	-	ns

Note: Timings are programmable

5.9.4. AC97 Sync Timing

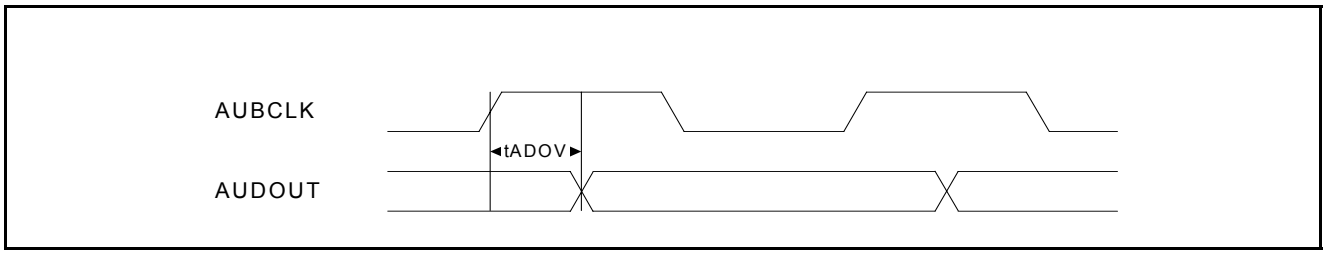


AC97 Sync Timing

Symbol	Parameter	Min	Typ.	Max	Unit
tSYNCH	SYNC high pulse width	-	16	-	aubclk
tSYNCL	SYNC low pulse width	-	240	-	aubclk
tSYNCP	SYNC period	-	256	-	aubclk

Note: Timings are programmable

5.9.5. AC97 Audio Data Output Timing

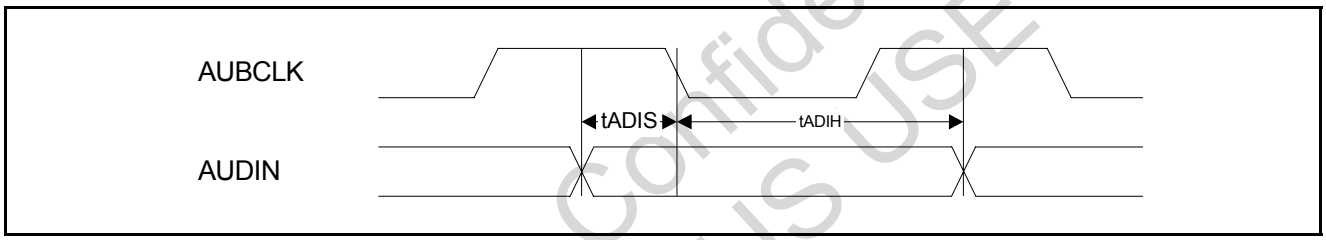


AC97 Audio Data Output Timing

Symbol	Parameter	Min	Typ.	Max	Unit
tADOV	AUDOUT valid delay	-	-	25	ns

Note: Timings are programmable

5.9.6. AC97 Audio Data Input Timing



AC97 Audio Data Input Timing

Symbol	Parameter	Min	Typ	Max	Unit
tADIS	AUDIN setup time	15	-	-	ns
tADIH	AUDIN hold time	5	-	-	ns

Note: Timings are programmable

5.10. Analog Audio Interface Characteristics

Audio ADC and DAC

Parameters	Condition	Min.	Typ.	Max.	Units
INL	differential input	-	-	1	LSB
DNL		-	-	1	LSB
THD+N(AGC)	1K sin input	-	-45	-	dB

5.11. Analog Video Interface Characteristics

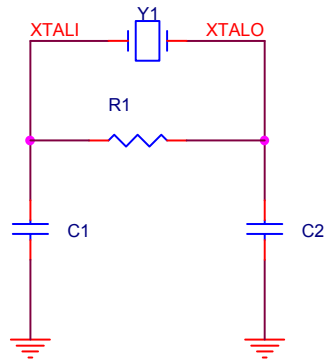
Video C DAC

Parameter	Condition	Min.	Typ.	Max.	Units
Power supply		3.0	3.3	3.6	V
Operating current		-	-	36	mA
Resolution		-	9	-	Bits
INL		-	±1	-	LSB
DNL		-	±0.5	-	LSB
Clock frequency		-	27	-	MHz
Output Voltage	R_{set}=1.5K	-	1.3	-	V
Settling time	Output at ±0.5LSB	-	-	25	ns
Glitch		-	60	-	pVsec

Video R/B DAC

Parameter	Condition	Min.	Typ.	Max.	Units
Power supply		3.0	3.3	3.6	V
Operating current		-	-	36	mA
Resolution		-	7	-	Bits
INL		-	±1	-	LSB
DNL		-	±0.5	-	LSB
Clock frequency		-	27	-	MHz
Output Voltage	R_{set}=1.5K	-	1.3	-	V
Settling time	Output at ±0.5LSB	-	-	25	ns
Glitch		-	60	-	pVsec

5.12. RTC Crystal Timing

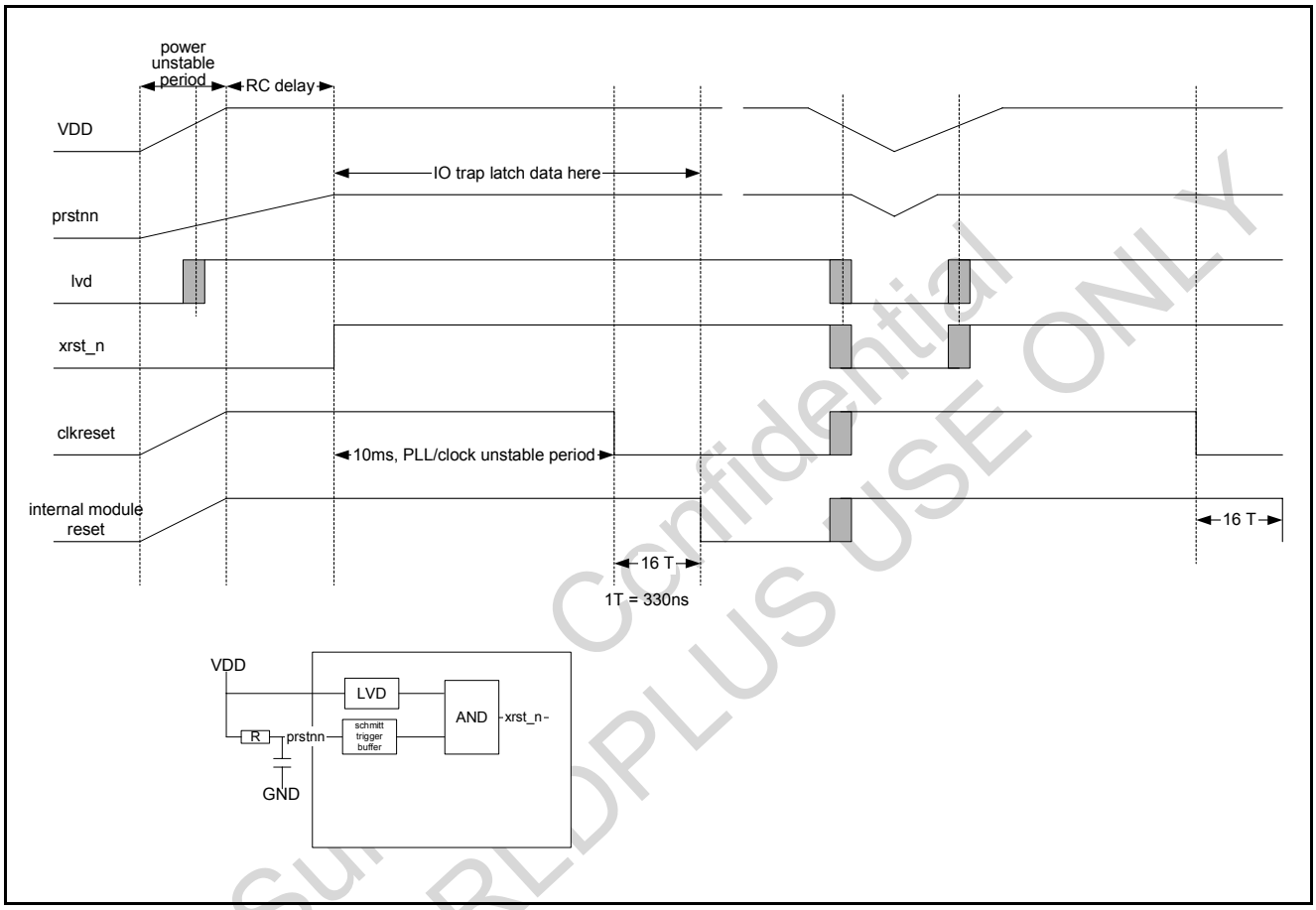


	Min.	Typ.	Max.	Unit
Resistor (R1)		NC*		Ohm
Capacitor (C1)	2.2	8.2	10	pF
Capacitor (C2)	2.2	8.2	10	pF

* NC: Not connected

5.13. Power-On Sequence

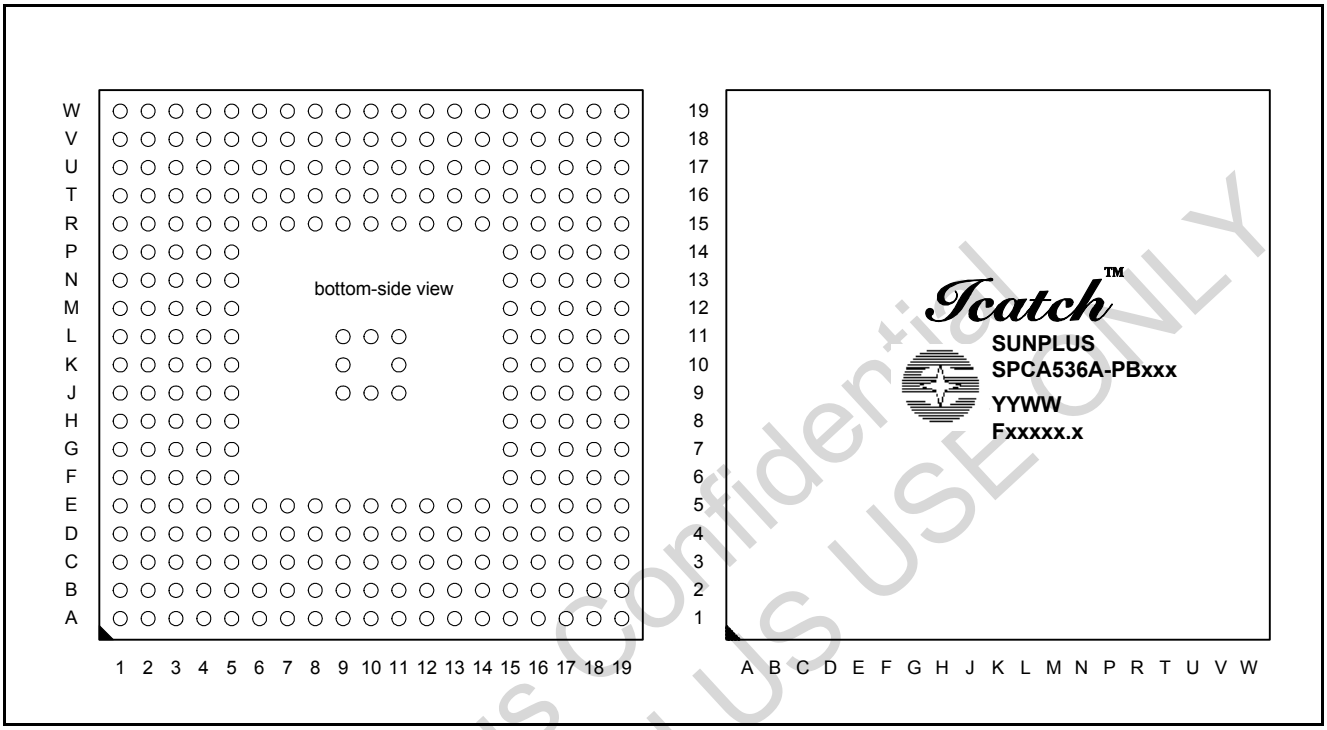
SPCA536A builds in a low-voltage detection function, which automatically reset the internal circuitry when the supply voltage is lower than 2.4 Volt.



6.PACKAGE/PAD LOCATION

6.1. TFBGA-288 Pin Assignments and Package Diagram

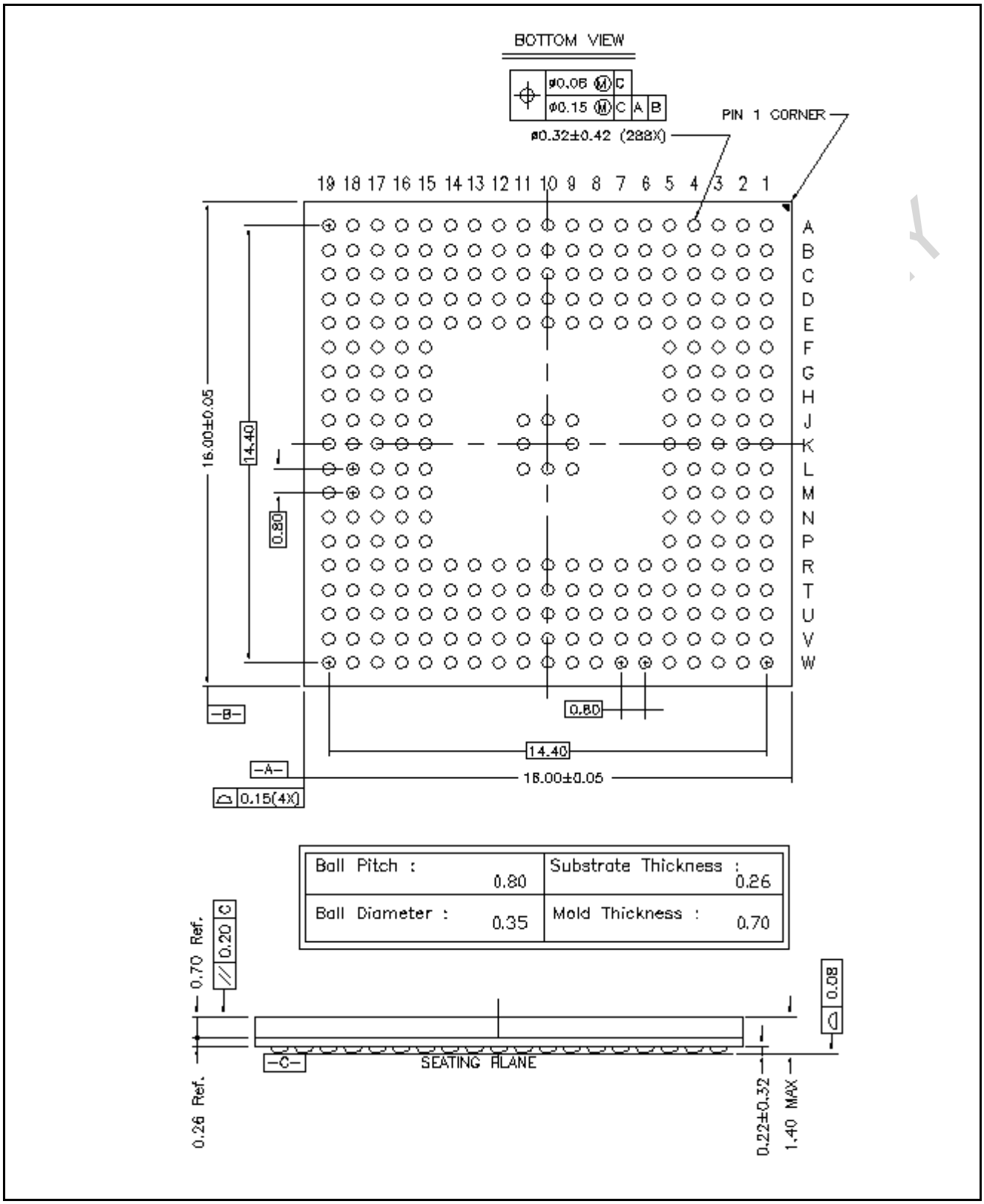
6.1.1. TFBGA-288 Pin assignments and mapping table



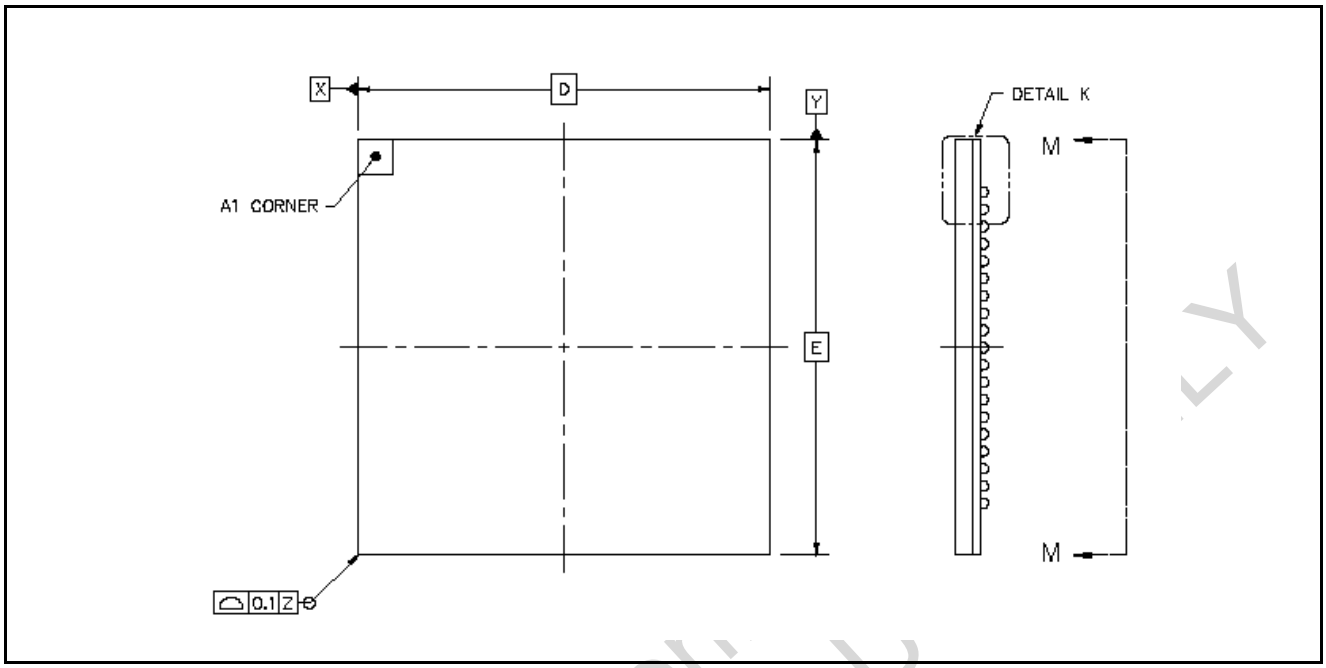
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A1	Utmi14	D2	Utmi21	H2	Md4	N2	Ldqm	U2	Ma13
A2	Utmi13	D3	Utmi20	H3	Md3	N3	Cke	U3	Digtv2
A3	Utmi10	D4	Utmi19	H4	Md2	N4	Ma0	U4	Digtv6
A4	Utmi7	D5	Utmi05	H5	**Uvss**	N5	**Dvss2**	U5	Digtc10
A5	Utmi2	D6	Utmi00	H15	**Xvdd2**	N15	**Ovdd7**	U6	Digtv14
A6	Fmgpio40	D7	Fmgpio38	H16	Audp0	N16	Rgb9	U7	Digtv18
A7	Fmgpio35	D8	Fmgpio34	H17	Jtagtdo	N17	Testmode	U8	Gpio6
A8	Fmgpio31	D9	Fmgpio30	H18	Jtagtdi	N18	Tgpio0	U9	Gpio10
A9	Fmgpio27	D10	Fmgpio26	H19	Jtagtms	N19	Tgpio1	U10	Cbl
A10	Fmgpio23	D11	Fmgpio19	J1	Md9	P1	Ma1	U11	Sg1b
A11	Fmgpio22	D12	Fmgpio15	J2	Md8	P2	Ma2	U12	Sg5b
A12	Fmgpio18	D13	Fmgpio11	J3	Md7	P3	Ma3	U13	Fs
A13	Fmgpio14	D14	Fmgpio7	J4	Md6	P4	Ma4	U14	Sen
A14	Fmgpio10	D15	Fmgpio3	J5	**Dvdd1**	P5	**Ovdd2**	U15	Sdo
A15	Fmgpio6	D16	Txd0	J9	**Ovss1**	P15	**Dvss5**	U16	V4
A16	Fmgpio2	D17	Xtalo	J10	**Ovss8**	P16	Rgb5	U17	Adclp
A17	Rxd0	D18	Xtali	J11	**Ovss7**	P17	Rgb6	U18	Obclp
A18	Gpio3	D19	micp	J15	**Xvss1**	P18	Rgb7	U19	Adck
A19	Gpio1	E1	Utmi26	J16	Jtagclk	P19	Rgb8	V1	Ma14
B1	Utmi16	E2	Utmi25	J17	Jtagrstn	R1	Ma5	V2	Digtv0
B2	Utmi15	E3	Utmi24	J18	Trap	R2	Ma6	V3	Digtv3
B3	Utmi11	E4	Utmi23	J19	Prstnn	R3	Ma7	V4	Digtv7
B4	Utmi8	E5	Utmi06	K1	Md13	R4	Ma8	V5	Digtv11
B5	Utmi3	E6	Utmi01	K2	Md12	R5	**Dvdd3**	V6	Digtv15
B6	Fmgpio41	E7	Fmgpio39	K3	Md11	R6	**Dvss3**	V7	Digtv19
B7	Fmgpio36	E8	**Ovss10**	K4	Md10	R7	**Ovdd3**	V8	Gpio7
B8	Fmgpio32	E9	**Ovdd10**	K5	**Dvss1**	R8	**Avdd1**	V9	Dacvref
B9	Fmgpio28	E10	**Dvss6**	K9	**Ovss2**	R9	**Avss1**	V10	rset
B10	Fmgpio24	E11	**Dvdd6**	K11	**Ovss6**	R10	**Ovdd4**	V11	Sg1a
B11	Fmgpio21	E12	**Ovss9**	K15	**Xvdd1**	R11	**Dvdd4**	V12	Sg5a
B12	Fmgpio17	E13	**Ovddd9**	K16	Tggpio10	R12	**Dvss4**	V13	Fcds
B13	Fmgpio13	E14	**Ovdd8**	K17	Tggpio11	R13	**Ovdd5**	V14	Vsubctrl
B14	Fmgpio9	E15	Micn	K18	Tggpio12	R14	**Ovdd6**	V15	Fr
B15	Fmgpio5	E16	Agc	K19	Tggpio13	R15	**Dvdd5**	V16	V3
B16	Fmgpio1	E17	Opi	L1	sdclk	R16	Rgb1	V17	V6
B17	Gpio5	E18	Adcvref	L2	Md14	R17	Rgb2	V18	V10
B18	Gpio2	E19	Opo	L3	Md15	R18	Rgb3	V19	V9
B19	Gpio0	F1	Dp	L4	Rasnn	R19	Rgb4	W1	Sdclknn
C1	Utmi18	F2	Utmi30	L5	**Ovdd1**	T1	Ma9	W2	Digtv1
C2	Utmi17	F3	Utmi29	L9	**Ovss3**	T2	Ma10	W3	Digtv4
C3	Utmi12	F4	Utmi28	L10	**Ovss4**	T3	Ma11	W4	Digtv8
C4	Utmi09	F5	Utmi27	L11	**Ovss5**	T4	Digtv5	W5	Digtv12

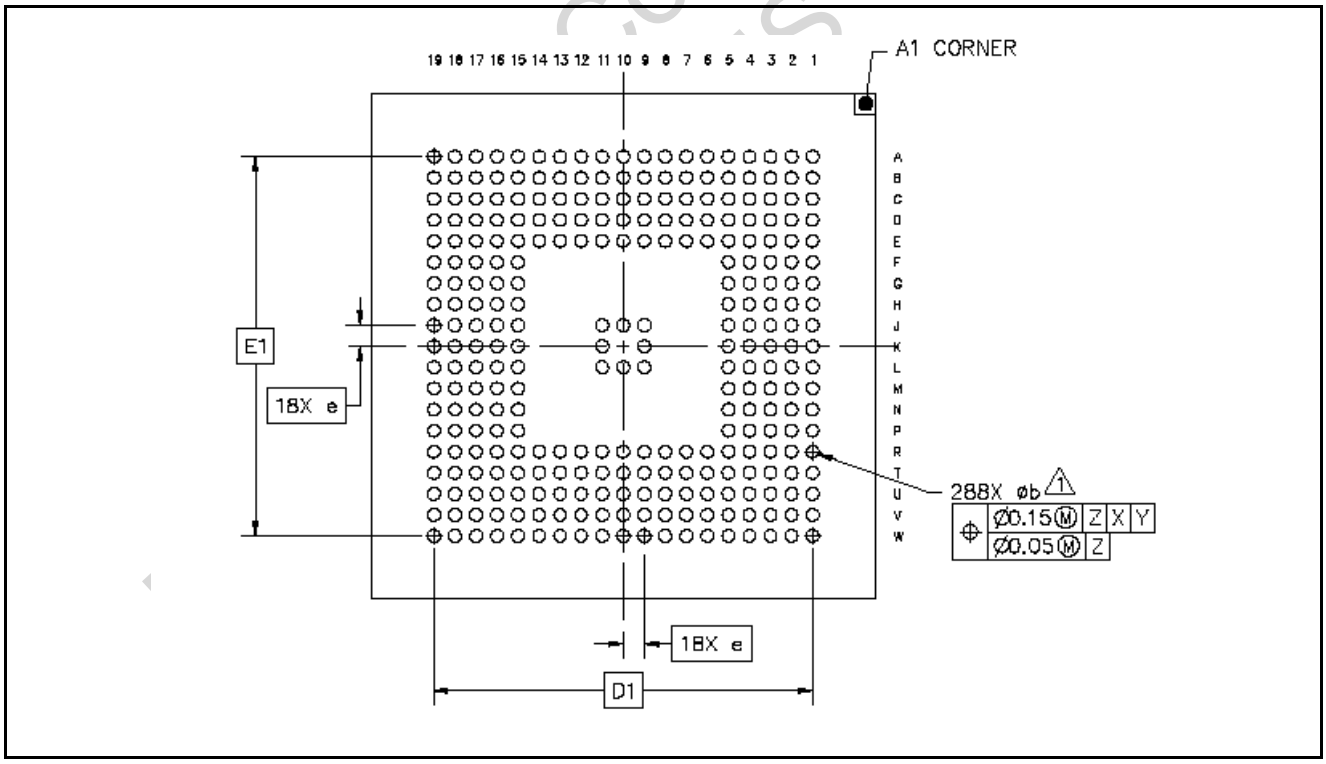
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
C5	Utmi04	F15	Agcout	L15	**Avss3**	T5	Digtv9	W6	Digtv16
C6	Fmgpio42	F16	Chb	L16	Tggpio6	T6	Digtv13	W7	Digtv20
C7	Fmgpio37	F17	Chc	L17	Tggpio7	T7	Digtv17	W8	Gpio8
C8	Fmgpio33	F18	Chd	L18	Tggpio8	T8	Digtv21	W9	Bout
C9	Fmgpio29	F19	Audp5	L19	Tggpio9	T9	Gpio9	W10	Cout
C10	Fmgpio25	G1	Dm	M1	Udqs	T10	Cbu	W11	Rout
C11	Fmgpio20	G2	Suspend	M2	Mwenn	T11	Sg3a	W12	Sg3b
C12	Fmgpio16	G3	Md1	M3	Casnn	T12	Sg7a	W13	Sg7b
C13	Fmgpio12	G4	Md0	M4	Udqm	T13	Sub	W14	Fh2
C14	Fmgpio08	G5	**Uvdd**	M5	**Dvdd2**	T14	Sck	W15	Fh1
C15	Fmgpio04	G15	**Xvss2**	M15	**Avdd3**	T15	V1	W16	V2
C16	Fmgpio00	G16	Audp4	M16	Tggpio2	T16	Pblk	W17	V5
C17	Gpio4	G17	Audp3	M17	Tggpio3	T17	Mshutter	W18	V7
C18	Xtalrtco	G18	Audp2	M18	Tggpio4	T18	Flashctr	W19	V8
C19	Xtalrtci	G19	Audp1	M19	Tggpio5	T19	Rgb0		
D1	Utmi22	H1	Md5	N1	Ldqs	U1	Ma12		

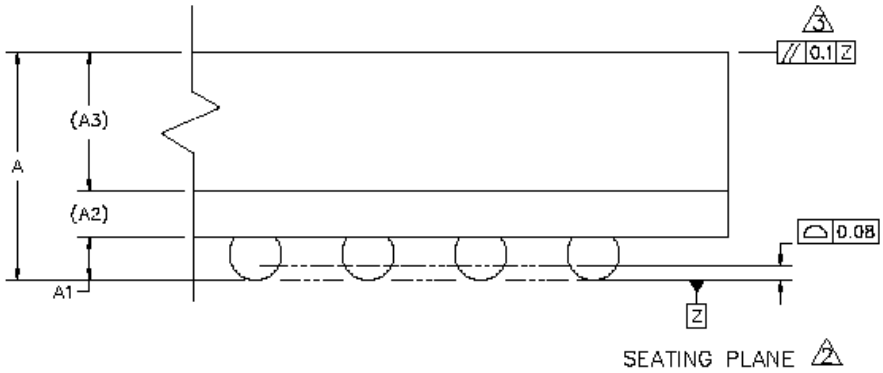
6.1.2. TFBGA-288 package diagram and dimensions (16x16)



6.1.3. TFBGA-288 package diagram and dimensions (12x12)







DETAIL K
SCALE 30/1
(ROTATE 90°)

DIM	MIN.	NOR.	MAX.
A	---		1.0
A1	0.18		0.28
A2		0.21 REF	
A3		0.54 REF	
b	0.27		0.37
D		12 BSC	
E		12 BSC	
e		0.5 BSC	
D1		9 BSC	
E1		9 BSC	

NOTES

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
2. DATUM Z IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

UNIT	DIMENSION AND TOLERANCES	REFERENCE DOCUMENT
MM	ASME Y14.5M	---

6.2. Ordering Information

Product Number	Package Type
SPCA536A-PB111	SPCA536A 288 BGA 16x16 mm
TBD	SPCA536A 288 BGA 12x12 mm

7.DISCLAIMER

The information appearing in this publication is believed to be accurate.

Integrated circuits sold by Sunplus Technology are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only. SUNPLUS makes no warranty, expressed, statutory implied or by description regarding the information in this publication or regarding the freedom of the described chip(s) from patent infringement. FURTHERMORE, SUNPLUS MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. SUNPLUS reserves the right to halt production or alter the specifications and prices at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders. Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by SUNPLUS for such applications. Please note that application circuits illustrated in this document are for reference purposes only.

8.REVISION HISTORY

Date	Revision #	Description	Page
JUN. 11, 2003	0.1	Original	24
OCT. 16, 2003	0.2	Add Electrical Specification	18-36
DEC. 16, 2003	0.3	Modify Pin List	13
FEB. 17, 2004	0.4	Add TFBGA-288 package diagram and dimensions (12x12)	44-45
MAR. 23, 2004	1.0	Add AC/DC information	5-42