DATA SHEET

SUNPLUS

SPCP16A

Low-Speed USB Peripheral Controller

MAR. 06, 2003

Version 1.1

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LOW-SPEED USB PERIPHERAL CONTROLLER

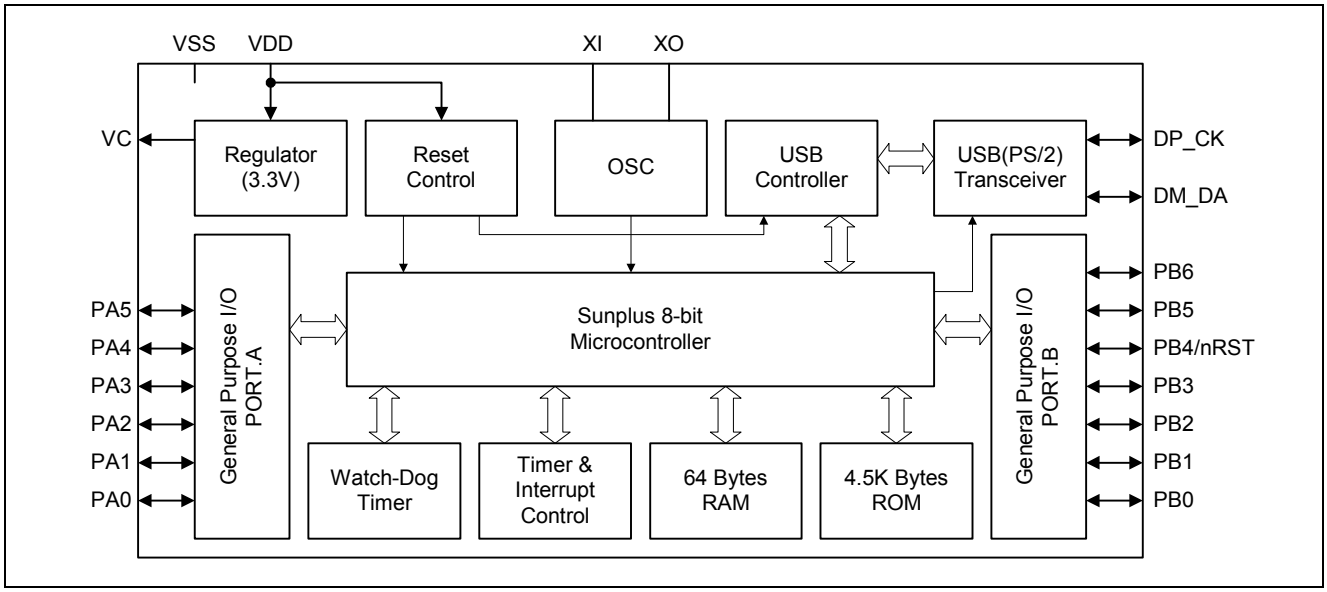
1. GENERAL DESCRIPTION

SPCP16A, a low-speed USB peripheral controller, supports a low-speed USB interface or satisfies the PS/2 interface by firmware detection. The embedded voltage regulator provides regulated 3.3V as the reference voltage for USB signals. Two USB endpoints support control and interrupt transferring. In addition, it is confirmed to USB 1.5Mbps specification ver1.1 as well as USB HID specification ver1.0. The main controller of SPCP16A is an 8-bit Sunplus micro-controller with 64 bytes of RAM and 4.5K bytes of ROM loaded. Up to 13 general-purpose I/Os can be configured for majority of USB mouse applications.

2. FEATURES

- A low-cost solution to both low-speed USB and PS/2 mouse
- Conformed to USB 1.5 Mbps specification, version 1.1
- Conformed to USB HID Specification, version 1.0
- Contains two USB endpoints, where endpoint 0 for Control Transfer, and endpoint 1 for mouse data transfer by Interrupt pipe.
- Built-in 8-bit Sunplus micro-controller.
- Built-in 64 bytes RAM and 4.5K bytes ROM.
- 6 MHz crystal or resonator
- External / Internal power-on reset, illegal address reset, watchdog timer reset, and low voltage reset.
- Power saving modes: STOP and WAIT.
- One 8-bit timer and one watchdog timer.
- Operating voltage: 4.3V - 5.25V for USB; 4.4V - 5.6V for PS/2
- Low cost 20-pin or 18-pin PDIP packages or COB available

3. BLOCK DIAGRAM



4. SIGNAL DESCRIPTIONS

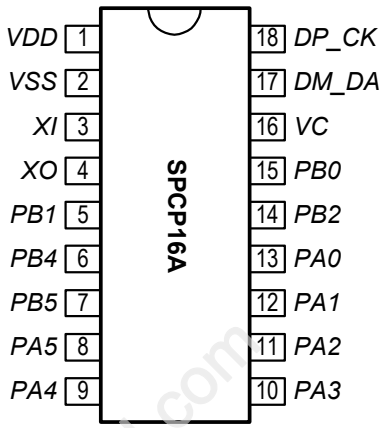
Mnemonic	18 PIN No.	20 PIN No.	Type	Description
VDD	1	1	I	5.0V power
VSS	2	2	I	Power ground
XI	3	3	I	Crystal input or Oscillator input
XO	4	4	O	Crystal output
PB1	5	5	I/O	Port.B Data 1, high drive GPIO (24mA)
nRST/ PB4	6	6	I/O	External Reset or Port.B Data 4, GPIO (4.0mA), see note.1
PB5	7	7	I/O	Port.B Data 5, GPIO (4.0mA) or external IRQ0 input
PA5	8	8	I/O	Port.A Data 5, GPIO (4.0mA)
PA4	9	9	I/O	Port.A Data 4, GPIO (4.0mA)
PA3	10	12	I/O	Port.A Data 3, GPIO (4.0mA)
PA2	11	13	I/O	Port.A Data 2, GPIO (4.0mA)
PA1	12	14	I/O	Port.A Data 1, GPIO (4.0mA)
PA0	13	15	I/O	Port.A Data 0, GPIO (4.0mA)
PB2	14	16	I/O	Port.B Data 2, high drive GPIO (24mA)
PB0	15	17	I/O	Port.B Data 0, GPIO (4.0mA)
VC	16	18	O	3.3V, came from USB transceiver, see note.2
DM_DA	17	19	I/O	USB -Data or PS/2 Data
DP_CK	18	20	I/O	USB +Data or PS/2 Clock
PB3	-	10	I/O	Port.B Data 3, GPIO (4.0mA)
PB6	-	11	I/O	Port.B Data 6, GPIO (4.0mA)

Note1: nRST or PB4 is chosen by mask option; if reset function is selected, it is low active.

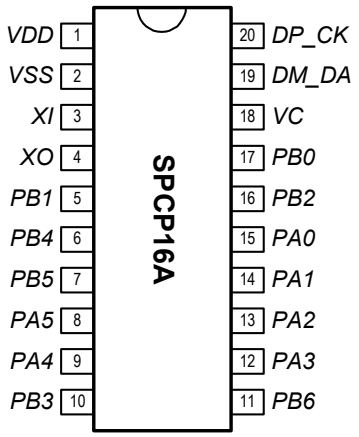
Note2: A large capacitor should be applied on VC pin to avoid the power ripple. VC can also be 3.3V for external pull-up resistor (If internal pull-up is not selected).

4.1. PIN Configuration

4.1.1. 18 PIN configuration

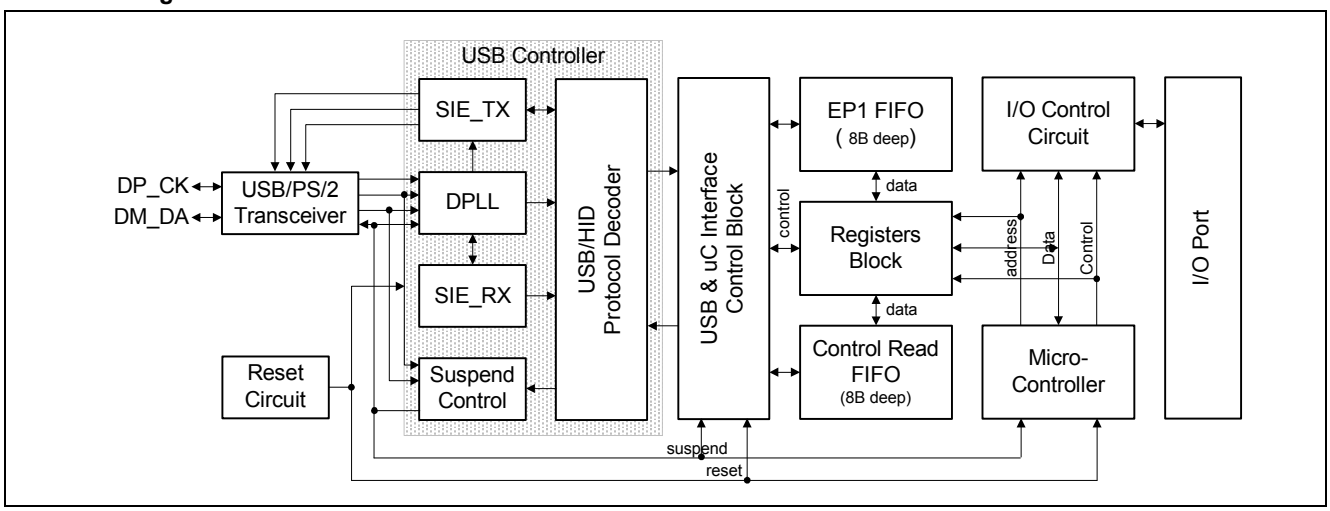


4.1.2. 20 PIN configuration

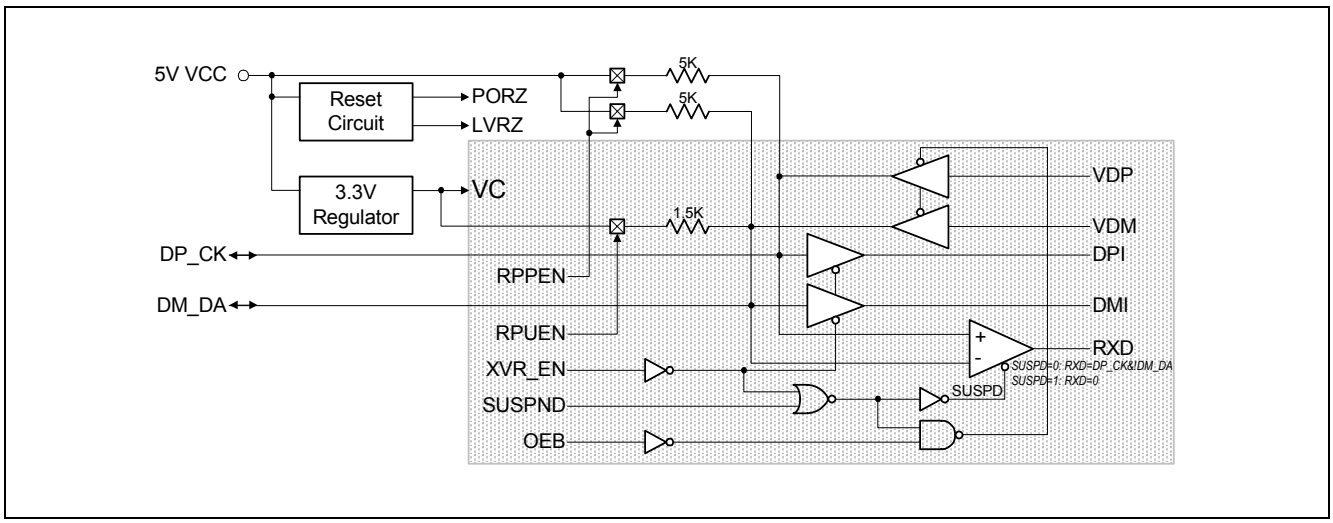


5. FUNCTIONAL DESCRIPTIONS

5.1. Block Diagram



5.1.1. Internal USB transceiver architecture



5.2. Register Sets

r: read accessibility

w: write accessibility

Values in the parentheses ( ) indicate initial condition.

5.2.1. General registers

PA: Port A Data (Addr. 0000h)

b7	b6	b5	b4	b3	b2	b1	b0
-	-	r/w(0)	R/w(0)	r/w(0)	r/w(0)	r/w(0)	r/w(0)
-	-	A[5:0]					

PB: Port B Data (Addr. 0001h)

b7	b6	b5	b4	b3	b2	b1	b0
-	r/w(0)	r/w(0)	R/w(0)	r/w(0)	r/w(0)	r/w(0)	r/w(0)
-	B[6:0]						

DPA: Port A Data Direction (Addr. 0002h)

b7	b6	b5	b4	b3	b2	b1	b0
-	-	w(0)	w(0)	w(0)	w(0)	w(0)	w(0)
-	-	DPA[5:0]					

DPB: Port B Data Direction (Addr. 0003h)

b7	b6	b5	b4	b3	b2	b1	b0
-	w(0)	w(0)	w(0)	w(0)	w(0)	w(0)	w(0)
-	DPB[6:0]						

TCS1: Timer Control and Status 1 (Addr. 0004h)

b7	b6	b5	b4	b3	b2	b1	b0
r(0)	r(0)	r/w(0)	R/w(0)	w(0)	w(0)	r/w(1)	r/w(1)
TOF	RTIF	TOFE	RTIE	TOFR	RTIFR	RT1	RT0

TCR1: Timer Counter Reg. 1 (Addr. 0005h)

b7	b6	b5	b4	b3	b2	b1	b0
r(0)	r(0)	r(0)	r(0)	r(0)	r(0)	r(0)	r(0)
TMR[7:0]							

IRQS: IRQ Control and Status (Addr. 0006h)

b7	b6	b5	b4	b3	b2	b1	b0
w(0)	w(0)	r(0)	r0)	r(0)	r(0)	r/w(0)	r/w(0)
IRQR1	IRQR	-	-	IRQF	IRQF1	IRQE1	IRQE

CPWD: CMP and WDT Status (Addr. 0007h)

b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	-	w(0)
-	-	-	-	-	-	-	WDT

SNW: STOP and WAIT (Addr. 0008h)

b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	w(0)	-	-	-	w(0)
-	-	-	STOP	-	-	-	WAIT

RPA: Port A Pull-up/down (Addr. 0009h)

b7	b6	b5	b4	b3	b2	b1	b0
-	-	w(0)	w(0)	w(0)	w(0)	w(0)	w(0)
-	-	RPA[5:0]					

RPB: Port B Pull-up (Addr. 000Ah)

b7	b6	b5	b4	b3	b2	b1	b0
-	w(0)	w(0)	w(0)	w(0)	w(0)	w(0)	w(0)
-	RPB[6:0]						

5.2.1.1. Port A registers and PINs

The data register, direction control register, and pull up-down control register are built for PortA access and control. The related PortA pins are controlled by these registers. Data register (PA) is a read/write accessible register. The Direction Control Register (DPA) and the Pull up-down Register (RPA) are “write” only registers and they are read back as all 0s. The detail description is shown below:

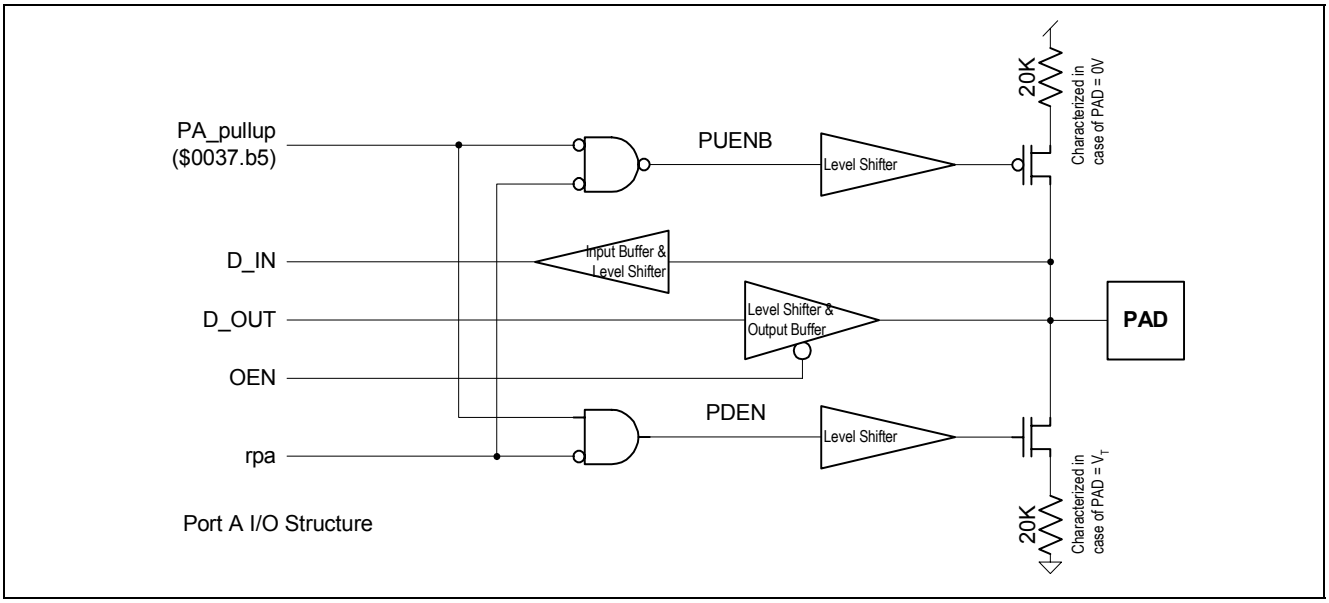
PA	Port A Data Register (0000h)			
Name	**Bit**	**RW**	**Dft**	**Functional Description**
a[5:0]	[5:0]	A	0h	*Port A Data*. When Port A is programmed as output pin, the output data on Port A pins are determined by PA data register. When Port A is programmed as input pin, any "read" command on Port A Data Register will reflect the logic status of those I/O pins. PA data register is set to all 0s when RESET occurs.

DPA	Port A Data Direction Register (0002h)			
Name	**Bit**	**RW**	**Dft**	**Functional Description**
dpa[5:0]	[5:0]	W	0h	*Port A Data Direction*. Port A can be programmed as input or output by DPA register. When dpan = "1", the corresponding pins are programmed as outputs. When dpan = "0", the corresponding pins are programmed as inputs. The DPA is set to all 0s (input) when RESET occurs.

RPA	Port A Pull Up-Down Register (0009h)			
Name	**Bit**	**RW**	**Dft**	**Functional Description**
rpa[5:0]	[5:0]	W	0h	*Port A Pull Up-Down Disable*. When “0” is given, the built-in pull-down resistor of the corresponding pins (PA0~PA5) at input mode will be enabled. When “1” is set, the pull-down resistor will be disabled. The pull-down resistors are disconnected at output mode. The RPA is set to all 0s (enable mode) when RESET occurs.

More information about PortA pins is shown below:

PIN on Port A	Pull Up-Down	R Value	In	Out	Source/Sink	Mask Option for Pull-Down	I/O Cells Name
PA5	Pull down/up @ rpa5	20KΩ	std TTL	std CMOS	4/4 mA	Yes	PAIO4
PA4	Pull down/up @ rpa4	20KΩ	std TTL	std CMOS	4/4 mA	Yes	PAIO4
PA3	Pull down/up @ rpa3	20KΩ	std TTL	std CMOS	4/4 mA	Yes	PAIO4
PA2	Pull down/up @ rpa2	20KΩ	std TTL	std CMOS	4/4 mA	Yes	PAIO4
PA1	Pull down/up @ rpa1	20KΩ	std TTL	std CMOS	4/4 mA	Yes	PAIO4
PA0	Pull down/up @ rpa0	20KΩ	std TTL	std CMOS	4/4 mA	Yes	PAIO4



Port A I/O Structure

5.2.1.2. Port B registers and PINs

The data register, direction control register, and pull up-down control register are built for PortB access and control. These registers control PortB pins. Data register (PB) is a read/write accessible register. The Direction Control Register (DPB) and the pull up/down register (RPB) are “write” only registers and they are read back as all 0s. The detail description is shown below:

PB	Port B Data Register (0001h)			
Name	**Bit**	**RW**	**Dft**	**Functional Description**
b[6:0]	[6:0]	A	0h	*Port B Data.* When Port B is programmed as output pin, the output data on Port B pins are determined by PB data register. When Port B is programmed as input pin, any "read" command on Port B Data Register will reflect the logic status of those I/O pins. PB data register is set to all 0s when RESET occurs.

DPB	Port B Data Direction Register (0003h)			
Name	**Bit**	**RW**	**Dft**	**Functional Description**
dpb[6:0]	[6:0]	W	0h	*Port B Data Direction*. Port B can be programmed as input or output by DPB register. When DPBn = "1", the corresponding pins are programmed as outputs. When DPBn = "0", the corresponding pins are programmed as inputs. The DPB is set to all 0s (input) when RESET occurs.

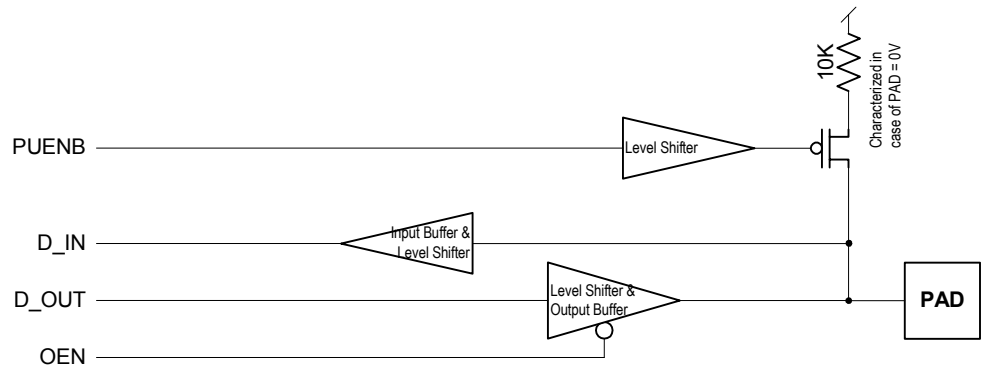
RPB	Port B Pull Up-Down Register (000Ah)			
Name	**Bit**	**RW**	**Name**	**Bit**
rpb[6:0]	[6:0]	W	0h	*Port B Pull Up-Down Disable*. When "0" is given, the built-in pull-up resistor of the corresponding pins (PB0~PB6) at input mode will be enabled. When "1" is given, the pull up/down resistor will be disabled. The pull-up resistors are disconnected at output mode, except for PB1, PB2, and PB5. In PB1, PB2, and PB5, the pull-up resistor is also enabled when the respective PB bit = 1. The RPB register is set to all 0s (enable mode) when RESET occurs.

The more information of the port B pins is shown below:

Pin on Port B	Pull Up-Down	R Value	In	Out	Source /Sink	Mask Option for pull-up	I/O cells Name
PB6	Pull Up @rpb6	10KΩ	IS	std CMOS	4/4 mA	Yes	PBIO4
PB5	Pull Up @rpb5	10KΩ	IS	OD	-/4 mA	No	PBIO4
PB4	Pull Up @rpb4	10KΩ	IS	std CMOS	4/4 mA	No	PBIO4
PB3	Pull Up @rpb3	10KΩ	IS	std CMOS	4/4 mA	Yes	PBIO4
PB2	Pull Up @rpb2	10KΩ	IS	OD	-/24 mA	No	PBIO24
PB1	Pull Up @rpb1	10KΩ	IS	OD	-/24 mA	No	PBIO24

Note1: IS: Schmitt trigger TTL input

Note2: OD: Open Drain output



Port B I/O Structure

5.2.1.3. Reset function

1). External Reset (nRST/PB4 pin)

The RESET/PB4 pin can be optioned to reset function or PB4 I/O through mask option. When RESET function is selected, this pin is the only reset source from external. It is connected to an Schmitt trigger input gate with low active trigger. It can be programmed to an internal pull-up resister.

2). Power-on Reset

This reset is generated internally. The power-on reset will generate a reset signal to reset CPU until oscillator is stabilized. The oscillator will become active after 4096 clock cycles.

3). Watchdog Reset ($0007 bit0 WDT, 1 = clear)

The watchdog timer can be disabled or enabled through mask option. When enabled, an internal watchdog reset is generated by a watchdog-timer time out. This time out generates a reset if WDT register is not cleared within a specific period. An internal reset will be generated and the reset vector will be fetched. To prevent a WDT time-out reset, write a “1” to WDT ($0007 b0) within a certain time period. The minimum WDT reset time is listed in (RT1, RT0) & WDT interrupt frequency table.

4). Illegal Address Reset (IAR)

The internal reset of IAR is generated when an instruction opcode fetches an address which is not implemented in the RAM ($00C0-$00FF) nor ROM ($0400-$0FFF). The IAR will reset the CPU and other peripherals.

5). Low Voltage Reset (LVR)

The internal LVR reset is generated when VDD falls under the specified LVR trigger voltage (2.2V) for at least one cycle.

Note: Only " External reset " and " Power on reset " are able to reset USB controller. Other than these two resets, there is also a soft_reset which will reset the USB state to the "Powered" state. Other resets will not influence the current USB state.

The following table shows all possible resets in:

Items	Reset CPU?	USB controller state
External Reset	Yes	Reset to " Powered " state
Power-on Reset	Yes	Reset to " Powered " state
Watch Dog timer Reset	Yes	Not Change
Illegal Address Reset	Yes	Not Change
Low Voltage Reset	Yes	Not Change
USB Reset from USB port	No	Reset to " Default " state
Soft Reset from ext_reg1	No	Reset to " Powered " state

5.2.1.5. Interrupt

1). Software Interrupt (BRK)

The BRK is an executable instruction interrupt since it is executed regardless of the state of the i-bit in the processor status register flag (inside CPU). When BRK occurs, program jumps to IRQ_routine. With any instruction, interrupts pending during the previous instruction will be served.

2). External Interrupt: (PB0, PB3, PB4, PB5, PB6 and PA[3:0])

IRQS: IRQ Control and Status (Addr. 0006h)

b7	b6	b5	b4	b3	b2	b1	b0
w(0)	w(0)	r(0)	r0)	r(0)	r(0)	r/w(0)	r/w(0)
IRQR1	IRQR	-	-	IRQF	IRQF1	IRQE1	IRQE

The PB0, PB3, PB4, PB5 and PB6 pins can be selected as IRQ or normal I/O function and they are enabled by the corresponding mask options. Each of these pins is connected to an Schmitt trigger input buffer with a 10K pull-up resistor connected on it. PA0 - PA3 can also be selected as external interrupt sources. Similar to PB pin, the interrupt function is enabled by only one mask option

Note: When PB4 is selected to an “External Reset Input” (mask option), it will override its interrupt setting; as a result, it can not be used as an interrupt input.

Both PB pins and PA0-PA3 pins are also software controlled by the IRQE ($0006 bit.0). Whenever an interrupt is generated, the interrupt flag IRQF will be set to “1”. However, it doesn’t mean CPU is serving the interrupt. CPU serves the interrupt only when IRQE = 1 and mask option is enabled. The IRQR ($0006 bit6) is the acknowledge status for IRQ pin interrupt. Writing a "1" to IRQR will clear the interrupt flag IRQF.

There is also a mask option, which controls the interrupt trigger mode. If it is set to "edge trigger mode", the interrupt will then be triggered by a falling edge on enabled PB pin or by a rising edge on any of PA0-PA3. Else if the mask option is set to "level trigger mode", the interrupt is low level triggered by enabled PB pin or high level triggered by any of PA0-PA3.

3). USB Resume Interrupt

When USB bus enters suspend mode, CPU may be programmed to enter STOP mode for power savings purpose. At this time, the only way to wake CPU up is through interrupt. The interrupt can be triggered by a signal event on the pins such as PB0, PB3, PB4, PB5, PB6 or PA0-PA3 (must be pre-enabled). After CPU wakes up, the firmware should upload data to the data FIFO to wake USB subsystem up; this procedure is called "Remote Wakeup". The USB subsystem will next generate a "Resume" signal to indicate USB subsystem has been awakened.

Note: Cares must be exercised while using PA[3:0] and PB pins to trigger interrupt. Before entering STOP mode, all mask options of enabled IRQ sources must stay at "inactive state", i.e. PB pins must stay at high and PA pins must remain at low; otherwise, the interrupt will not be triggered. For example, suppose PB pins are mask option selected as IRQ pins and PB4 has been driving low. It causes any negative edge trigger on other PB pins will not trigger IRQ after entering STOP mode. That is, program will be stranded in STOP mode.

When the USB suspend state is resumed by the USB host, CPU may still stay in wait mode or stop mode. In this condition, the “resume” signal can be used to generate an interrupt to notify firmware that USB has resumed and to exit from wait mode or stop mode. This procedure is called "Host Resume". The USB resume interrupt is enabled by IRQE1 ($0006 bit.1), and it is triggered at the falling edge (functional compatible with PA7 interrupt of SPMC01). When IRQF1 is set ($0006 bit.2 = 1), the IRQR1 ($0006 bit.7) is used as USB resume interrupt acknowledge. Writing a "1" to IRQR1 will clear the interrupt flag IRQF1.

4). Timer Interrupt (TIMER)

The timer interrupt is generated by the multi-function timer when either a timer overflows or a real time interrupt occurs. The Timer Control & Status Register (TCS, located at $0004) specifies the timer interrupt flags (TOF, RTIF), enable bits (TOFE and RTIE), and the timer interrupt acknowledge bits (TOFR and RTIFR). The i-bit in the processor status flag (inside of CPU) must be cleared to 0 to enable the interrupt.

5.2.1.6. Multi-function timer

The timer for this device is a 15-bit multi-function ripple up-counter. Functions include Timer Overflow, Real Time Interrupt (RTI), Power on Reset, and Watchdog Timer reset (WDT). When Timer Counter Register (TCR $0005) overflows, the Timer Overflow Flag (TOF) will be set. Moreover, TOF = 1 will result in an interrupt request to CPU if Timer Overflow Enable is set (TOFE = 1). When TOFR = 1, the TOF flag bit will be cleared. The Real Time Interrupt Flag (RTIF) will be set when 1 of 4 selections (RT1, RT0) is activated. If Real Time Interrupt Enable is set (RTIE = 1) and when RTIF = 1, an interrupt request will be generated for CPU. Writing a “1” to RTIFR will clear the RTIF flag bit.

5.2.1.7. Timer registers

The 15-stage timers contain two registers: Timer Counter and Timer Control/Status Register:

1). Timer Counter Register (TCR) - $0005

The timer counter register is a read-only register, which contains the present value of the 8-bit timer chain.

2). Timer Control/Status Register (TCS)- $0004

The TCS contains the timer interrupt flag (TOF, RTIF), the timers interrupt enable (TOFE, RTIE), timers interrupt acknowledge (TOFR, RTIFR), and the real timers interrupt rate selection bits (RT1, RT0). Bit 2 and bit 3 are write-only bits and always be read back as zeros.

TCS1: Timer Control and Status 1 (Addr. 0004h)

b7	b6	b5	b4	b3	b2	b1	b0
r(0)	r(0)	r/w(0)	r/w(0)	w(0)	w(0)	r/w(1)	r/w(1)
TOF	RTIF	TOFE	RTIE	TOFR	RTIFR	RT1	RT0

TOF - Timer Overflow Flag (read-only flag bit.)

Set to “1” when 8-bit ripple counter rolls over from $FF to $00. A timer interrupt request will also be generated if TOFE is set. Writing a “1” to TOFR (TOF acknowledges bit) will clear TOF to “0”.

RTIF - Real Time Interrupt Flag (read-only flag bit.)

Set to “1” when output of the chosen Real Time Interrupt stage goes active. A timer interrupt request will also be generated if RTIE is also set. Writing a “1” to RTIFR (RTIF acknowledges bit) will clear RTIF to “0”.

TOFE - Timer Overflow Enable

Enables generating timer interrupt when Timer Counter Register overflows.

1: the timer interrupt is generated when TOF flag bit is set.

0: no timer interrupt caused by TOF bit will be generated.

RTIE - Real Time Interrupt Enable

Enables generating timer interrupt by RTIF bit.

1: the timer interrupt is generated when RTIF flag bit is set.

0: no timer interrupt caused by RTIF bit will be generated.

TOFR - Timer Overflow Acknowledge

Acknowledge bit to reset TOF flag. Reading TOFR will always return a zero.

1: Clears TOF flag bit.

0: Does not clear TOF flag bit.

RTIFR - Real Time Interrupt acknowledge

Acknowledge bit to reset RTIF flag bit. Reading RTIFR will always return a zero.

1: Clears RTIF flag bit.

0: Not clear RTIF flag bit.

RT1:RT0 - Real Time Interrupt Rate Select

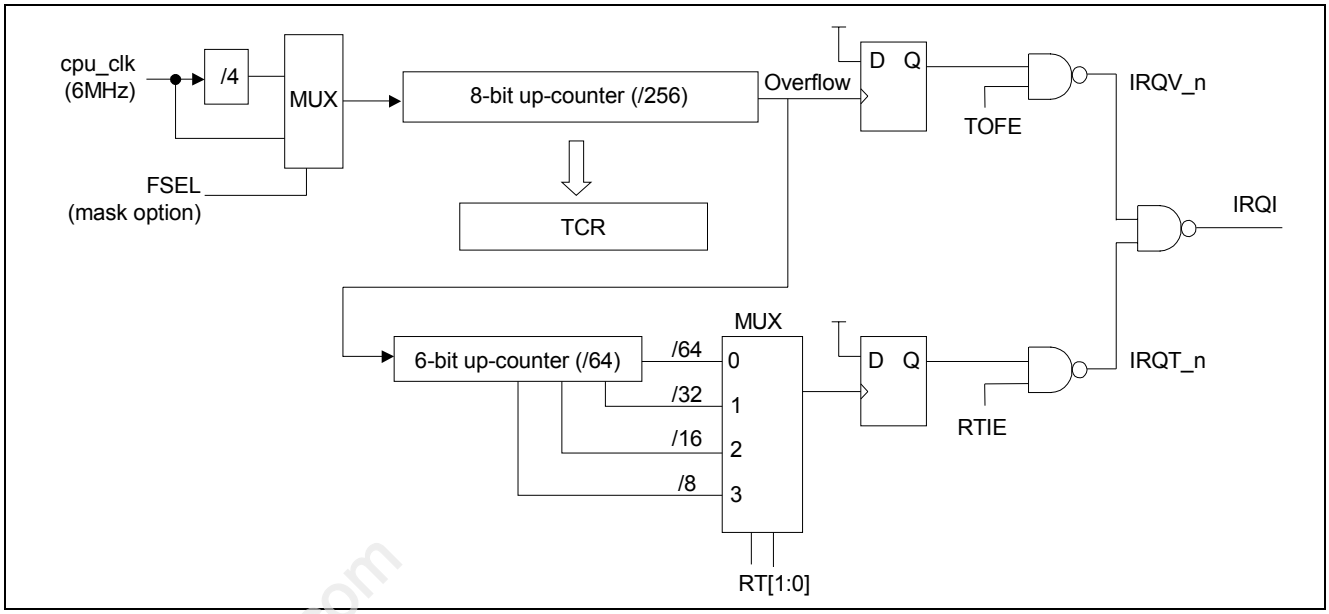
The RT0 & RT1 control bits select one of four taps for the Real Time Interrupt circuit. The following table shows the available interrupt rates for two frequencies.

The Overflow timer = base_clk / 256. When mask option FSELX = 1, base_clk = 6 MHZ CLK/4; so, the TOF period = 171 us.

The (RT1, RT0) versus RTI & WDT Interrupt Frequency Table (Assume mask option FSELX = 1, i.e. select base_clk = 6MHz clk/4)

RT1, RT0	RTI rates		WDT timeout period	
	Divider		Divider	
00	8192	1.37 ms	65536	10.92 ms
01	16384	2.73 ms	131072	21.85 ms
10	32768	5.46 ms	262144	43.69 ms
11	65536	10.92 ms	524288	87.38 ms

Note: The watchdog timer rate is always = the RTI rate / 8



5.2.1.8. Wait and STOP mode

The WAIT mode function will stop the CPU clock and keep the timer counter counting. As in WAIT mode ($0008 bit0 is set to “1”), the TOF, RTI or external interrupt can be used to wake CPU up and the program can work normally after that. The STOP mode function will stop both CPU clock and Timer counter. As in the STOP mode ($0008 bit4 is set to “1”), only external interrupt is able to wake CPU up and the timer works normally after that.

5.2.2. USB/PS2 mode control registers

DPG: Port G Data Direction, power on reset = 0, (write only) port address = 001Ah

b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	-	-	-	dpg

PG: Port G Data, power on reset = 00h (read/write) port address = 001Bh

b7	b6	b5	b4	b3	b2	b1	b0
PG[7:0]							

DPG defines the internal PortG direction (similar to DPA or DPB) and PG is the PortG data register. SPCP16A uses PortG to transfer data between USB controller and micro-controller. When dpg = 0, PG is written protected. When dpg = 1, PG is a read/write register. The firmware reports the EP0 or EP1 data simply by writing data to PG byte by byte, depends on the ep0_rdy or ep1_rdy status of the PH register ($001E). When ep1_rdy = 1, the firmware could report EP1 data to PG; When ep0_rdy = 1 and a valid USB Control read command has been detected on PH[3:0], the firmware should report the Control Read data to PG.

PH: Port H Data, power on reset = 00h, (read only) port address = 001Eh

b7	b6	b5	b4	b3	b2	b1	b0
suspend	resume	ep0_rdy	ep1_rdy	cmd.3	cmd.2	cmd.1	cmd.0

PH is also an internal micro-controller (μC) data port, used here as a read only register (input mode only for μC) which returns USB controller status. The μC polls this register to determine the operation in responding to various USB commands

suspend: = 1 means USB bus is in suspend state; 0 otherwise

resume: = 1 indicates the suspend state is exited by remote wake up, and the USB controller is sending K state cycle to wake USB system up. Note this bit is not active if USB is resumed by HOST.

cmd[3:0]: encoded USB control transfer command, see below table for details

ep0_rdy: = 1 means the Control Read FIFO is ready to accept data from μC. When μC detects a valid USB control read command on cmd[3:0], μC should check this bit before writing data to PG.

ep1_rdy: = 1 means the Endpoint.1 FIFO is ready to accept data from μC. Note the Endpoint.1 FIFO is used to store the data of Mouse event from PA or PB. This is also done by directly writing to PG. Upon the number of bytes stored in the FIFO reaches the ep1_pkt_size[3:0] value of ext_reg2, ep1_rdy will be cleared to "0" and will become "1" (ready) again when USB host has issued an interrupt read to endpoint.1

Command Encoding:

cmd(3:0)	Commands	μC operation
0000	non-Control cycle	polling mouse event
0001	Get_Descriptor (Device)	μC returns the specific data from ROM
0010	Get_Descriptor (Configuration)	μC returns the specific data from ROM
0011	Get_Descriptor (HID)	μC returns the specific data from ROM
0100	Get_Descriptor (String0)	μC returns the specific data from ROM
0101	Get_Descriptor (String1)	μC returns the specific data from ROM
0110	Get_Descriptor (String2)	μC returns the specific data from ROM
0111	Get_Descriptor (String3)	μC returns the specific data from ROM
1000	Get_Descriptor (Report)	μC returns the specific data from ROM
1001	Get_Report (Input)	μC returns the report (IN) data from RAM
1010	not support	-
1011	not support	-
1100	not support	-
1101	not support	-
1110	not support	-
1111	not support	-

Note1: Set_Descriptor, Set_Report(Input), Set_Report(Feature) and Get_Report (Feature) are not supported.

Note2: The HID descriptor can be either returned by Get_Descriptor (Configuration) or by Get_Descriptor (HID).

Note3: The μC can update the mouse scan data only cmd (3:0) = 0000 and ep1_rdy = 1

Note4: Set_Idle, Get_Idle, Set_Protocol and Get_Protocol are done by USB controller and are not passed to μC.

ext_reg1: Extended register No.1, power on reset = 00h, (read /write) port address = 0020h

b7	b6	B5	b4	b3	b2	b1	b0
r/w(0)	r(0)	-	-	-	r/w (0)	-	r/w(0)
soft_reset	rwakeup_en	-	-	-	config_done	-	xfr_done

soft_reset : This is a software reset bit used to reset the USB controller. Setting this bit to 1 will force the USB subsystem into "Powered" state. When it is set to 1, it should be set to 0 by the firmware for the normal operation. This bit is "written protected" by ext_reg5, and it is "written enabled" only when ext_reg5 = 74h.

rwakeup_en : This is a read-only bit to show present remote wakeup feature status. Reads a "1" meaning USB has finished a successful Set_Feature (device) to the device. Reads a "0" meaning the remote wakeup feature is not enabled by host or is cleared by Clear_Feature (device).

config_done : This is a GPIO bit. It can be used by firmware to record the USB configuration status; it is the only register bit to be reset by both power-on reset and USB reset. After writing it to 1, the firmware should reconfirm (read back) it to prevent from being an invalid write within USB reset cycle.

xfr_done : When μC has completed all data transfer of current Control Read or Write , it must write a "1" to this bit to inform the USB controller that current transaction is completed; so that the state machine of the USB controller is able to enter handshaking stage to check handshaking with USB host. This bit is automatically cleared to "0" when the handshaking cycle is done.

ext_reg2: Extended register No.2, power on reset = 43h, port address = 0021h

b7	b6	B5	b4	b3	b2	b1	b0
r(0)	r(1)	r(0)	r(0)	r/w(0)	r/w(0)	r/w(1)	r/w(1)
vendor	protocol	sof	usb_reset	ep1_pkt_size(3:0)			

vendor : vendor specific bit. When this bit = 1, and the cmd[3:0] in the PH register = 1001; it means the current control cycle = Get_Report(Vendor). This is a diagnostic command for reporting the RAM contents and its USB setup packet formats are:

bmRequestType	=	C0h
bmRequest	=	01h
wValueL	=	RAM address
wValueH	=	don't care
wIndex	=	don't care
wLength	=	0001h - 0008h (must be less than ep1_pkt_size of ext_reg2)

Note: when the USB host requests the command, the wValueL (report RAM address) will be put at ext_reg8 ($0027). Firmware may read the register to know the address of the RAM for reporting the request.

protocol : This is a read only bit which indicates the current HID protocol in response to Set_Protocol command by USB host. 0 means booting protocol and 1 means reporting protocol; the power on value = 1 (report protocol).

sof : A read only bit. It is active high when a SOF packet is shown on USB bus

usb_reset : This is a read only bit; active high when a USB_reset cycle is shown on USB bus.

ep1_pkt_size: 4-bit value defines EP1 packet size in numbers of byte. Note the maximum allowable programmed value = 8 (the packet size for Endpoint.0 is always 8, except the packet size of Get_report(input) is ep1_pkt_size).

ext_reg3: Extended register No.3, power on reset = 00h, port address = 0022h

b7	b6	b5	b4	b3	b2	b1	b0
r/w(0)	r/w(0)	r/w(0)	r/w(0)	r/w(0)	r/w(0)	r(0)	r(0)
usb_ps2n	xver_en	rpuen	rppen	ps2_txclk	ps2_txd	ps2_rxclk	ps2_rxd

usb_ps2n : USB or PS/2 mode selection bit; 0 = PS/2 mode(default), 1 = USB mode
xver_en : Internal USB transceiver enable control signal, active HIGH; see page 3 for details
rpuen : controls the connection of the 1.5 K pull-up resistor for USB mode
0: open (default), 1: connected; see page 3 for details
rppen : controls the connection of 5K-Ohm pull-up resistor for PS/2 mode
0: open (default), 1: connected; see page 3 for details
ps2_txclk : write ports of CLK output at PS/2 mode; it must be kept at HIGH at input mode .
ps2_txd : write ports of DATA output at PS/2 mode; it must be kept at HIGH at input mode.
ps2_rxclk : Read port of CLK input at PS/2 mode
ps2_rxd : Read port of DATA input at PS/2 mode

ext_reg4: Extended register No.4, power on reset = 32h, (write only) port address = 0023h

b7	b6	b5	b4	b3	b2	b1	b0
rpt_des_size[7:0]							

This register defines the size of the report descriptor in numbers of byte. The report descriptor size depends on applications and the USB controller will refer this register to report DATA for USB host.

It is suggested to program this register at the firmware initial setting.

ext_reg5: Extended register No.5, power on reset = 00h, (read / write) port address = 0024h

b7	b6	b5	b4	b3	b2	b1	b0
GPIO[7:0]							

This is a general-purpose register, which is reset by power-on reset, not USB reset

ext_reg8: Extended register No.8, power on reset = 00h, (read only) port address = 0027h

b7	b6	b5	b4	b3	b2	b1	b0
rpt_ram_addr / report_ID							

This register returns the report RAM address when the command Get_Report(Vendor) has issued and if ext_reg2[7] = 1 & cmd[3:0] = 1001 ;

This register returns the report ID when the command Get_Report(input) has issued and if ext_reg2[7] = 0 & cmd[3:0] = 1001 ; The wValueL of both requests is stored in this register

ext_reg9: Extended register No.9, power on reset = FEh, (read/write) port address = 0028h

B7	B6	B5	B4	B3	B2	B1	B0
str1_des_size[7:0]							

This register defines the size of the string descriptor 1 in numbers of byte; the maximum allowable value = FEh (default value); the register should be programmed to “the exact size of the descriptor data”.

ext_reg10: Extended register No.10, power on reset = FEh, (read/write) port address = 0029h

B7	B6	B5	B4	B3	B2	B1	B0
str2_des_size[7:0]							

This register defines the size of the string descriptor 2 in numbers of byte; the maximum allowable value = FEh (default value); the register should be programmed to “the exact size of the descriptor data “.

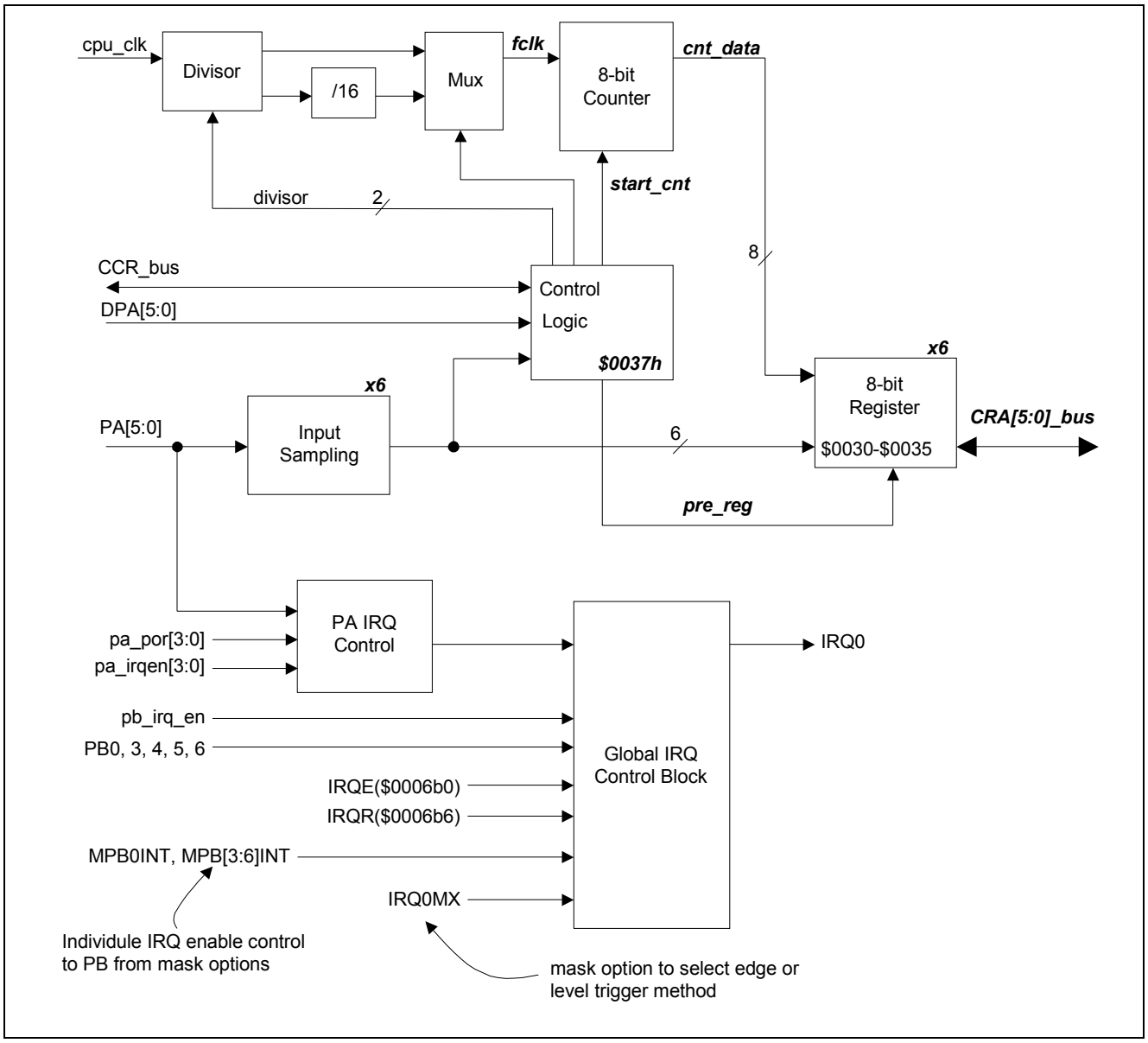
ext_reg11: Extended register No.11, power-on reset = FEh, (read/write) port address = 002Ah

B7	B6	B5	B4	B3	B2	B1	B0
str3_des_size[7:0]							

This register defines the size of the string descriptor 3 in numbers of byte; the maximum allowable value = FEh (default value); the register should be programmed to “the exact size of the descriptor data”.

5.2.3. Input capture registers ($0030h - $0035h, $0037h)

There are one 8-bit counter, six 8-bit registers, one control register, and the control logic to perform the PA[5:0] input Capture feature. The counter is cleared to "0h" and each of the Capture Registers (CCR0 - 5) is set to “FFh” when the start bit of the Capture Control Register (CCR) is "0". Below shows the block diagram:



The start bit is designed to enable the operation. When the start bit is enabled and at least one of the DPA[5:0] is set to input mode, the counter starts counting up. When the counter reaches the value “FFh”, it will keep the value until the start bit is cleared. Once the related PA port input is sampled from low to high, the count value will be stored into the related register. The data will be kept until the start bit is cleared.

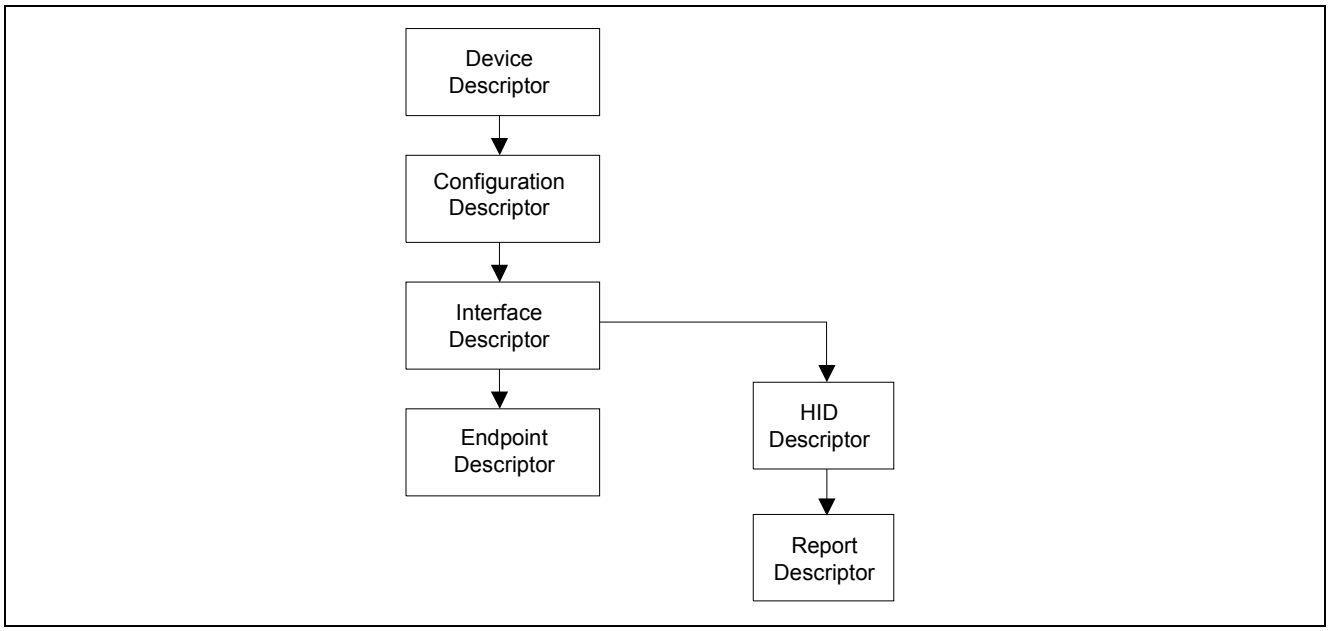
The clock for 8-bit capture counter (fclk) is controlled by base_clk_sel ($0037 b3) and div[1:0] ($0037 b[1:0]). When base_clk_sel = 0, the maximum capture duration for 6MHz CPU clk = 167ns * 4 * 256 = 171us; when base_clk_sel = 1, the maximum capture duration for 6MHz CPU clk = 167ns * 4 * 16 * 256 = 2.7ms. In control logic, one start bit is implemented for the operating control. In addition, six 8-bit latches are used to latch the counting value for related PA inputs.

CRA[5:0]	Capture Register for PA[5:0]			$0030-$0035
Name	**Bit**	**RW**	**Dft**	**Functional Description**
cran[7:0]	[7:0]	R	FFh	*Capture Register for PA[5:0]*. The capture count value latched by PA[5:0] transition edge. For CR0 - 3 (latched by PA0 - 3), the transition edge (rising or falling) follows the interrupt polarity as defined in the Capture IRQ Register ($0036h). For CR4 and CR5 (latched by PA4, PA5), capture count is always latched by rising edge. Each capture register is set to "FFh" by power-on reset or when the start bit of CCR is cleared.

CIR[7:0]	Capture IRQ Register			$0036
Name	**Bit**	**RW**	**Dft**	**Functional Description**
pa_por[3:0]	[7:4]	A	00h	Interrupt polarity for PA[3:0], 0: rising (default) ; 1: falling
pa_irqen[3:0]	[3:0]	A	00h	Individual Interrupt enable control for PA[3:0]; 0: disable (default), 1: enable Note the interrupt of PA[3:0] is also enabled by IRQE ($0006 b0)

CCR	Capture Control Register			$0037
Name	**Bit**	**RW**	**Dft**	**Functional Description**
resv.	[7:6]	-		*Reserved.*
PA_pullup	5	A	0h	This bit selects either pull-down or pull-up for PA ports; 0 (default): pull up/down, 1: pull-up. When PA is set to falling edge trigger, it is recommended to set this bit to high to ensure proper IRQ operation. When PA is set to rising edge trigger, it is better to set this bit to low for proper IRQ operation.
PB_irq_en	4	A	1h	This is the software control bit for PB IRQ. Since PB shares the same IRQ with PA[3:0], this allows programmer to temporarily set this bit to "0" (disable) for only PA IRQ effect needs . Note this bit is normally written protected; so that, the firmware can be backward compatible with SPCP13A. The firmware must first write "82h" to ext_reg5($0024h) to unlock it. The other bits of this register are not written protected.
base_clk_sel	3	A	0h	Select base_clk duration for the capture counter: 0: base_clk = CPU clk (6 MHZ); 1: base_clk = CPU clk / 16
start	2	A	0	*Count Function Start*. This bit will combine with the DPA [5:0] to enable the count. Once this bit is set to "0", the counter will be reset to "0" and the capture registers CRA[5:0] are set to "FFh". When it is set to "1", the counter will start counting up if at least one of the dpa[5:0] is set to input mode.
div[1:0]	[1:0]	A	0h	*Divisor for Capture Counter*. 00: Stop the clock; 01: base_clk/2; 10:base_clk/3; 11: base_clk/4.

5.3. USB Descriptors



Note1: With response to the Get_Descriptor (Configuration) request , the order of returned descriptors are:
Configuration descriptor
Interface descriptor (specifying HID class)
HID descriptor (associated with above Interface)
Endpoint descriptor (for HID Interrupt ENdpoint)

Note2: String Descriptor is not returned by above request, but by Get_Descriptor(String)

Note3: HID Report Descriptor is read by the request: Get_Descriptor(Report), which is not a standard USB device request, but MUST be supported for HID device.

Below is an example of USB descriptors for a 3-key USB mouse.

5.3.1. Device descriptor: (18 bytes)

Offset	Field	Size	Value	Description
0	bLength	1	12h	Size of this descriptor in byte
1	bDescriptor Type	1	01h	Device descriptor type
(3,2)	bcdUSB	2	0100h	USB specification release number in BCD
4	bDeviceClass	1	00h	Class Code (assigned by USB)
5	bDeviceSubClass	1	00h	Subclass code (assigned by USB)
6	bDeviceProtocal	1	00h	Protocol code (assigned by USB)
7	bMaxPacketSize0	1	08h	Maximum packet size for endpoint 0
(9,8)	idVendor	2	04FCh	Sunplus Vendor ID (assigned by USB)
(11,10)	idProduct	2	0001h	Product ID (assigned by manufacturer)
(13,12)	bcdDevice	2	0110h	Device release number in BCD
14	iManufacturer	1	01h	Index of string descriptor describing manufacturer
15	iProduct	1	02h	Index of string descriptor describing product
16	iSerialNumber	1	03h	Index of string descriptor describing the device serial number
17	bNumConfigurations	1	01h	Number of possible configurations

5.3.2. Configuration descriptor: (9 bytes)

Offset	Field	Size	Value	Description
0	bLength	1	09h	Size of this descriptor in byte
1	bDescriptor Type	1	02h	Configuration descriptor type
3,2	wTotalLength	2	0022h	Total length of data returned for this configuration by Get_Descriptor command, the data comprises configuration, interface, endpoint, and HID
4	bNumInterfaces	1	01h	Number of Interface supported by this configuration
5	bConfigurationValue	1	01h	Value to use as an argument to Set_Configuration
6	iConfiguration	1	00h	Index of string descriptor describing this configuration; 00h means none
7	bmAttributes	1	A0h	Bus powered, remote wakeup
8	bMaxPower	1	14h	Maximum power consumption in 2 MA unit

5.3.3. Interface descriptor: (9 bytes)

Offset	Field	Size	Value	Description
0	bLength	1	09h	Size of this descriptor in byte
1	bDescriptor Type	1	04h	Interface descriptor Type
2	bInterfaceNumber	1	00h	Number of interface
3	bAlternateSetting	1	00h	Value used to select alternate setting for the interface identified in the prior field
4	bNumEndpoints	1	01h	Number of endpoints used by the interface (excluding endpoint zero)
5	bInterfaceClass	1	03h	Class code (HID code assigned by USB)
6	bInterfaceSubClass	1	01h	0: no subclass ; 1:Boot Interface subclass
7	bInterfaceProtocol	1	02h	0: none; 1: Keyboard; 2: Mouse
8	iInterface	1	00h	Index of string descriptor describing this configuration, 00h means none

5.3.4. HID descriptor: (9 bytes)

Offset	Field	Size	Value	Description
0	bLength	1	09h	Size of this descriptor in byte
1	bDescriptor Type	1	21h	HID descriptor Type
3,2	bcdHID	2	0100h	HID class specification release number in BCD
4	bCountryCode	1	00h	Hardware target country
5	bNumDescriptors	1	01h	Number of HID class descriptors to follow
6	bDescriptorType	1	22h	Report descriptor type
(8,7)	wDescriptorLength	2	# 0032h	Total length of eport descriptor

Note: # The length depends on Vendor, and must be same as the programmed value of ext_reg4 (addr. 0023h)

5.3.5. Endpoint descriptor: (7 bytes)

Offset	Field	Size	Value	Description
0	bLength	1	07h	Size of this descriptor in byte
1	bDescriptor Type	1	05h	Endpoint descriptor Type
2	bEndpointAddress	1	81h	IN endpoint, endpoint number = 0001
3	bmAttribute	1	03h	B(1:0) = 11 means interrupt endpoint
(5,4)	wMaxPacketSize	2	0008h	Maximum packet size; this endpoint is capable of sending or receiving data
6	bInterval	1	0Ah	Interval for polling endpoint for data transfer. This is expressed in milliseconds, here = 10 ms

5.3.6. Report descriptor: (50 bytes)

(The number of bytes (50 = 32h) has already described in the HID descriptor)

Item	Value (hex)
Usage Page (Generic Desktop),	05 01
Usage (Mouse),	09 02
Collection (Application),	A1 01
Usage (Pointer),	09 01
Collection (Physical),	A1 00
Usage Page(Buttons),	05 09
Usage Minimum (01),	19 01
Usage Maximum (03),	29 03
Logical Minimum (0),	15 00
Logical Maximum (1),	25 01
Report Count (3),	95 03
Report Size (1),	75 01
Input (Data, Variable, Absolute), ;3 button bits	81 02
Report Count (1),	95 01
Report Size (5),	75 05
Input (Constant), ;5 bit padding	81 01
Usage Page (Generic Desktop),	05 01
Usage (X),	09 30
Usage (Y),	09 31
Logical Minimum (-127),	15 81
Logical Maximum(127),	25 7F
Report Size (8),	75 08
Report Count (2),	95 02
Input (Data, Variable, Relative), ; 2 position bytes (X & Y)	81 06
End Collection	C0
End Collection	C0

Note1: Report descriptor size is determined by the value programmed in the ext_reg4 which, which is reset to 32h.

Note2: The report size for the Get_Report (input) command is determined by the value " max_pkt_size" programmed in the ext_reg2, which is reset to 3 for Mouse and 8 for KBE

5.3.7. String descriptor

(string Index.0 as for Get_Descriptor(String))

Offset	Field	Size	Value	Description
0	bLength	1	04h	Size of this descriptor in byte
1	bDescriptor Type	1	03h	String descriptor Type
3,2	bString	2	0009h	Array of LangID code, here is for English

(string Index.1 as for Get_Descriptor(String))

Offset	Field	Size	Value	Description
0	bLength	1	str_size	Size of this descriptor in byte
1	bDescriptor Type	1	03h	String descriptor Type
str_size -1	bString	str_size -2		String description of manufacturer

(string Index.2 as for Get_Descriptor(String))

Offset	Field	Size	Value	Description
0	bLength	1	str_size	Size of this descriptor in byte
1	bDescriptor Type	1	03h	String descriptor Type
str_size -1	bString	str_size -2		String description of Manufacturer

(string Index.3 as for Get_Descriptor(String))

Offset	Field	Size	Value	Description
0	bLength	1	str_size	Size of this descriptor in byte
1	bDescriptor Type	1	03h	String descriptor Type
str_size -1	bString	str_size -2		String description of manufacturer

Note1: All values of bString must use UNICODE(16 bit) string.

Note2: The string size for string 0 is fixed to 4. The string size for string 1 to string 3 is not fixed and the maximum allowable string size is 254.

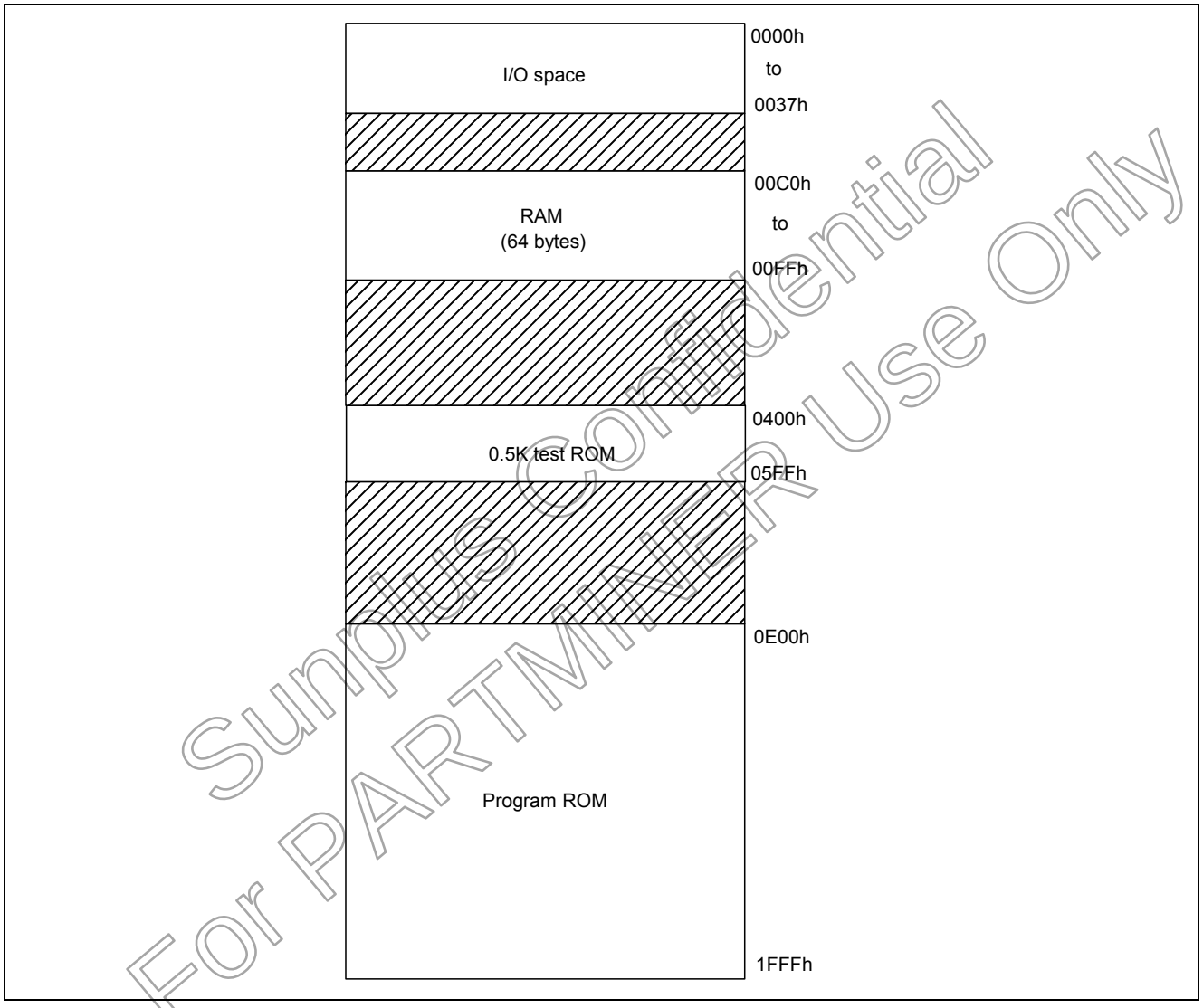
5.5. I/O and Memory Address Space

The I/O address space starts from 0000h to 0037h.

The ROM address space starts from 0E00h to 1FFFh (totally 4608 bytes) for SPCP16A.

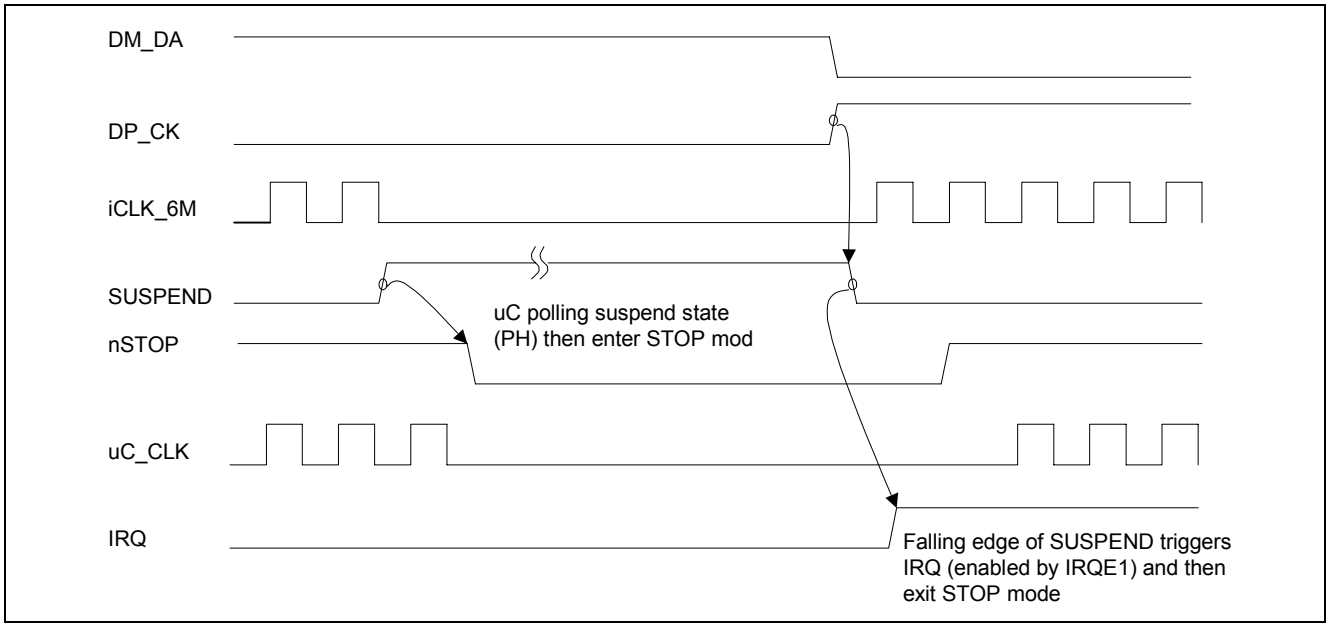
The RAM address space starts from 00C0h to 00FFh (totally 64 bytes).

The other address spaces not specified are not supported and not accessible.

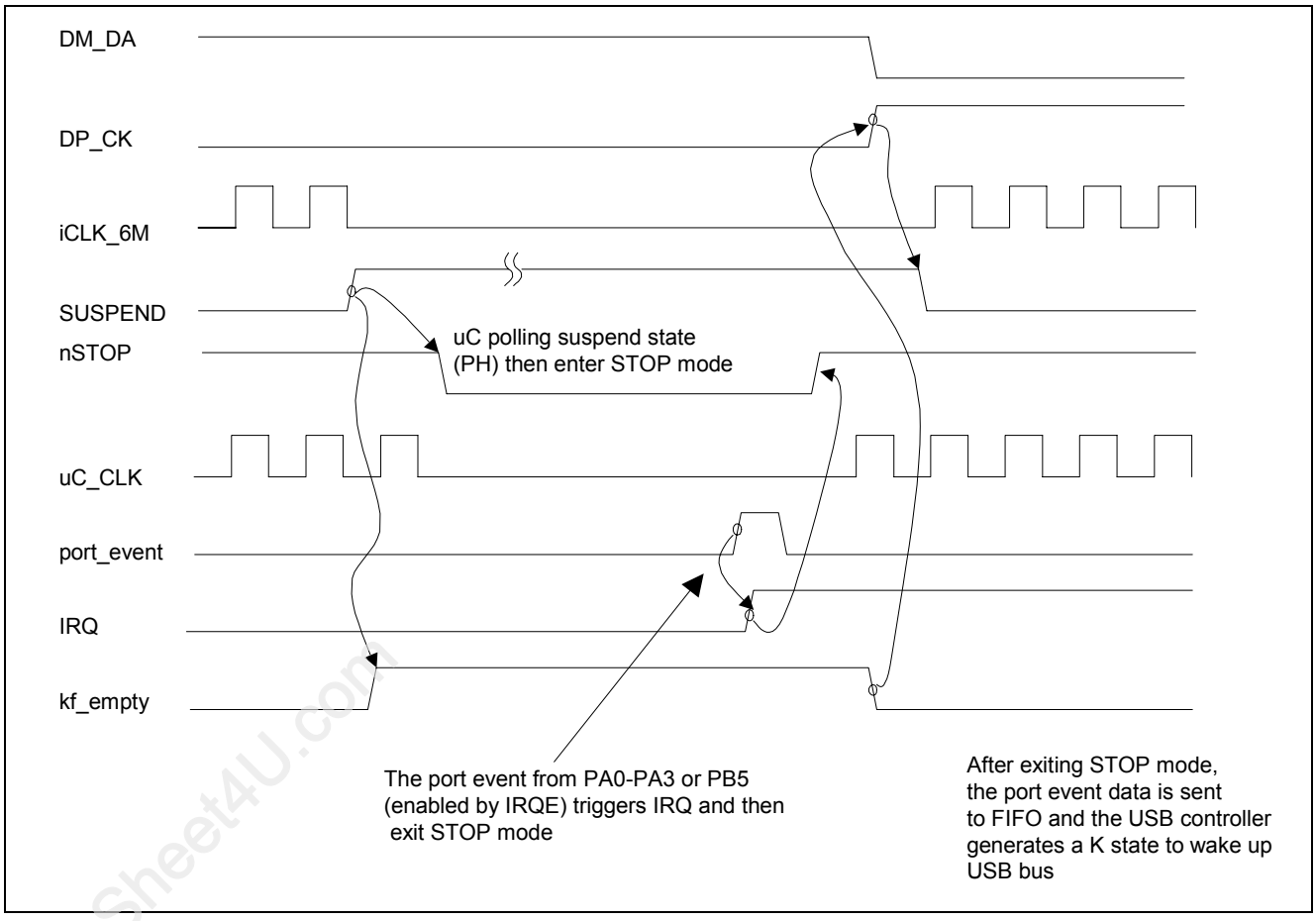


5.6. Timing

5.6.1. Suspend and host resume timing



5.6.2. Suspend and remote wakeup Timing



5.7. Mask Option Summary

PA Pull Up/Down Enable	☐ Enable	☐ Disable	
PB0 Pull Up Enable	☐ Enable	☐ Disable	
PB3 Pull Up Enable	☐ Enable	☐ Disable	
PB6 Pull Up Enable	☐ Enable	☐ Disable	
PA[3:0] Ext. Interrupt Function	☐ Enable	☐ Disable	
PB0 Ext. Interrupt Function	☐ IRQ with I/O	☐ PB0, no IRQ	
PB3 Ext. Interrupt Function	☐ IRQ with I/O	☐ PB3, no IRQ	
PB5 Ext. Interrupt Function	☐ IRQ with I/O	☐ PB5, no IRQ	
PB6 Ext. Interrupt Function	☐ IRQ with I/O	☐ PB6, no IRQ	
PB4 Ext. Input Function	☐ I/O only	☐ I/O with RST	☐ I/O with IRQ
PB0,3,4,5,6 & PA[3:0] Ext. Interrupt Trigger Mode	☐ Edge	☐ Edge-Level	
Watch Dog Timer Option	☐ Yes	☐ No	
Low Voltage Reset Option	☐ Yes	☐ No	
Timer Pre-scale Option	☐ Divided by 4	☐ No Divided	

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Rating

Characteristics	Item	Min.	Typ.	Max.	Unit	Condition
Storage Temperature	T_{STR}	-40	-	125	ºC	
Operating Ambient Temperature	T_{OPR}	0	-	70	ºC	
Voltage Rating on Input	V_{IN}	-0.3	-	VDD +0.3	V	
Voltage Rating on VDD		-0.3	-	7.0	V	
Output Voltage	V_{OUT}	0	-	VDD	V	

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. Recommended Operating Conditions

Characteristics	Item	Min.	Typ.	Max.	Unit	Condition
Operating Supply Voltage	VDD	4.4	-	5.6	V	PS/2 Mode
		4.3	-	5.25	V	USB Mode
Power Consumption	I_{DD}	-	-	20	mA	VDD = 5.6V, rms value
Suspend Current	I_{susp}	-	-	400	μA	VDD = 5.25V, rms value
LVR Trigger Voltage	V_{LVR}	-	2.2	-	V	

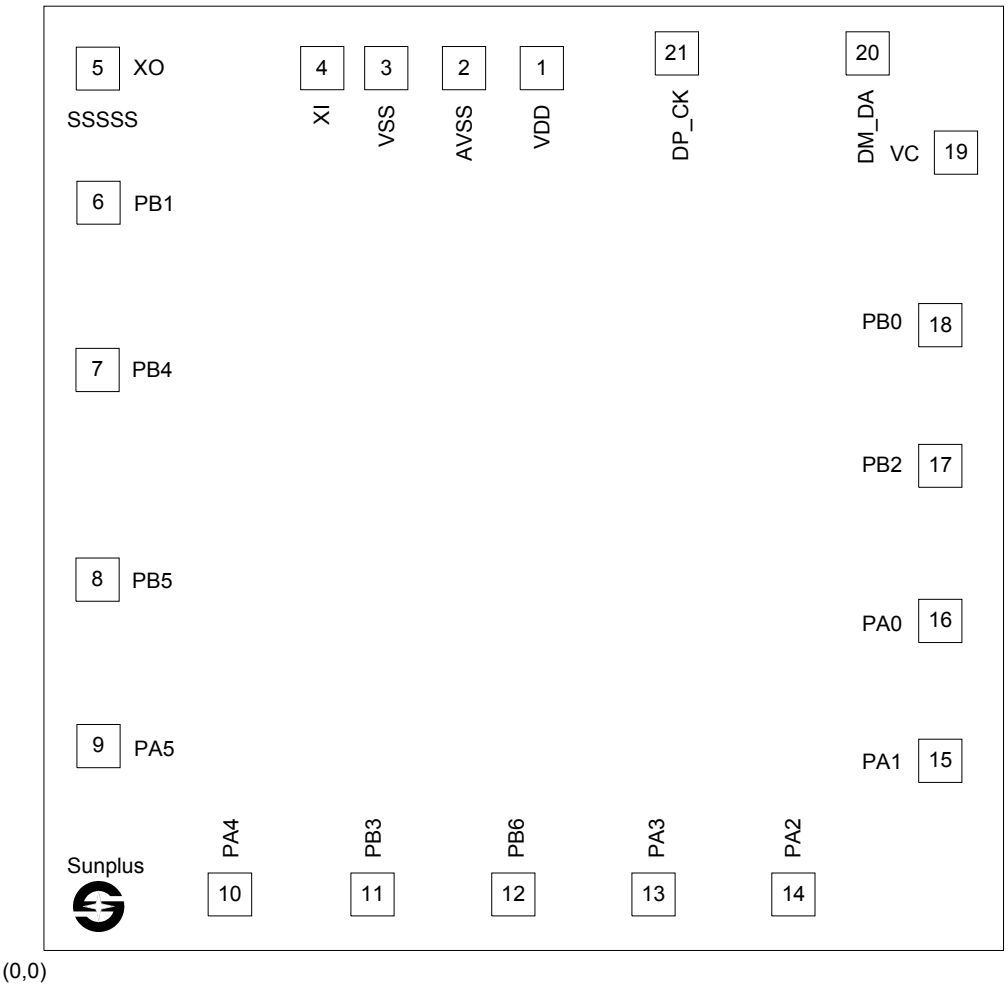
6.3. DC Characteristics

Name	Description	Symbol	Min.	Typ.	Max.	Unit	Test Condition
VC	3.3V regulator output	V_{OH}	3.0	3.3	3.6	V	VDD = 4.4 - 5.25V
DP_CK	Input Voltage High	V_{IH}	2.0	-	-	V	
	Input Voltage Low	V_{IL}	-	-	0.8	V	
	Output Voltage High	V_{OH}	2.8	-	3.6	V	
	Output Voltage Low	V_{OL}	0	-	0.3	V	
	Rise Time	T_{LR}	75	-	300	ns	For C_{LOAD} = 200-600P
	Falling Time	T_{LF}	75	-	300	ns	For C_{LOAD} = 200-600P
	Input Leakage Current	I_{IZ}	-	-	10	μA	
	PS/2 mode Pullup	R_{PPU}	3.5	5.0	6.5	KΩ	
DM_DA	Input Voltage High	V_{IH}	2.0	-	-	V	
	Input Voltage Low	V_{IL}	-	-	0.8	V	
	Output Voltage High	V_{OH}	2.8	-	3.6	V	
	Output Voltage Low	V_{OL}	0	-	0.3	V	
	Rise Time	T_{LR}	75	-	300	ns	For C_{LOAD} = 200-600P, and VDD = 4.4V ~ 5.25V
	Falling Time	T_{LF}	75	-	300	ns	
	Input Leakage Current	I_{IZ}	-	-	10	μA	Internal pull-down disabled
	USB mode Pull-up	R_{PU}	1.20	1.50	1.80	KΩ	
	PS/2 mode Pull-up	R_{MPU}	3.5	5.0	6.5	KΩ	
PA[5:0]	Input Voltage High	V_{IH}	2.0	-	-	V	
	Input Voltage Low	V_{IL}	-	-	0.8	V	
	Input Leakage Current	I_{IZ}	-	-	10	μA	Internal pull-down disabled
	Output Voltage High	V_{OH}	2.4	-	-	V	Source current = 4.0mA
	Output Voltage Low	V_{OL}	-	-	0.5	V	Sink current = 4.0mA
	Pull-down Resistor	R_{PD}	14	20	26	KΩ	Measured at PAD = 1.5V
	Pull-up Resistor	R_{PU}	14	20	26	KΩ	Measured at PAD = 0V

Name	Description	Symbol	Min.	Typ.	Max.	Unit	Test Condition
PB6	Input Voltage High	V_{IH}	2.0	-	-	V	
PB4	Input Voltage Low	V_{IL}	-	-	0.8	V	
PB3	Input Leakage Current	I_{IZ}	-	-	10	μA	Internal pull-up disabled
PB0	Output Voltage High	V_{OH}	2.4	-	-	V	Source current = 4.0mA
	Output Voltage Low	V_{OL}	-	-	0.5	V	Sink current = 4.0mA
	Pull-up Resistor	R_{PU}	7.0	10	13	KΩ	Measured at PAD = 0V
PB2	Input Voltage High	V_{IH}	2.0	-	-	V	
PB1	Input Voltage Low	V_{IL}	-	-	0.8	V	
	Input Leakage Current	I_{IZ}	-	-	10	μA	Internal pull-up disabled
	Output Voltage Low	V_{OL}	-	-	0.5	V	Sink current = 24mA
	Pull-up Resistor	R_{PU}	7.0	10	13	KΩ	Measured at PAD = 0V
PB5	Input Voltage High	V_{IH}	2.0	-	-	V	
	Input Voltage Low	V_{IL}	-	-	0.8	V	
	Input Leakage Current	I_{IZ}	-	-	10	μA	Internal pull-up disabled
	Output Voltage Low	V_{OL}	-	-	0.5	V	Sink current = 4.0mA
	Pull-up Resistor	R_{PU}	7.0	10	13	KΩ	Measured at PAD = 0V

7. PACKAGE/PAD LOCATIONS

7.1. PAD Assignment



Chip Size: 1740μm x 1770μm

This IC substrate should be connected to VSS

Note1: Chip size included scribe line.

Note2: To ensure the IC functions properly, please bond all of VDD and VSS pins.

Note3: The 0.1μF capacitor between VDD and VSS should be placed to IC as closed as possible.

7.2. Ordering Information

Product Number	Package Type
SPCP16A-nnnnV-C	Chip form
SPCP16A-nnnnV-PD04	Package form - PDIP 18
SPCP16A-nnnnV-PD05	Package form - PDIP 20
SPCP16A-nnnnV-PS07	Package form - SOP 20 (300mil)

Note1: Code number (nnnnV) is assigned for customer.

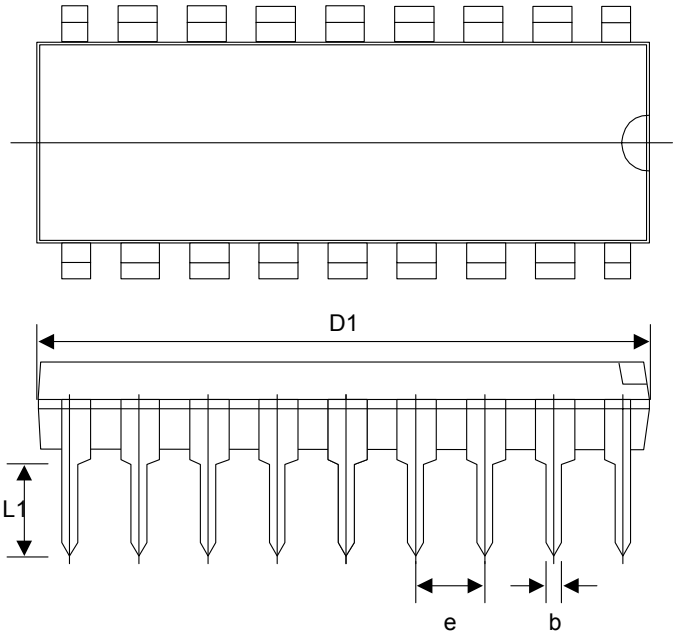
Note2: Code number (nnnn = 0000 - 9999); version (V = A - Z).

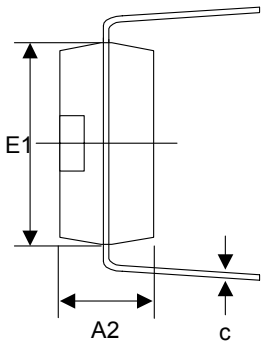
7.3. PAD Locations

Pin	Pad	Name	Att	Rp	X	Y
	1	VDD	PWR		852.44	1513.60
	2	AVSS	PWR		719.30	1513.60
	3	VSS	PWR		586.12	1513.60
	4	XI	I		476.08	1513.60
	5	XO	O		91.00	1513.62
	6	PB1	I/OD		90.50	1284.15
	7	PB4	I/O		90.50	994.38
	8	PB5	I/OD		90.50	633.53
	9	PA5	I/O		90.50	346.20
	10	PA4	I/O		317.50	93.30
	11	PB3	I/O		561.97	93.30
	12	PB6	I/O		804.00	93.30
	13	PA3	I/O		1043.57	93.30
	14	PA2	I/O		1285.60	93.30
	15	PA1	I/O		1538.50	320.30
	16	PA0	I/O		1538.50	562.20
	17	PB2	I/OD		1538.50	829.75
	18	PB0	I/O		1538.50	1071.65
	19	VC	O		1565.03	1369.30
	20	DM_DA	I/O		1413.72	1540.07
	21	DP_CK	I/O		1084.15	1540.07

7.4. Package Information

7.4.1. PDIP 18





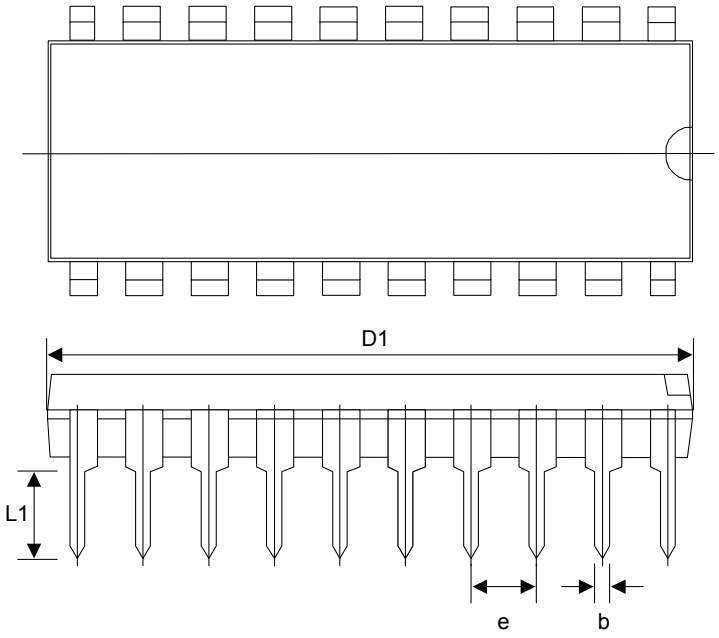
Body Size			Lead Size			
D1	E1	A2	L1	b	c	e
900±10	250±4	130±5	130±15	18±2	10Typ	100Typ

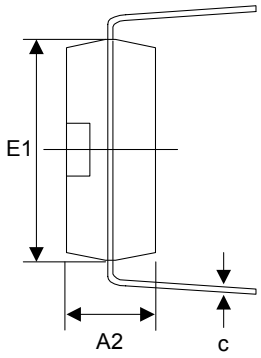
All units are in mil. 1mil = 25.4μm

D1	Body Length
E1	Body Width
A2	Body Thickness
L1	Lead Length
b	Lead Width
c	Lead Thickness
e	Lead Pitch

PDIP-18-300

7.4.2. PDIP 20





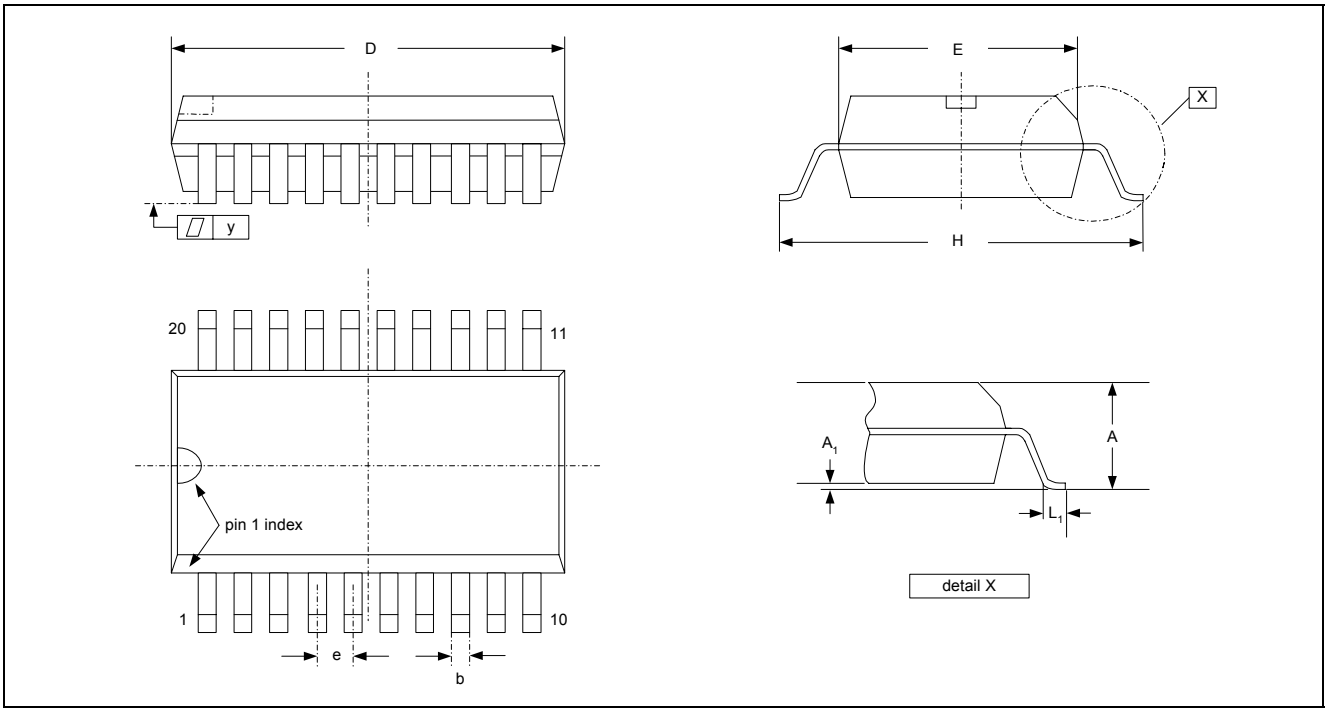
Body Size			Lead Size			
D1	E1	A2	L1	b	c	e
1020±10	250±4	130±5	130±15	18±2	10Typ	100Typ

All units are in mil. 1mil = 25.4μm

D1	Body Length
E1	Body Width
A2	Body Thickness
L1	Lead Length
b	Lead Width
c	Lead Thickness
e	Lead Pitch

PDIP-20-300

7.4.3. SOP 20 (300mil)



Symbol	Dimension in inch		
	Min.	Typ.	Max.
A	0.093	-	0.104
A1	0.004	-	0.012
b	-	0.016	-
D	0.496	-	0.508
E	0.291	-	0.299
e	-	0.050	-
H	0.394	-	0.419
L1	0.016	-	0.050
y	-	-	0.004

8. DISCLAIMER

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9. REVISION HISTORY

Date	Revision #	Description	Page
OCT. 31, 2001	0.1	Original	
JAN. 08, 2002	0.2	Correct PB0 and PB2 description	4
AUG. 12, 2002	1.0	1. Delete "*PRELIMINARY*" 2. Change document title 3. Add section Input Capture Register 4. Remove table USB request summary 5. Add "*7. PACKAGE/PAD LOCATIONS*"	 1, 3 17 19 28 - 30
MAR. 06, 2003	1.1	1. Changed the VCC low spec. for USB from 4.4V to 4.3V 2. Add some programming note for the config_done bit of ext_reg1 3. Modify the mask option table to be same as the tapeout form 4. Modify "*7. PACKAGE/PAD LOCATIONS*"	3, 26 14 25 28 - 32