

SPCR02A

Sound Controller with 40KB MROM and Serial RAM Interface

SEP. 19, 2001

Version 1.5

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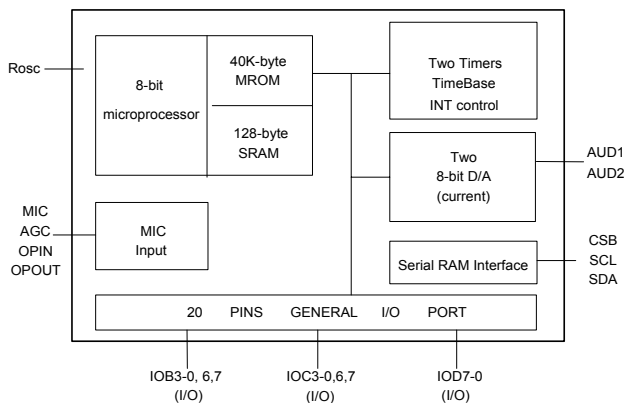
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SOUND CONTROLLER WITH 40KB MROM AND SERIAL RAM INTERFACE

1. GENERAL DESCRIPTION

The SPCR02A is a CPU based device for recording (one channel) and playback (two channel) that includes a CMOS 8-bit microprocessor, 40K-byte MROM (speech is compressed by 4-bit ADPCM with approx. 12sec. speech duration @ 7KHz sampling rate). It also includes Serial SRAM Interface and 128-byte working SRAM. It includes two Timer/Counters, 20 software selectable I/Os, two 8-bit audio current output D/A, MIC (microphone) input, and AGC function. For audio processing, melody and speech can be mixed into one output. It operates over a single power voltage range of 2.4V - 5.5V. In addition, the SPCR02A has a Clock Stop mode for power savings. The power savings mode saves the SRAM contents, but freezes the oscillator, causing all other chip functions to be inoperative. The Max. CPU clock frequency is 6.0MHz. It has an instruction cycle rate of 2 clock cycles (min.) - 6 clock cycles (max.). The SPCR02A includes, not only the latest technology, but also the full commitment and technical support of Sunplus.

2. BLOCK DIAGRAM



3. FEATURES

- 8-bit microprocessor
- Software-based audio processing
- Provides 40K-byte MROM for program and audio data with approx. 12 sec. speech @ 7KHz sampling rate with ADPCM
- 128-bytes working SRAM
- Operating voltage (single power): 2.4V - 3.6V
3.6V - 5.5V
- Supports Rosc
- Max. CPU clock speed: 6.0MHz @ 5.0V
- Serial SRAM Interface
- Standby mode (Clock Stop mode) for power savings.
Max. 5 μ A @ 5.0V
- Below 1000ns instruction cycle time @ 4.0MHz CPU clock
- Provides 20 general I/Os
- Two 12-bit timer/counters
- Two 8-bit audio current output (D/A)
- 6 INT sources
- Sunplus Serial SRAM Chip-Set Options
 - SPRS256A (10sec @ 6.4KHz sampling rate)
 - SPRS512C (20sec @ 6.4KHz sampling rate)
 - SPRS1024C (40sec @ 6.4 Sampling Rate)
- Key wake -up function
- MIC input with AGC and Comparator

4. APPLICATION FIELD

- Intelligent education toys
 - Ex. Pattern to voice (animal, car, color, etc.)
 - Spelling (English or Chinese)
 - Math
- High end toy controller
- Talking instrument controller
- General speech recorder
- Interactive games
- Industrial controller

5. SIGNAL DESCRIPTIONS*

Mnemonic	PIN No.	Type	Description
VDD	10	I	Positive supply for logic and I/O pins.
VSS	3	I	Ground reference for logic and I/O pins.
RESET	4	I	RESET input (This pin is active low reset for the chip)
ROSC	11	I	ROSC input
SDA	21	I/O	External SRAM interface with the following Serial SRAM Chip-Set Options: SPRS256A, SPRS512C, and SPRS1024C.
SCL	22	O	
CSB	23	O	
AUD1	17	O	AUDIO output A
MIC	13	I	Microphone input
OPIN	15	I	Preamplifier Input
OPOUT	16	O	Preamplifier Output
ALC	14	I	Automatic Gain Control
AUD2	12	O	AUDIO output B
IOB0	30	I/O	Port B is an 8-bit bi-directional programmable Input / Output port with Pull-low or Open-drain option. As inputs, Port B can be in either the Pure or Pull-low states. As outputs, Port B can be either Buffer or Open-drain NMOS types (Sink current). **See note 1 and 2 below.
IOB1	31	I/O	
IOB2	32	I/O	
IOB3	33	I/O	
IOB6	1	I/O	
IOB7	2	I/O	
IOC0	24	I/O	Port C is an 8-bit bi-directional programmable Input / Output port with Pull-high or Open-drain option. As inputs, Port C can be in either the Pure or Pull-high states. As outputs Port C can be a Buffer or Open-drain type. Port C3 - C0 are Open-drain NMOS type (Sink current) and Port C7 - C6 are Open-drain NMOS (Sink current). IOC1: EXT INT IN IOC2: EXT COUNT IN **See note 1 and 2 below.
IOC1	25	I/O	
IOC2	26	I/O	
IOC3	27	I/O	
IOC6	28	I/O	
IOC7	29	I/O	
IOD0	20	I/O	Port D is an 8-bit bi-directional Input / Output port with Pull-low or Open-drain option. As inputs, Port D can be either Pure or Pull-low states. As outputs, Port D can be either Buffer or Open-drain PMOS (send current). Also, Port D can be software programmed for wake-up I/O pins. (Key change, Wake up I/O) **See note 1 and 2 below.
IOD1	19	I/O	
IOD2	18	I/O	
IOD3	9	I/O	
IOD4	8	I/O	
IOD5	7	I/O	
IOD6	6	I/O	
IOD7	5	I/O	

* Refer to SPC Programming Guide for complete information.

**Note: 1.) Three input states can be specified; Pure Input, Pull-High or Pull Low.

2.) Three output states can be specified as Buffer output, Open Drain PMOS output (send), or Open Drain NMOS output (sink).

6. FUNCTIONAL DESCRIPTIONS

6.1. CPU

The SPCR02A 8-bit microprocessor is a high performance processor equipped with Accumulator, Program Counter, X Register, Stack pointer and Processor Status Register (this is the same as the 6502 instruction structure). SPCR02A is able to perform with 6.0MHz (max.) depending on the application specifications.

6.2. ROM Area

The SPCR02A provides a 40K-byte MROM that can be defined as the program area, audio data area, or both.

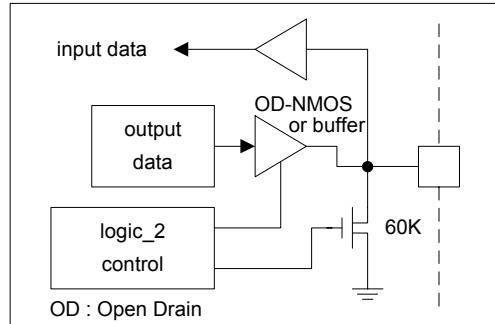
6.3. RAM Area

The SPCR02A total RAM consists of 128 bytes (including Stack) at locations from \$80 through \$FF.

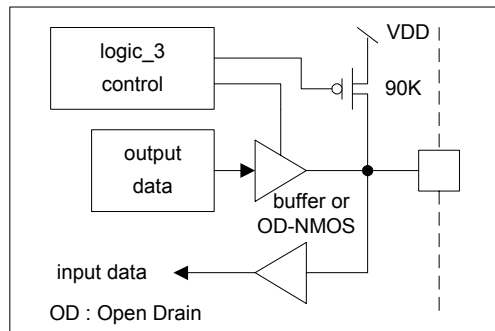
6.4. Map of Memory and I/Os

<p>*I/O PORT:</p> <ul style="list-style-type: none"> - PORT IOB \$0003 <li style="padding-left: 20px;">IOC \$0004 <li style="padding-left: 20px;">IOD \$0005 - I/O CONFIG \$0000 <li style="padding-left: 20px;">\$0001 <p>*NMI SOURCE:</p> <ul style="list-style-type: none"> - INTA (from TIMER A) <p>*INT SOURCE:</p> <ul style="list-style-type: none"> - INTA (from TIMER A) - INTB (from TIMER B) - CPU CLK / 1024 - CPU CLK / 8192 - CPU CLK / 65536 - EXT INT 	<p>*MEMORY MAP (From ROM view)</p> <table border="1" style="border-collapse: collapse; width: 100%;"> <tr> <td style="text-align: right; padding-right: 5px;">\$00000</td> <td style="padding: 5px;">HW register, I/Os</td> </tr> <tr> <td style="text-align: right; padding-right: 5px;">\$00080</td> <td style="padding: 5px;">USER RAM and STACK</td> </tr> <tr> <td style="text-align: right; padding-right: 5px;">\$00100</td> <td style="padding: 5px;">DUMMY for ice debug</td> </tr> <tr> <td style="text-align: right; padding-right: 5px;">\$06000</td> <td style="padding: 5px;">USER'S PROGRAM & DATA AREA</td> </tr> <tr> <td style="text-align: right; padding-right: 5px;">\$0FFFF</td> <td></td> </tr> </table>	\$00000	HW register, I/Os	\$00080	USER RAM and STACK	\$00100	DUMMY for ice debug	\$06000	USER'S PROGRAM & DATA AREA	\$0FFFF	
\$00000	HW register, I/Os										
\$00080	USER RAM and STACK										
\$00100	DUMMY for ice debug										
\$06000	USER'S PROGRAM & DATA AREA										
\$0FFFF											

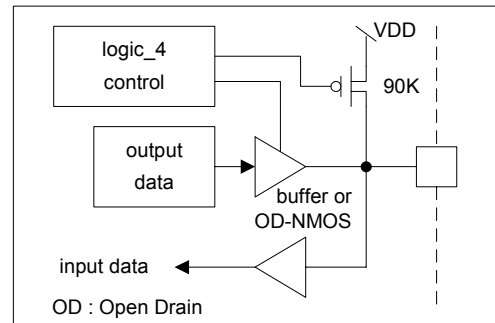
Input/Output IOB port : IOB7,6



Input/Output IOC port : IOC3 - 0

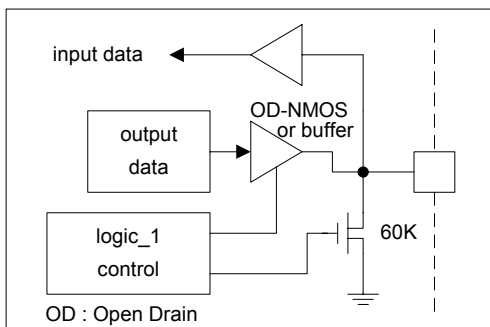


Input/Output IOC port : IOC7,6

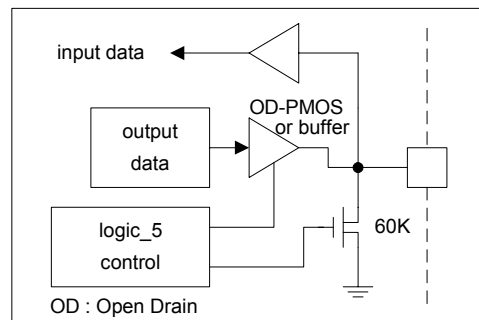


6.5. I/O Port Configurations*

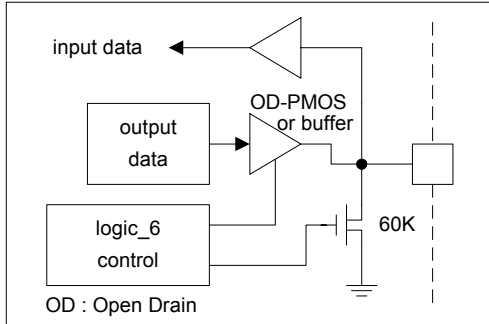
Input/Output IOB port : IOB3 - 0



Input/Output IOD port : IOD3 - 0



Input/Output IOD port : IOD7 - 4



*Values shown are for VDD = 5.0V test conditions only.

6.6. Timer/Counter

The SPCR02A contains two 12-bit timer/counters, TMA and TMB respectively. TMA can be specified as a timer or a counter, but TMB can only be used as a timer. In the timer mode, TMA and TMB are re-loaded up-counters. When timer overflows from \$0FFF to \$0000, the carry signal will make the timer automatically reload to the user's pre-set value and be up-counted again. At the same time, the carry signal will generate the INT signal if the corresponding bit is enabled in the INT ENABLE Register. If TMA is specified as a counter, users can reset by loading #0 into the counter. After the counter has been activated, the value of the counter can also be read from the counters at the same time. The read instruction will not reset or affect the value of the counter.

6.8. Power Savings Mode

The SPCR02A provides a power savings mode (Standby mode) for those applications that require very low stand-by current. To enter standby mode, the Wake-Up Register should be enabled and then stop the CPU clock by writing the STOP CLOCK Register. The CPU will then go to the stand-by mode. In such a mode, RAM and I/Os will remain in their previous states until being

Clock source of Timer/Counter can be selected as follows:

Timer/Counter		Clock Source
TMA	12-BIT TIMER	CPU CLOCK (T) or T/4
	12-BIT COUNTER	T/64, T/8192, T/65536 or EXT CLK
TMB	12-BIT TIMER	T or T/4
MODE SELECT REGISTER		TMA only, select timer or counter
TIMER CLOCK SELECTOR		Select T or T/4

6.7. Speech and Melody

Since the SPCR02A provides a large ROM and wide range of CPU operation speeds, it is most suitable for speech and melody synthesis.

For speech synthesis, the SPCR02A can provide NMI for accurate sampling frequency. For recording users can record the sound and digitize it into the external Serial SRAM. The sound data can be played back in the sequence of the control functions as designed by the user's program. For pre-recorded data several algorithms are recommended for high fidelity and compression of sound including PCM, LOG PCM, and ADPCM.

For melody synthesis, the SPCR02A provides the dual tone mode. After selecting the dual tone mode, users only need to fill either TMA or TMB, or both TMA and TMB to generate expected frequency for each channel. The hardware will toggle the tone wave automatically without entering into an interrupt service routine. Users are able to simulate musical instruments or sound effects by simply controlling the envelope of tone output.

awakened. Port IOD7-0 is the only wake-up source in the SPCR02A. After the SPCR02A is awakened, the internal CPU will go to the RESET State ($T_w \geq 65536 \times T_1$) and then continue processing the program. Wakeup Reset will not affect RAM or I/Os. (See FIG.1)

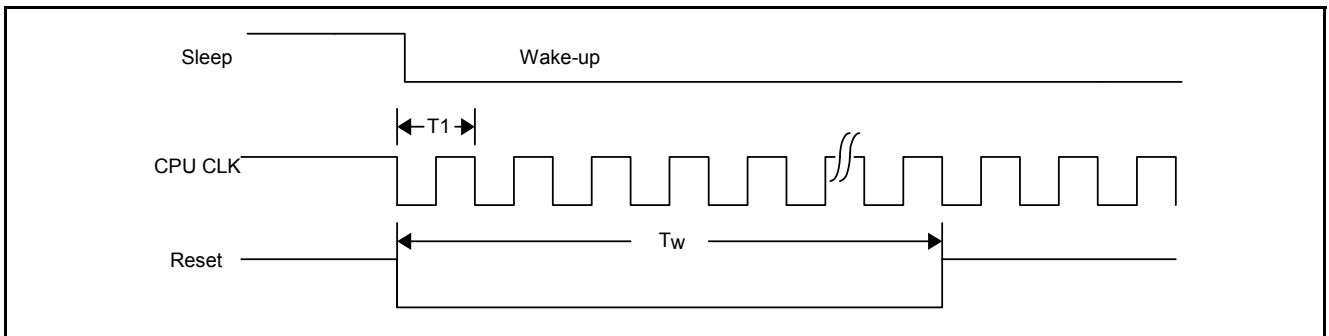


FIG. 1

$$T_1 = 1 / (F_{CPU}), T_w \geq 65536 \times T_1$$

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to $V_+ + 0.5V$
Operating Temperature	T_A	-10°C to +70°C
Storage Temperature	T_{STO}	-50°C to +150°C

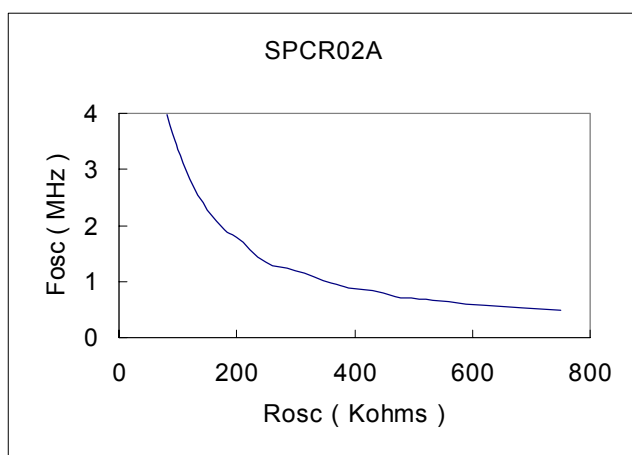
Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. DC/AC Characteristics

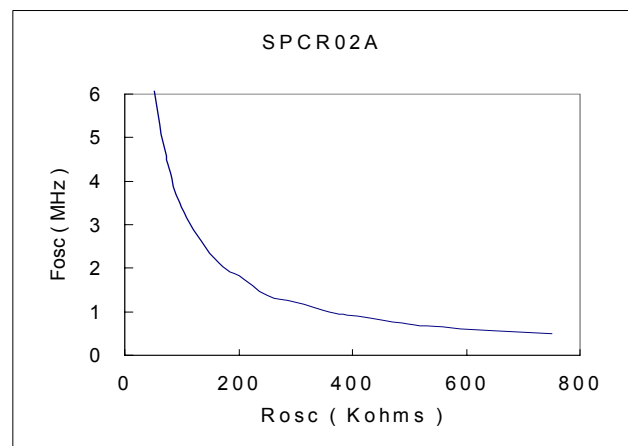
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	5.5	V	
Operating Current	I_{OP}	-	4.0	10	mA	$F_{OSC} = 4.0MHz @ 5.0V$, no load
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 5.0V
OSC frequency	F_{OSC}	-	3.0	6.0	MHz	VDD = 5.0V
Audio output current	I_{AUD}	-	-1.2	-	mA	VDD = 5.0V
Input high level	V_{IH}	3.0	-	-	V	VDD = 5.0V
Input Low level	V_{IL}	-	-	0.8	V	VDD = 5.0V
Output high I IOB, IOC, IOD	I_{OH}	-1.0	-	-	mA	VDD = 5.0V $V_{OH} = 4.2V$
Output sink I IOB, IOC, IOD	I_{OL}	4.0	-	-	mA	VDD = 5.0V $V_{OL} = 0.8V$
Input resistor IOB, IOC, IOD	R_{IN}	-	30	-	Kohm	Pull Low or Pull High
OSC frequency	F_{CPU}	-	-	4.0	MHz	VDD = 3.0V

7.3. The Relationship between the R_{OSC} and the F_{CPU}

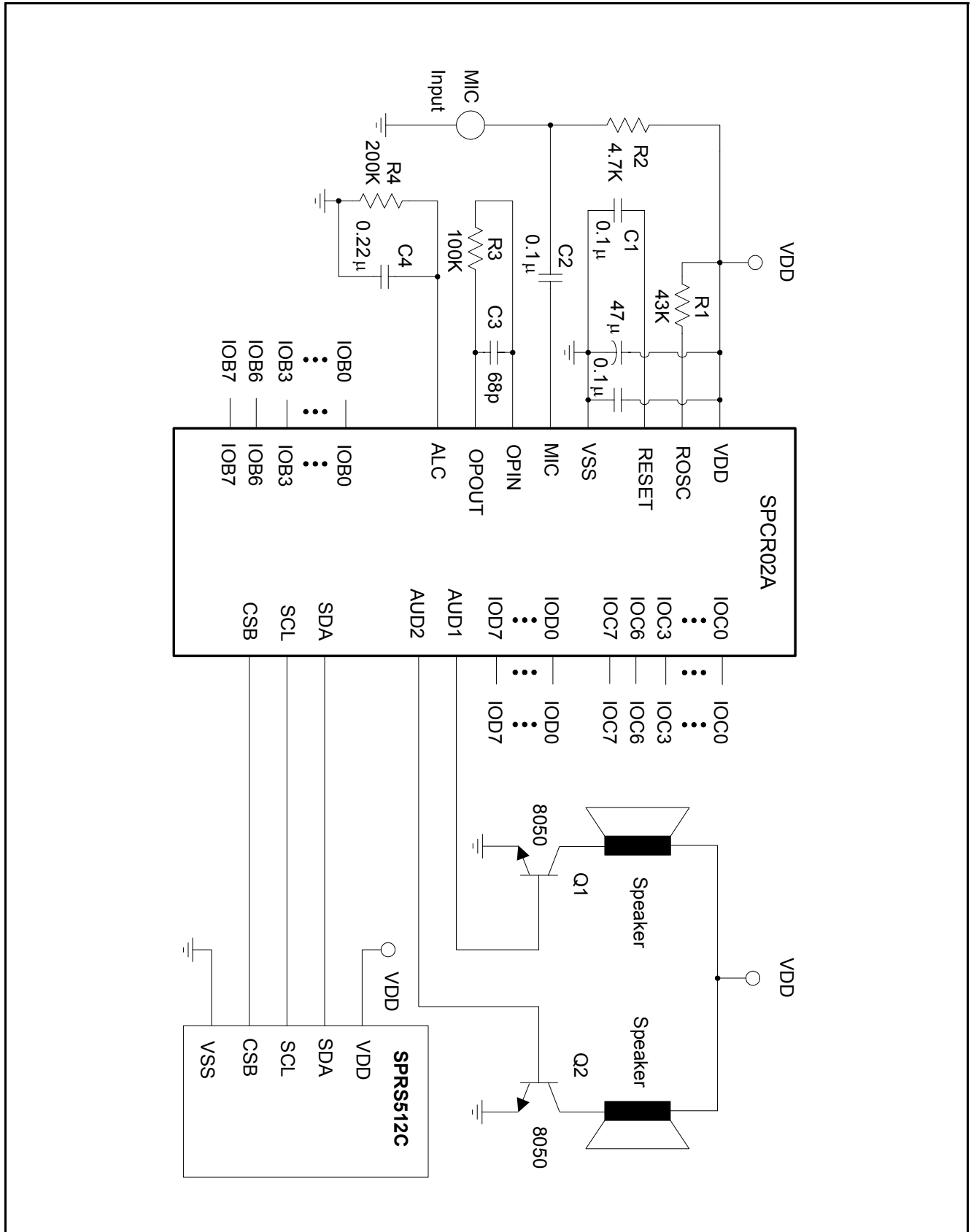
7.3.1. VDD = 3.0V, $T_A = 25^\circ C$



7.3.2. VDD = 4.5V, $T_A = 25^\circ C$

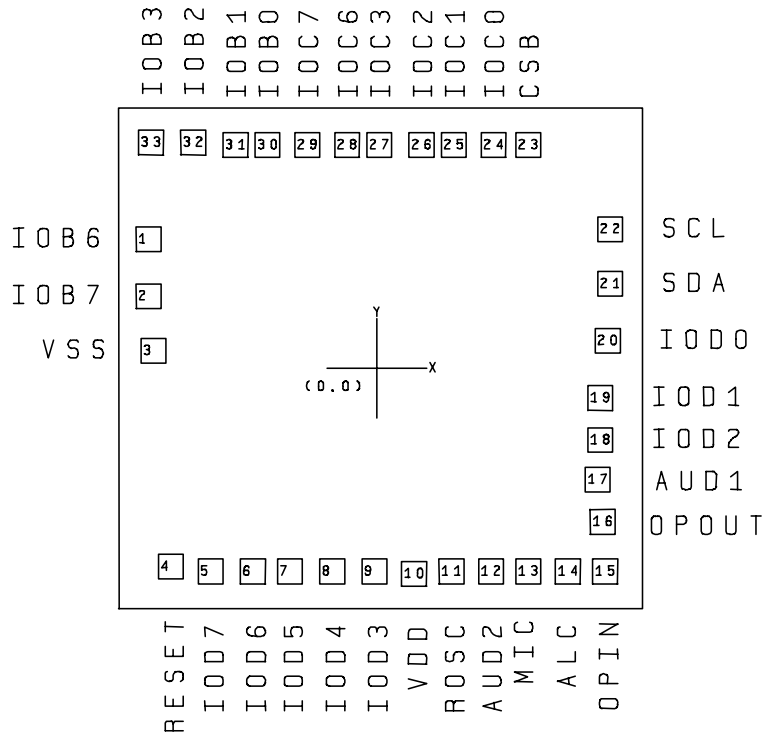


8. APPLICATION CIRCUIT



9. PACKAGE/PAD LOCATIONS

9.1. PAD Assignment



Chip Size: 2220 μ m x 2120 μ m

This IC substrate should be connected to VSS

Note1: Chip size included scribe line.

Note2: The 0.1 μ F capacitor between VDD and VSS should be placed to IC as close as possible.

9.2. Ordering Information

Product Number	Package Type
SPCR02A-nnnnV-C	Chip form

Note1: Code number (nnnnV) is assigned for customer.

Note2: Code number (nnnn = 0000 - 9999); version (V = A - Z).

9.3. PAD Locations

PAD No.	PAD Name	X	Y
1	IOB6	-915	518
2	IOB7	-917	288
3	VSS	-897	63
4	RESET	-833	-807
5	IOD7	-669	-825
6	IOD6	-502	-825
7	IOD5	-345	-825
8	IOD4	-175	-825
9	IOD3	-14	-825
10	VDD	152	-832
11	ROSC	304	-821
12	AUD2	465	-821
13	MIC	614	-821
14	ALC	775	-821
15	OPIN	925	-821
16	OPOUT	908	-620
17	AUD1	891	-451
18	IOD2	904	-290
19	IOD1	904	-121
20	IOD0	935	106
21	SDA	937	333
22	SCL	937	557
23	CSB	613	893
24	IOC0	474	892
25	IOC1	313	895
26	IOC2	176	894
27	IOC3	15	893
28	IOC6	-119	894
29	IOC7	-278	893
30	IOB0	-437	898
31	IOB1	-569	897
32	IOB2	-742	903
33	IOB3	-908	901

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
NOV. 28, 1997	1.0	Original	
DEC. 27, 1997	1.1	Modify error. IOB4 -> IOB6, IOB5 -> IOB7, IOC4 -> IOC6, IOC5 -> IOC7	
FEB. 06, 1998	1.2	Modify error. IOB4 -> IOB6, IOB5 -> IOB7, IOC4 -> IOC6, IOC5 -> IOC7	2, 3, 7
AUG. 18, 1998	1.3	Correction error.	
DEC. 15, 1999	1.4	1. Modify Format 2. Add PIN No. 3. Add " <u>DISCLAIMER</u> "	
SEP. 19, 2001	1.5	1. Modify operating voltage: 2.4V - 3.4V -> 2.4V - 3.6V 2. Correct chip size 3. Add Note1 and Note2 in the " <u>9.1 PAD Assignment</u> " 4. Renew to a new document format	3 9 9