SPE0504
4-Line ESD Protection Array

DESCRIPTION

The SPE0504 are designed by TVS array that is to protect sensitive electronics from damage or latch-up due to ESD. They are designed for use in applications where board space is at a premium. SPE0504 will protect up to four line, and may be used on lines where the signal polarities swing above and below ground.

SPE0504 offer desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.

SPE0504 may be used to meet the immunity requirements of IEC 61000-4-2, level 4. The small SOT-23-6L package makes them ideal for use in portable electronics such as cell phones, PDA's, notebook computers, and digital cameras.

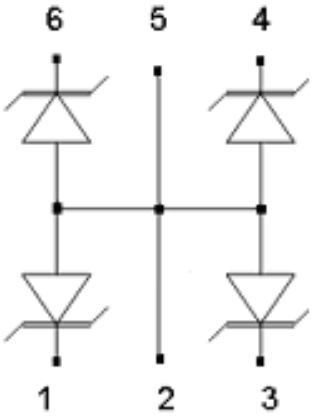
APPLICATIONS

- Cellular Handsets and Accessories
- Cordless Phone
- PDA
- Notebooks and Handhelds
- Portable Instrumentation
- Digital Cameras
- MP3 Player

FEATURES

- Transient protection for data lines to
  IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
  IEC 61000-4-4 (EFT) 40A (5/50ns)
- Protects four I/O lines
- Working voltage: 5V
- Low leakage current
- Low operating and clamping voltages

PIN CONFIGURATION (SOT-23-6L)



PART MARKING

Y : Year Code
W : Week Code

SPE0504
4-Line ESD Protection Array

ORDERING INFORMATION

Part Number	Package	Part Marking
SPE0504S26RGB	SOT-23-6L	E4

※ Week Code : A ~ Z(1 ~ 26) ; a ~ z(27 ~ 52)

※ SPE0504S26RGB : Tape Reel ; Pb – Free ; Halogen – Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

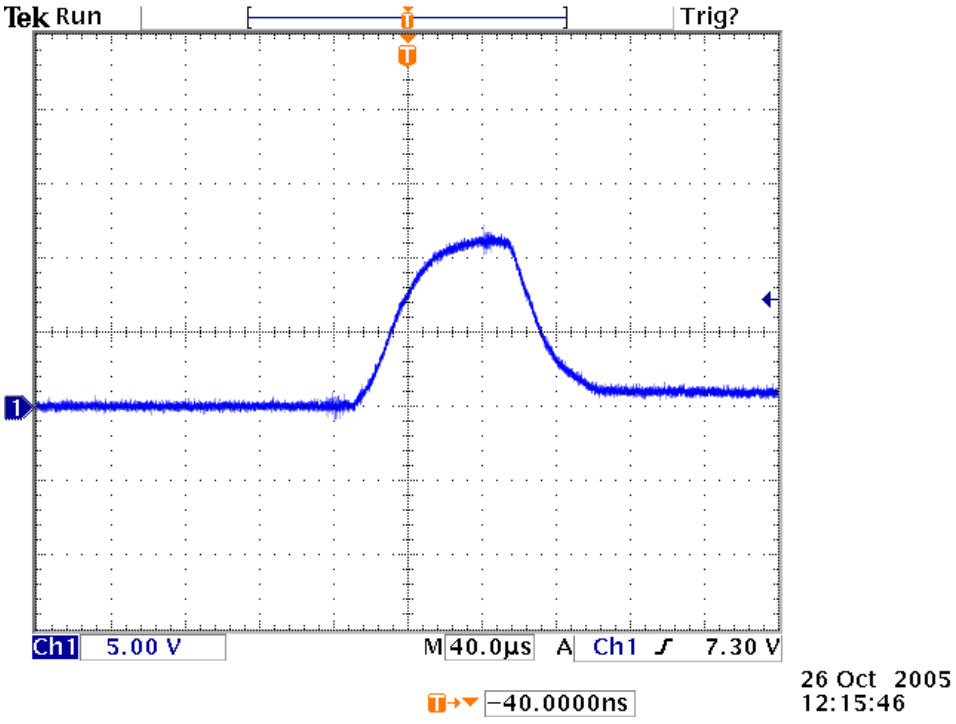
Parameter	Symbol	Typical	Unit
Peak Pulse Power (tp = 8/20 μs)	Ppk	250	W
Maximum Peak Pulse Current (tp = 8/20 μs)	Ipp	7	A
ESD per IEC 61000 – 4 – 2 (Air)	Vpp	±15	KV
ESD per IEC 61000 – 4 – 2 (Contact)	Vpp	±8	KV
Operating Junction Temperature	T_J	-55 ~ 125	℃
Storage Temperature Range	T_{STG}	-55 ~ 150	℃
Lead Soldering Temperature	T_L	260 (10sec)	℃

ELECTRICAL CHARACTERISTICS

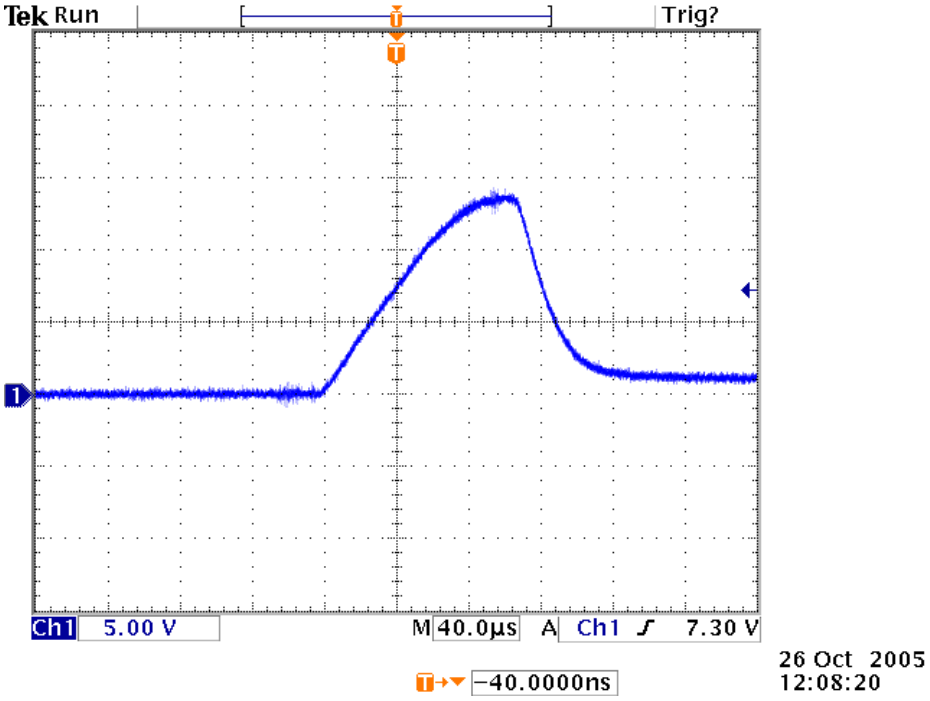
(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Reverse Stand – Off Voltage	V_{RWM}				5	V
Reverse Breakdown Voltage	V_{BR}	It = 1mA	6			V
Reverse Leakage Current	I_R	V_{RWM} = 5V , T=25℃		0.01	1	μA
Reverse Leakage Current	I_R	V_{RWM} = 3V , T=25℃		0.01	0.5	μA
Clamping Voltage	V_C	Ipp = 1A , tp = 8/20 μs			11	V
Clamping Voltage	V_C	Ipp = 7A , tp = 8/20 μs			15	V
Junction Capacitance	Cj	Between I/O Pin and GND V_R = 0V , f = 1MHz		10	20	pF

TYPICAL CHARACTERISTICS



Clamping Voltage (Ipp = 1A , tp = 8/20 µs)



Clamping Voltage (Ipp = 7A , tp = 8/20 µs)

TYPICAL CHARACTERISTICS

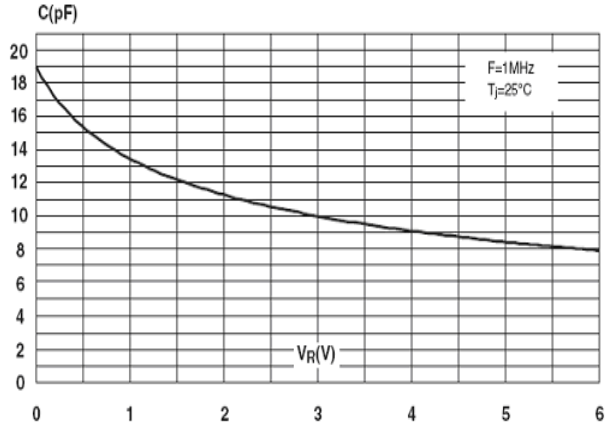


Fig 1 : Junction Capacitance V.S Reverse Voltage Applied

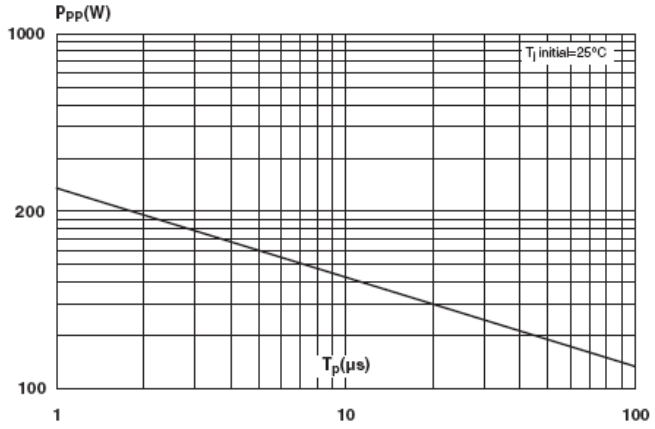


Fig 2 : Peak Plus Power V.S Exponential Plus Duration

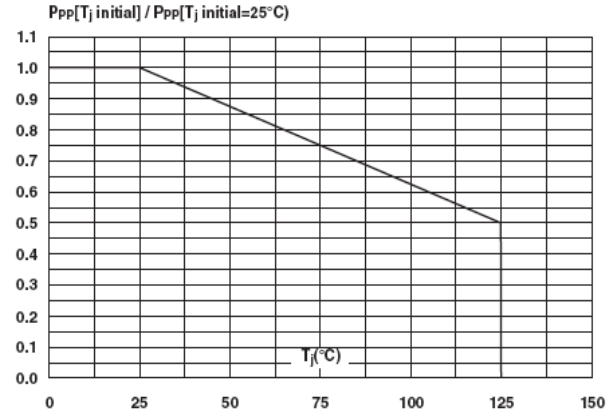


Fig 3 : Relative Variation of Peal Plus Power V.S Initial Junction Temperature

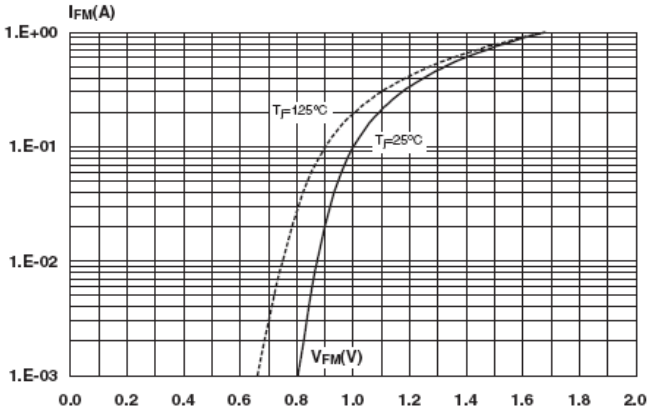


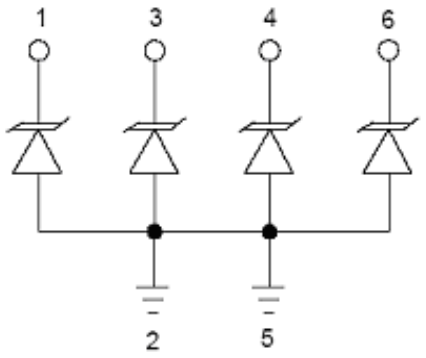
Fig 4 : Forward Voltage Drop V.S Peak Forward Current

APPLICATION NOTE

Device Connection for Protection of Four Data Lines

SPE0504 is designed to protect up to four data lines. The device is connected as follows:

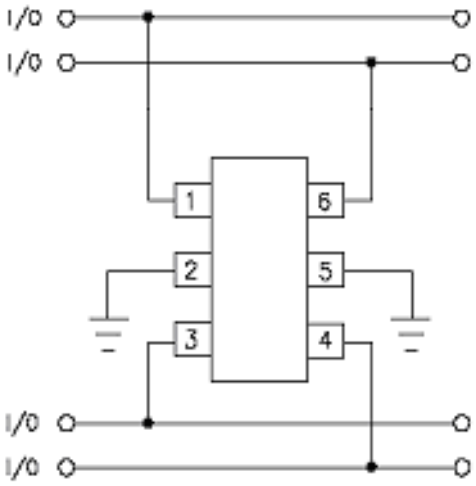
1. The TVS protection of four I/O lines is achieved by connecting pins 1, 3, 4 and 6 to the data lines. Pin 2 and 5 are connected to ground. The ground connection should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance.



Circuit Board Layout Recommendations for Suppression of ESD

Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

1. Place the TVS near the input terminals or connectors to restrict transient coupling.
2. Minimize the path length between the TVS and the protected line.
3. Minimize all conductive loops including power and ground loops.
4. The ESD transient return path to ground should be kept as short as possible.
5. Never run critical signals near board edges.
6. Use ground planes whenever possible.



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