



SPEAR-09-B042

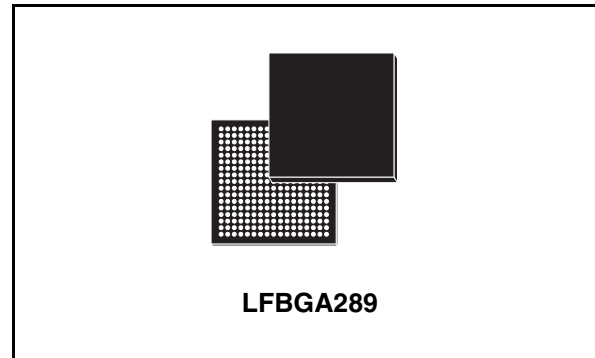
SPEAr[®] BASIC

ARM 926EJ-S core, customizable logic, large IP portfolio SoC

Preliminary Data

Features

- ARM926EJ-S core @333 MHz
 - 16 Kbyte instructions/data cache
- Reconfigurable logic array:
 - 300 Kgate (100% utilization rate)
 - 102 I/O lines
 - No clock domain limitation
 - 64 Kbyte + 8 Kbyte configurable memory pool
- Multilayer AMBA 2.0 compliant bus with f_{MAX} 166 MHz
- 32-Kbyte boot ROM
- 8 Kbyte common static RAM
 - Shared with reconfigurable array
- Dynamic power saving features
- High performance DMA
 - 8 channels
- Ethernet 10/100 MAC with MII interface. (IEEE-802.3)
- USB 2.0 device with integrated PHY
- 2 USB 2.0 host with integrated PHY
- External DRAM memory interface:
 - 8/16-bit (LPDDR@166 MHz)
 - 8/16-bit (DDR2@333 MHz)
 - 2 banks available
- Flash interface:
 - SPI serial (up to 50 Mbps)
- SPI master/slave up to 50 Mbps
 - Compliant with Motorola, Texas instruments and National semiconductor protocols
- I²C master/slave mode – high, fast and slow speed
- UARTs (up to 460.8 Kbps)
- IrDA (FIR/MIR/SIR) compliant serial link from 9.6 Kbps to 4 Mbps speed-rate



- 6 legacy GPIO bidirectional signals with interrupt capability
- ADC 10-bit, 1 Msps 8 inputs
 - Hw supporting up to 13.5 bits at 8 KSPS by oversampling and accumulation
- JPEG codec accelerator (1 clock/pixel)
- C3 crypto accelerator
- 3 pairs of 16-bit general purpose timers with programmable prescaler
- Real-time clock
- Watchdog
- System controller
- Miscellaneous internal control registers
 - SOC parameter configuration
- JTAG (IEEE1149.1) interface
- ETM9 interface
- Operating temperature: - 40 to 85 °C
- Low power consumption technology

Description

SPEAr BASIC is a powerful digital engine belonging to SPEAr family, the innovative customizable system-on-chip. The device integrates an ARM 926 core with an extensive set of proven IPs and a large configurable logic block that allows very fast customization of unique and/or proprietary solutions.

Contents

1	Reference documentation	7
2	Product overview	8
3	Features	9
4	Architecture properties	10
5	Block diagram	11
5.1	Core architecture	11
6	Pins description	12
6.1	Functional pin group	12
6.2	Special I/Os	19
6.2.1	USB 2.0 transceiver	19
6.2.2	SSTL_2/SSTL_18	19
7	Memory map	20
8	Main blocks	23
8.1	CPU subsystem	23
8.1.1	Overview	23
8.1.2	CPU ARM 926EJ-S	23
8.2	Clock and reset system	24
8.3	Main oscillator	25
8.3.1	Crystal connection	25
8.3.2	Crystal equivalent model	25
8.4	RTC oscillator	26
8.4.1	Crystal connection	26
8.4.2	Crystal equivalent model	26
8.5	Ethernet controller	27
8.6	USB2 host controller	27
8.7	USB2 device controller	28
8.8	32-Kbyte boot ROM	28

8.9	Serial memory interface	29
8.10	JPEG (codec)	29
8.11	Cryptographic co-processor (C3)	30
8.12	Low jitter PLL	30
8.13	Main PLL	30
8.13.1	PLL block diagram	31
8.13.2	Normal mode	31
8.13.3	Fractional mode	31
8.13.4	Double side dithering mode	31
8.13.5	Single side dithering mode	31
8.14	ADC controller	32
8.15	UART	32
8.16	IrDA	32
8.17	SPI	32
8.18	I ² C	33
8.19	DDR memory controller	33
8.20	Reconfigurable logic array	33
8.20.1	Overview	33
8.20.2	Custom project development	34
8.20.3	Customization process	34
9	Standard customization	35
9.1	Features	35
9.2	Block diagram	36
9.3	Standard customization memory map	37
9.4	PL_GPIO sharing scheme	38
9.4.1	LCD controller	41
9.4.2	SD card controller	42
9.4.3	Flexible static memory controller	43
9.4.4	Keyboard interface	44
9.4.5	TDM interface	45
9.4.6	I2S interface	48
9.4.7	SPI_I2C cell	49
9.4.8	GPIO_IT cell	50
9.4.9	One bit DAC	50

9.4.10	ADC enhanced control	51
9.4.11	Camera interface	51
9.4.12	Interrupt and DMA request management	55
9.5	TDM timing	58
9.5.1	I2S interface timings	59
10	Electrical characteristics	60
10.1	Absolute maximum ratings	60
10.2	DC electrical characteristics	61
10.3	General purpose I/O characteristics	61
10.4	LPDDR and DDR2 pad electrical characteristics	62
10.5	Power up sequence	62
10.6	PowerGood	62
11	Package information	63
12	Order code	64
13	Revision history	65

List of tables

Table 1.	Pin description by functional group	12
Table 2.	Power supply	19
Table 3.	Main memory map	20
Table 4.	ICM1 – Low speed connection	20
Table 5.	ICM4 – High speed connection.	21
Table 6.	ML1 – Multi layer CPU subsystem	21
Table 7.	ICM3 – Basic subsystem	22
Table 8.	Equivalent values	25
Table 9.	Equivalent values	26
Table 10.	Endpoint assignments	28
Table 11.	Reconfigurable logic array interfaces	33
Table 12.	RAS_M – communication subsystem	37
Table 13.	PL_CLK mapping	38
Table 14.	PL_GPIO mapping	38
Table 15.	KBREG coding	44
Table 16.	TDM block pins	45
Table 17.	I2S interface pins	49
Table 18.	DAC performances	51
Table 19.	Maximum picture size according data format and buffer size.	53
Table 20.	Camera interface pinout	54
Table 21.	Camera interface timing specification	55
Table 22.	TDM timing specification (1024 TS = 65536 kHz = 15.26 ns).	58
Table 23.	I2S timing specification	59
Table 24.	Absolute maximum rating	60
Table 25.	Recommended operating condition	61
Table 26.	Low voltage TTL DC input specification (3V < V _{DD} < 3.6V)	61
Table 27.	Low voltage TTL DC output specification (3V < V _{DD} < 3.6V)	61
Table 28.	Pull-up and pull-down characteristics	61
Table 29.	DC characteristics	62
Table 30.	Driver characteristics	62
Table 31.	On die termination	62
Table 32.	Reference voltage	62
Table 33.	Ordering information	64
Table 34.	Document revision history	65

List of figures

Figure 1.	SPEAr BASIC functional interfaces	8
Figure 2.	Block diagram	11
Figure 3.	Crystal connection	25
Figure 4.	Crystal equivalent model	25
Figure 5.	Crystal connection	26
Figure 6.	Crystal equivalent model	26
Figure 7.	PLL block diagram	31
Figure 8.	SPEAr BASIC standard block diagram	36
Figure 9.	Pre-defined frame sync shapes (slave or master)	46
Figure 10.	Switching constant delay between TSy and TSx	47
Figure 11.	Type of data carried by the TDM	48
Figure 12.	External HSYNC synchronization	51
Figure 13.	External VSYNC synchronization	52
Figure 14.	ITU656 embedded synchronization	52
Figure 15.	CSI2 embedded synchronization	53
Figure 16.	Camera interface waveforms	54
Figure 17.	Interrupt and DMA block for telecom peripherals	57
Figure 18.	TDM signals description	58
Figure 19.	TDM signals description	59
Figure 20.	LFBGA289 mechanical data and package dimensions	63

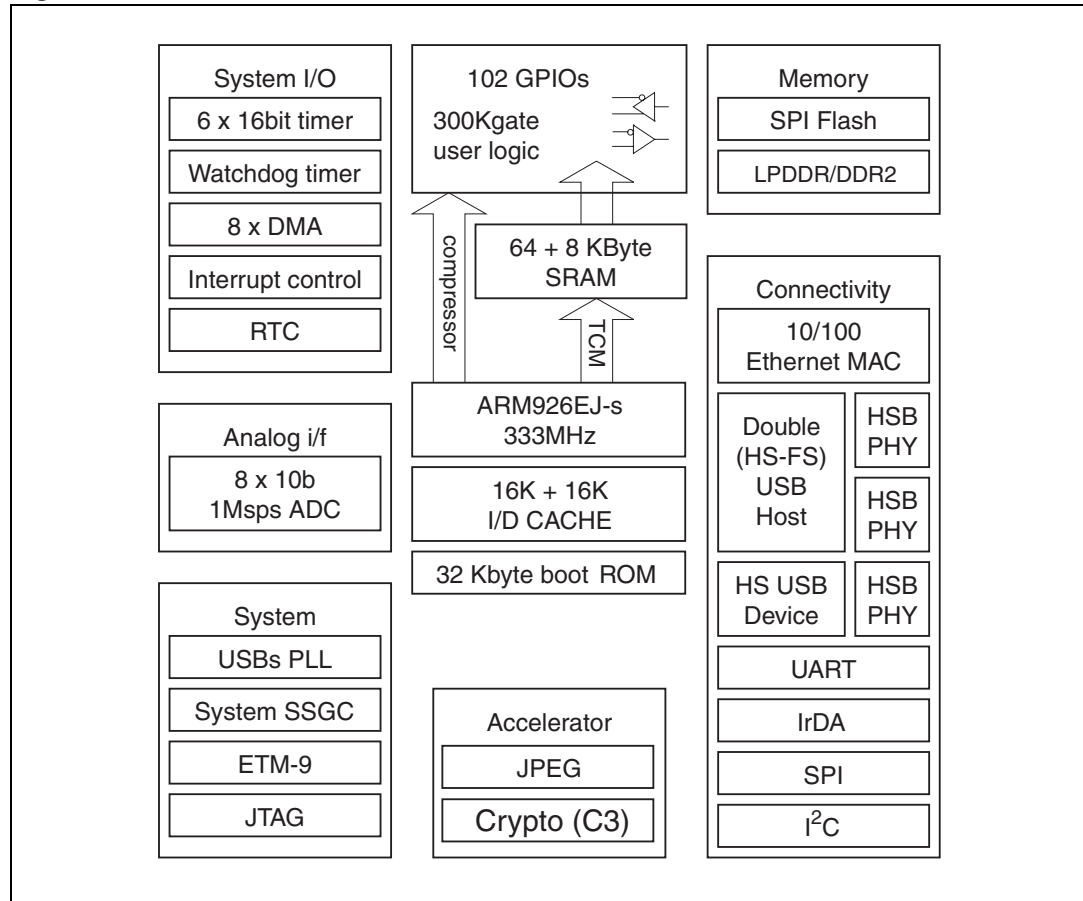
1 Reference documentation

1. ARM926EJ-S - technical reference manual
2. AMBA 2.0 specification
3. EIA/JESD8-9 specification
4. EIA/JESD8-15 specification
5. USB2.0 specification
6. OHCI specification
7. EHCI specification
8. IRPHY version1.3
9. IRLAP version 1.1
10. IEEE 1149.1
11. IEEE 802.3 – 2002
12. I²C - bus specification version 2.1

2 Product overview

An outline diagram of the main SPEAr BASIC functional interfaces is shown in [Figure 1](#).

Figure 1. SPEAr BASIC functional interfaces



3 Features

The main functionalities implemented in the SPEAr BASIC SoC device are as follows:

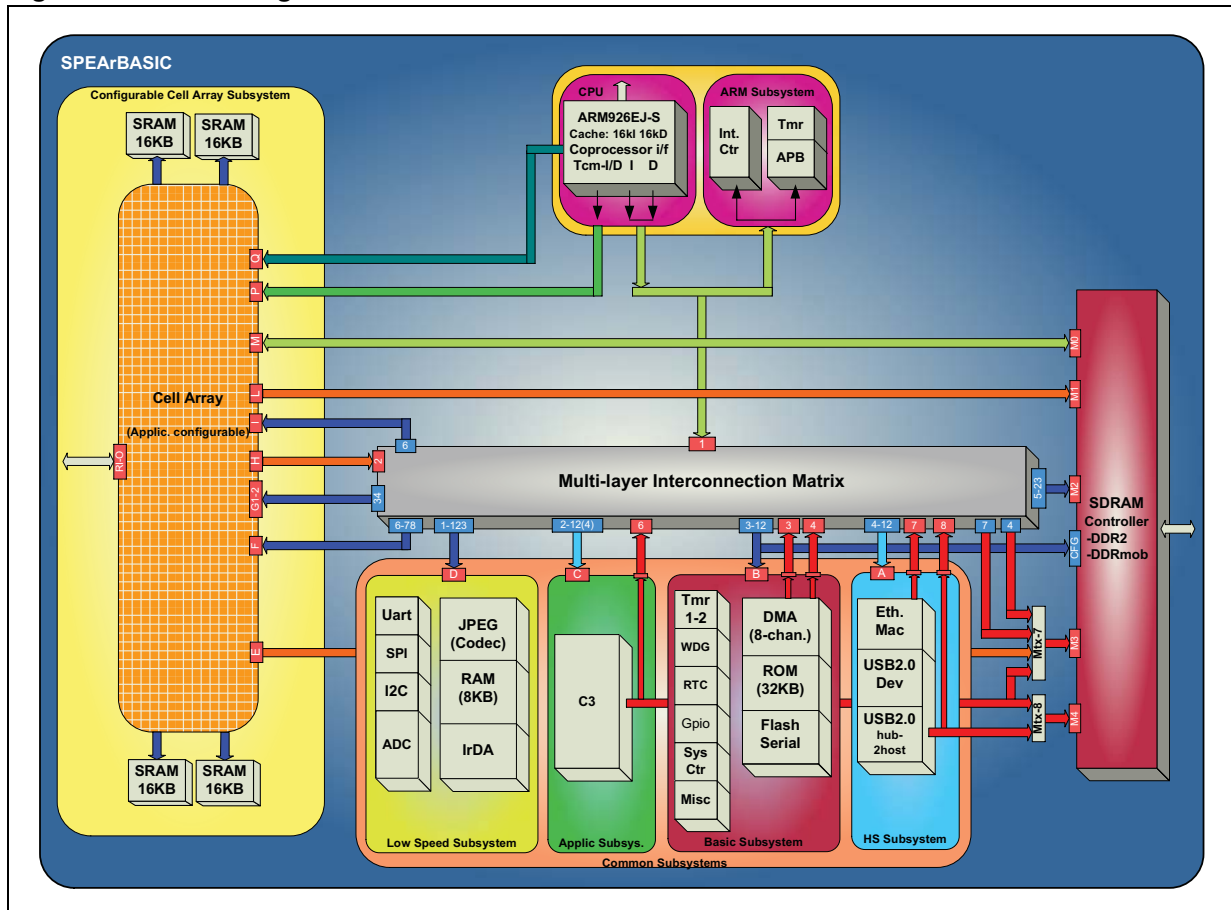
- ARM926EJ-S core @333 MHz, 16+16 KB-I/D cache, configurable TMC-I/D size, MMU, TLB, JTAG and ETM trace module (multiplexed interfaces)
- 300 KGate reconfigurable logic array (100% utilization rate, 4 metal and 4 vias masks)
- 64 + 8 Kbyte configurable internal memory pool (single and dual memory port)
- 32 Kbyte boot ROM (code customizable)
- Dynamic power save features
- High performance linked list 8 channels DMA
- Ethernet MAC 10/100 Mbps (MII PHY interface)
- USB2.0 device (high-full speed), integrated PHY transceiver
- 2 USB2.0 host (high-full-low speed), integrated PHY transceiver
- External memory interface: 8/16-bit mobile LPDDR@166 MHz/DDR2@333 MHz
- Flash interface: SPI serial (up to 50 Mbps)
- SPI master/slave (Motorola, Texas instruments, National semiconductor) up to 50 Mbps
- I2C (high-fast-slow speed) master/slave
- UART (speed rate up to 460.8 Kbps)
- IrDA (FIR/MIR/SIR) 9.6 Kbps to 4 Mbps speed-rate
- 6 legacy GPIOs bidirectional signals with interrupt capability
- 102 RAS GPIOs. (User customizable bidirectional signals with no clock domain limitations)
- ADC (1 μ s/1Msps) with 8 analog input channels, 10-bit approximation (supporting up to 13.5 bits at 8 KSPS by oversampling and accumulation)
- JPEG codec accelerator 1clock/pixel
- ST C3 (channel controller co-processor) flexible engine is a configurable array of Macro-Functions (channels) controlled by instruction dispatchers allowing symmetric or public key cryptography
- 3 pairs of 16-bits general purpose timers with programmable prescaler
- RTC – WDOG – SYSCTR – MISC internal control registers
- JTAG (IEEE1149.1) interface
- ETM9 interface and EmbeddedICE-RT

4 Architecture properties

- Power save features:
 - Operating frequency SW programmable
 - Clock gating functionality
 - Low frequency operating mode
 - Automatic power saving controlled from application activity demands
- Customizable logic to embed the customer's application:
 - 300 Kgate standard cell array
 - Internal memory pool (64 + 8 Kbyte) fully configurable
 - Up to 10 internal source clocks (some of these are programmable)
 - No clock domain limits (every PL_GPIO can clock the customizable logic)
 - Three memory paths toward the DRAM controller to ensure for optimal bandwidth
- Easily extendable architecture
- External memory bandwidth of each master tuneable to meet the target performance of different applications

5 Block diagram

Figure 2. Block diagram



5.1 Core architecture

The SoC internal architecture is based on several shared subsystem logic blocks interconnected through a multilayer interconnection matrix as detailed in [Figure 2](#).

The switch matrix structure allows different subsystem dataflows to be executed in parallel improving the core platform efficiency.

High performance master agents are directly interconnected with the memory controller reducing the memory access latency. Three different memory paths (two of them shared with other masters) are reserved for the programmable logic to enhance the user application throughput. The overall memory bandwidth assigned to each master port can be programmed and optimized through an internal efficient weighted round-robin arbitration mechanism.

The internal memory pool is completely configurable to improve the performance of the user application custom logic.

6 Pins description

6.1 Functional pin group

[Table 1](#) shows the pin list with functional pins grouped by IP, and power pins (including grounds) grouped separately. Please refer also to [Section 11](#).

Table 1. Pin description by functional group

Group	Signal name	Ball	Direction	Function	Pin type
ADC	AIN_0	N16	Input	ADC analog input channel	Analog buffer 2.5V tolerant
	AIN_1	N15			
	AIN_2	P17			
	AIN_3	P16			
	AIN_4	P15			
	AIN_5	R17			
	AIN_6	R16			
	AIN_7	R15			
	ADC_VREFN	N14		ADC negative voltage reference	
ADC_VREFP	P14	ADC positive voltage reference			
DEBUG	TEST_0	K16	Input	Test configuration ports. For functional mode they must be set to zero.	TTL input buffer, 3.3 V tolerant, PD
	TEST_1	K15			
	TEST_2	K14			
	TEST_3	K13			
	TEST_4	J15			
	BOOT_SEL	J14			
	nTRST	L16	Input	Test reset input	TTL Schmitt trigger input buffer, 3.3 V tolerant, PU
	TDO	L15	Output	Test data output	TTL output buffer, 3.3 V capable, 4 mA
	TCK	L17	Input	Test clock	TTL Schmitt trigger input buffer, 3.3 V tolerant, PU
	TDI	L14	Input	Test data input	
	TMS	L13	Input	Test mode select	
PL_I/O	PL_GPIO_0	F3	I/O	Shared I/O	TTL BIDIR buffer, 3.3 V capable, 4mA 3.3 V tolerant, PU
	PL_GPIO_1	E3			
	PL_GPIO_2	E4			
	PL_GPIO_3	D1			

Table 1. Pin description by functional group (continued)

Group	Signal name	Ball	Direction	Function	Pin type
	PL_GPIO_4	C1			
	PL_GPIO_5	D2			
	PL_GPIO_6	B1			
	PL_GPIO_7	D3			
	PL_GPIO_8	C2			
	PL_GPIO_9	B2			
	PL_GPIO_10	C3			
	PL_GPIO_11	E5			
	PL_GPIO_12	D4			
	PL_GPIO_13	A1			
	PL_GPIO_14	A2			
	PL_GPIO_15	B3			
	PL_GPIO_16	E6			
	PL_GPIO_17	C4			
	PL_GPIO_18	D5			
	PL_GPIO_19	A3			
	PL_GPIO_20	B4			
	PL_GPIO_21	C5			
	PL_GPIO_22	D6			
	PL_GPIO_23	A4			
	PL_GPIO_24	B5			
	PL_GPIO_25	C6			
	PL_GPIO_26	A5			
	PL_GPIO_27	B6			
	PL_GPIO_28	A6			
	PL_GPIO_29	A7			
	PL_GPIO_30	B7			
	PL_GPIO_31	C7			
PL_I/O	PL_GPIO_32	D7	I/O	Shared I/O	TTL BIDIR buffer, 3.3 V capable, 4mA 3.3 V tolerant, PU
	PL_GPIO_33	E7			
	PL_GPIO_34	E8			
	PL_GPIO_35	D8			
	PL_GPIO_36	C8			
	PL_GPIO_37	B8			
	PL_GPIO_38	A8			

Pins description

SPEAR-09-B042

Table 1. Pin description by functional group (continued)

Group	Signal name	Ball	Direction	Function	Pin type
	PL_GPIO_39	A9			
	PL_GPIO_40	B9			
	PL_GPIO_41	C9			
	PL_GPIO_42	D9			
	PL_GPIO_43	E9			
	PL_GPIO_44	A10			
	PL_GPIO_45	B10			
	PL_GPIO_46	A11			
	PL_GPIO_47	C10			
	PL_GPIO_48	B11			
	PL_GPIO_49	C11			
	PL_GPIO_50	A12			
	PL_GPIO_51	D10			
	PL_GPIO_52	B12			
	PL_GPIO_53	D11			
	PL_GPIO_54	E10			
	PL_GPIO_55	A13			
	PL_GPIO_56	C12			
	PL_GPIO_57	E11			
	PL_GPIO_58	D12			
	PL_GPIO_59	B13			
	PL_GPIO_60	A14			
	PL_GPIO_61	E12			
	PL_GPIO_62	A15			
	PL_GPIO_63	C13			
	PL_GPIO_64	D13			
	PL_GPIO_65	B14			
	PL_GPIO_66	E13			
	PL_GPIO_67	C14			
	PL_GPIO_68	B15			
	PL_GPIO_69	A16			
	PL_GPIO_70	C15			
	PL_GPIO_71	D14			
	PL_GPIO_72	B16			
	PL_GPIO_73	A17			

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Table 1. Pin description by functional group (continued)

Group	Signal name	Ball	Direction	Function	Pin type
	PL_GPIO_74	C16			
	PL_GPIO_75	E14			
	PL_GPIO_76	F13			
	PL_GPIO_77	B17			
	PL_GPIO_78	D15			
	PL_GPIO_79	F14			
	PL_GPIO_80	D16			
	PL_GPIO_81	C17			
	PL_GPIO_82	E15			
	PL_GPIO_83	E16			
	PL_GPIO_84	D17			
	PL_GPIO_85	F15			
	PL_GPIO_86	E17			
	PL_GPIO_87	G13			
	PL_GPIO_88	F16			
	PL_GPIO_89	F17			
	PL_GPIO_90	G14			
	PL_GPIO_91	G15			
	PL_GPIO_92	G16			
	PL_GPIO_93	G17			
	PL_GPIO_94	H13			
	PL_GPIO_95	H14			
	PL_GPIO_96	H15			
	PL_GPIO_97	H16			
PL_CLK	PL_CLK_1	K17	I/O	Shared external clock	TTL BIDIR buffer, 3.3 V capable, 8mA 3.3 V tolerant, PU
	PL_CLK_2	J17			
	PL_CLK_3	J16			
	PL_CLK_4	H17			
DDR I/F	DDR_ADD_0	T2	Output	Address line	SSTL_2/SSTL_18
	DDR_ADD_1	T1			
	DDR_ADD_2	U1			
	DDR_ADD_3	U2			
	DDR_ADD_4	U3			
	DDR_ADD_5	U4			
	DDR_ADD_6	U5			

Pins description

SPEAR-09-B042

Table 1. Pin description by functional group (continued)

Group	Signal name	Ball	Direction	Function	Pin type
	DDR_ADD_7	T5			
	DDR_ADD_8	R5			
	DDR_ADD_9	P5			
	DDR_ADD_10	P6			
	DDR_ADD_11	R6			
	DDR_ADD_12	T6			
	DDR_ADD_13	U6			
	DDR_ADD_14	R7			
	DDR_BA_0	P7	Output	Bank select	SSTL_2/SSTL_18
	DDR_BA_1	P8			
	DDR_BA_2	R8			
	DDR_RAS	U8	Output	Row add. strobe	SSTL_2/SSTL_18
	DDR_CAS	T8	Output	Col. add. strobe	SSTL_2/SSTL_18
	DDR_WE	T7	Output	Write enable	SSTL_2/SSTL_18
	DDR_CLKEN	U7	Output	Clock enable	SSTL_2/SSTL_18
	DDR_CLK_P	T9	Output	Differential clock	Differential SSTL_2/SSTL_18
	DDR_CLK_N	U9			
	DDR_CS_0	P9	Output	Chip select	SSTL_2/SSTL_18
	DDR_CS_1	R9			
	DDR_ODT_0	T3	I/O	On-die termination enable lines	SSTL_2/SSTL_18
	DDR_ODT_1	T4			
	DDR_DATA_0	P11	I/O	Data lines (lower byte)	SSTL_2/SSTL_18
	DDR_DATA_1	R11			
	DDR_DATA_2	T11			
	DDR_DATA_3	U11			
	DDR_DATA_4	T12			
	DDR_DATA_5	R12			
	DDR_DATA_6	P12			
	DDR_DATA_7	P13			
	DDR_DQS_0	U10	Output	Lower data strobe	Differential SSTL_2/SSTL_18
	DDR_nDQS_0	T10			
	DDR_DM_0	U12	Output	Lower data mask	SSTL_2/SSTL_18
	DDR_GATE_0	R10	I/O	Lower gate open	SSTL_2/SSTL_18
	DDR_DATA_8	T17	I/O	Data lines (upper byte)	SSTL_2/SSTL_18

SPEAR-09-B042

Pins description

Table 1. Pin description by functional group (continued)

Group	Signal name	Ball	Direction	Function	Pin type
	DDR_DATA_9	T16			
	DDR_DATA_10	U17			
	DDR_DATA_11	U16			
	DDR_DATA_12	U14			
	DDR_DATA_13	U13			
	DDR_DATA_14	T13			
	DDR_DATA_15	R13			
	DDR_DQS_1	U15	I/O	Upper data strobe	Differential SSTL_2/SSTL_18
	DDR_nDQS_1	T15			
	DDR_DM_1	T14	I/O	Upper data mask	SSTL_2/SSTL_18
	DDR_GATE_1	R14	I/O	Upper gate open	SSTL_2/SSTL_18
	DDR_VREF	P10	Input	Reference voltage	Analog
	DDR_COMP_GND	R4	Power	Return for external resistors	Power
	DDR_COMP_1V8	P4	Power	External resistor 1.8V	Analog
	DDR2_EN	J13	Input	Configuration	TTL input buffer 3.3 V tolerant, PU
USB	DEV_DP	M1	I/O	USB device D+	Bidirectional analog buffer 5V tolerant
	DEV_DM	M2		USB device D-	
	DEV_VBUS	G3	Input	USB device VBUS	TTL Input buffer 3.3 V tolerant, PD
	HOST1_DP	H1	I/O	USB HOST1 D+	Bidirectional analog buffer 5V tolerant
	HOST1_DM	H2		USB HOST1 D-	
	HOST1_VBUS	H3	Output	USB HOST1 VBUS	TTL output buffer 3.3 V capable, 4mA
	HOST1_OVRC	J4	Input	USB host1 over-current	TTL input buffer 3.3 V tolerant, PD
	HOST0_DP	K1	I/O	USB HOST0 D+	Bidirectional analog buffer 5v tolerant
	HOST0_DM	K2		USB HOST0 D-	
	HOST0_VBUS	J3	Output	USB HOST0 VBUS	TTL Output Buffer 3.3 V capable, 4mA
	HOST0_OVRC	H4	Input	USB host0 over-current	TTL input buffer 3.3 V tolerant, PD
	USB_TXRTUNE	K5	Output	Reference resistor	Analog
	USB_ANALOG_TEST	L4	Output	Analog test output	Analog
Master Clock	MCLK_XI	P1	Input	24 MHz crystal I	Oscillator 2.5V capable
	MCLK_XO	P2	Output	24 MHz crystal O	

Pins description

SPEAR-09-B042

Table 1. Pin description by functional group (continued)

Group	Signal name	Ball	Direction	Function	Pin type
RTC	RTC_XI	E2	Input	32KHz crystal I	Oscillator 1V capable
	RTC_XO	E1	Output	32 KHz crystal O	
SMI	SMI_DATAIN	M13	I/O	Serial Flash input data	TTL input buffer 3.3 V tolerant, PU
	SMI_DATAOUT	M14	I/O	Serial Flash output data	TTL output buffer 3.3 V capable, 4mA
	SMI_CLK	N17	I/O	Serial Flash clock	
	SMI_CS_0	M15	Output	Serial Flash chip select	
	SMI_CS_1	M16			
Reset	MRESET	M17	Input	Main reset	TTL Schmitt trigger input buffer, 3.3 V tolerant, PU
3.3 V Compens.	DIGITAL_REXT	G4	Output	Configuration	Analog, 3.3 V capable
	DIGITAL_GND_REXT	F4	Power	Power	Power

Note: PU means Pull Up and PD means pull down

Table 2. Power supply

Signal name	Ball	Value
GND	G6 G7 G8 G9 G10 G11 H6 H7 H8 H9 H10 H11 J6 J7 J8 J9 J10 J11 K6 K7 K8 K9 K10 K11 L6 L7 L8 L9 L10 M8 M9 M10	0 V
AGND	F2, G1, J2, L1, L3, L5, N2, N4, P3, R3	0 V
VDD3	F5 F6 F7 F10 F11 F12 G5 J12 K12 L12 M12	3.3 V
VDD	F8 F9 G12 H5 H12 J5 L11 M6 M7 M11	1.2 V
HOST0_VDDbc	L2	2.5 V
HOST0_VDDb3	K4	3.3 V
HOST1_VDDbc	K3	2.5 V
HOST1_VDDb3	J1	3.3 V
DEVICE_VDDbc	N1	2.5 V
USB_VDDbs	M3	1.2 V
DEVICE_VDDb3	N3	3.3 V
MCLK_VDD	R1	1.2 V
MCLK_VDD2v5	R2	2.5 V
DITH1_AVDD	G2	2.5 V
SSTL_VDDe	M5 N5 N6 N7 N8 N9 N10 N11	1.8 V
ADC_AGND	N12	0V
ADC_AVDD	N13	2.5 V
DITH2_AVDD	M4	2.5 V
RTC_VDD	F1	1.5 V

6.2 Special I/Os

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6.2.1 USB 2.0 transceiver

SPEAR BASIC has three USB 2.0 transceivers. One transceiver is used by the USB device controller, and two are used by the hosts. The transceivers are all integrated into a single USB three-PHY macro.

6.2.2 SSTL_2/SSTL_18

Fully compliant with JEDEC specification with programmable integrated terminations.

7 Memory map

Table 3. Main memory map

Start address	End address	Peripheral	Notes
0x0000.0000	0x3FFF.FFFF	External DRAM	Low power DDR or DDR2
0x4000.0000	0xBFFF.FFFF	RAS_M	Customizable logic array
0xC000.0000	0xCFFF.FFFF	-	Reserved
0xD000.0000	0xD7FF.FFFF	ICM1	Low speed connection
0xD800.0000	0xDFFF.FFFF	-	Reserved
0xE000.0000	0xE7FF.FFFF	ICM4	High speed connection
0xE800.0000	0xEFFF.FFFF	-	Reserved
0xF000.0000	0xF7FF.FFFF	ML1	Multi layer CPU subsystem
0xF800.0000	0xFFFF.FFFF	ICM3	Basic subsystem

Table 4. ICM1 – Low speed connection

Start address	End address	Peripheral	Notes	Bus
0xD000.0000	0xD007.FFFF	UART		APB
0xD008.0000	0xD00F.FFFF	ADC		APB
0xD010.0000	0xD017.FFFF	SPI		APB
0xD018.0000	0xD01F.FFFF	I2C		APB
0xD020.0000	0xD07F.FFFF	-	Reserved	APB
0xD080.0000	0xD0FF.FFFF	JPEG codec		AHB
0xD100.0000	0xD17F.FFFF	IrDA		AHB
0xD180.0000	0xD1FF.FFFF	-	Reserved	AHB
0xD280.0000	0xD2FF.FFFF	SRAM	Static RAM shared memory (8 Kbyte)	AHB
0xD300.0000	0xD7FF.FFFF	-	Reserved	AHB

Table 5. ICM4 – High speed connection

Start address	End address	Peripheral	Notes	Bus
0xE000.0000	0xE07F.FFFF	-	Reserved	APB
0xE080.0000	0xE0FF.FFFF	Ethernet ctrl	MAC	AHB
0xE100.0000	0xE10F.FFFF	USB2.0 device	FIFO	AHB
0xE110.0000	0xE11F.FFFF	USB2.0 device	Configuration registers	AHB
0xE120.0000	0xE12F.FFFF	USB2.0 device	Plug detect	AHB
0xE130.0000	0xE17F.FFFF	-	Reserved	AHB
0xE180.0000	0xE18F.FFFF	USB2.0 EHCI 0-1		AHB
0xE190.0000	0xE19F.FFFF	USB2.0 OHCI 0		AHB
0xE1A0.0000	0xE20F.FFFF	-	Reserved	AHB
0xE210.0000	0xE21F.FFFF	USB2.0 OHCI 1		AHB
0xE220.0000	0xE2FF.FFFF	-	Reserved	AHB
0xE280.0000	0xE280.FFFF	ML USB ARB	Configuration register	AHB
0xE290.0000	0xE7FF.FFFF	-	Reserved	AHB

Table 6. ML1 – Multi layer CPU subsystem

Start address	End address	Peripheral	Notes	Bus
0xF000.0000	0xF00F.FFFF	Timer		APB
0xF010.0000	0xF0FF.FFFF	-	Reserved	APB
0xF100.0000	0xF10F.FFFF	-	Reserved	AHB
0xF110.0000	0xF11F.FFFF	ITC Primary		AHB
0xF120.0000	0xF7FF.FFFF	-	Reserved	AHB

Table 7. ICM3 – Basic subsystem

Start address	End address	Peripheral	Notes	Bus
0xF800.0000	0xFBFF.FFFF	Serial Flash memory		AHB
0xFC00.0000	0xFC1F.FFFF	Serial Flash controller		AHB
0xFC20.0000	0xFC3F.FFFF	Reserved		AHB
0xFC40.0000	0xFC5F.FFFF	DMA controller		AHB
0xFC60.0000	0xFC7F.FFFF	DRAM controller		AHB
0xFC80.0000	0xFC87.FFFF	Timer 1		APB
0xFC88.0000	0xFC8F.FFFF	Watch dog timer		APB
0xFC90.0000	0xFC97.FFFF	Real-time clock		APB
0xFC98.0000	0xFC9F.FFFF	General purpose I/O		APB
0xFCA0.0000	0xFCA7.FFFF	System controller		APB
0xFCA8.0000	0xFCAF.FFFF	Miscellaneous registers		APB
0xFCB0.0000	0xFCB7.FFFF	Timer 2		APB
0xFCB8.0000	0xFCFF.FFFF	-	Reserved	APB
0xFDB8.0000	0xFEFF.FFFF	-	Reserved	AHB
0xFF00.0000	0xFFFF.FFFF	Internal ROM	Boot	AHB

8 Main blocks

8.1 CPU subsystem

8.1.1 Overview

The CPU sub-system includes the following blocks:

- ARM 926EJS
- Two timer channels
- Interrupt controller (32 IRQ lines)

8.1.2 CPU ARM 926EJ-S

The ARM926EJ-S processor is used, which is targeted for multi-tasking applications.

Belonging to ARM9 family of general-purpose microprocessors, it contains a memory management unit, which provides virtual memory features, making it compliant with WindowsCE, Linux and SymbianOS operating systems.

The ARM926EJ-S supports the 32-bit ARM and 16-bit Thumb instruction sets, enabling the user to trade off between high performance and high code density and includes features for efficient execution of Java byte codes.

It also uses the ARM debug architecture and includes logic to assist in software debug.

Its main features are:

- CORE f_{MAX} 333 MHz independent programmable for each CPU
- Memory management unit
- 16 Kbyte of instruction CACHE
- 16 Kbyte of data CACHE
- Configurable tightly coupled memory (I/D) size through the configurable logic array
- ARM-V5TEJ instructions set architecture:
 - ARM (32-bit), Thumb® (16-bit)
 - DSP extensions
 - JAVA™ (8-bit) instructions
- AMBA bus interface
- Embedded ICE-RT
- ETM9 (embedded trace macro-cell)

8.2 Clock and reset system

The clock system is a fully programmable block that generates all the clocks necessary to the chip.

The default operating clock frequencies are:

- Clock @ 333 MHz for the CPU. (*Note 1*)
- Clock @ 166 MHz for AHB bus and AHB peripherals. (*Note 1*)
- Clock @ 83 MHz for, APB bus and APB peripherals. (*Note 1*)
- Clock @ 333 MHz for DDR memory interface. (*Note 2*)

The default values give the maximum allowed clock frequencies. The user can modify the clock frequencies by programming dedicated registers.

The clock system consists of 2 main parts: a multiclock generator block and two internal PLLs.

The multiclock generator block, takes a reference signal (which is usually delivered by the PLL), generates all clocks for the IPs of SPEAr BASIC according to dedicated programmable registers.

Each PLL, uses an oscillator input of 24 MHz, to generate a clock signal at a frequency corresponding at the highest of the group. This is the reference signal used by the multiclock generator block to obtain all the other requested clocks for the group. Its main feature is electromagnetic interference reduction capability. The user can set up the PLL has a to modulate the VCO with a triangular wave. The resulting signal has a spectrum (and power) spread over a small programmable range of frequencies centered on F0 (the VCO frequency), obtaining minimum electromagnetic emissions. This method replaces all the other traditional methods of E.M.I. reduction, such as filtering, ferrite beads, chokes, adding power layers and ground planes to PCBs, metal shielding and so on. This gives the customer appreciable cost savings.

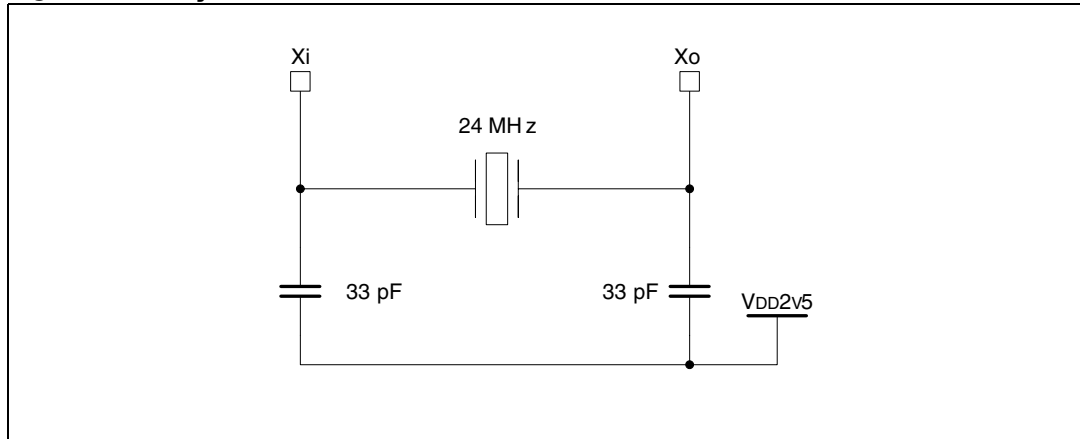
In sleep mode the SoC runs with the PLL disabled so the available frequency is 24 MHz or a sub-multiple (/2, /4, /8).

- Note:*
- 1 This frequency is based on the PLL1.
 - 2 This frequency is based on the PLL2.

8.3 Main oscillator

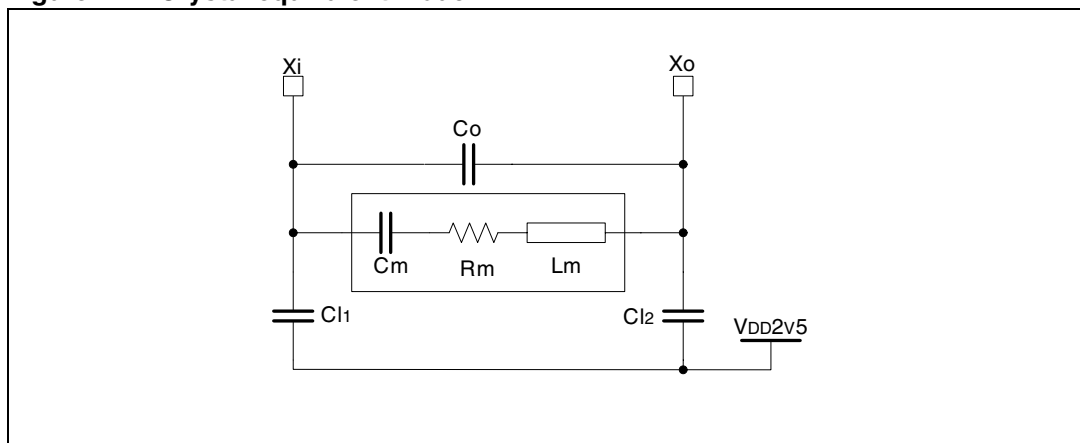
8.3.1 Crystal connection

Figure 3. Crystal connection



8.3.2 Crystal equivalent model

Figure 4. Crystal equivalent model



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Note: C_o is the parasitic capacitance of the crystal package
 C_{l1} and C_{l2} are the capacitance on each resonator PAD

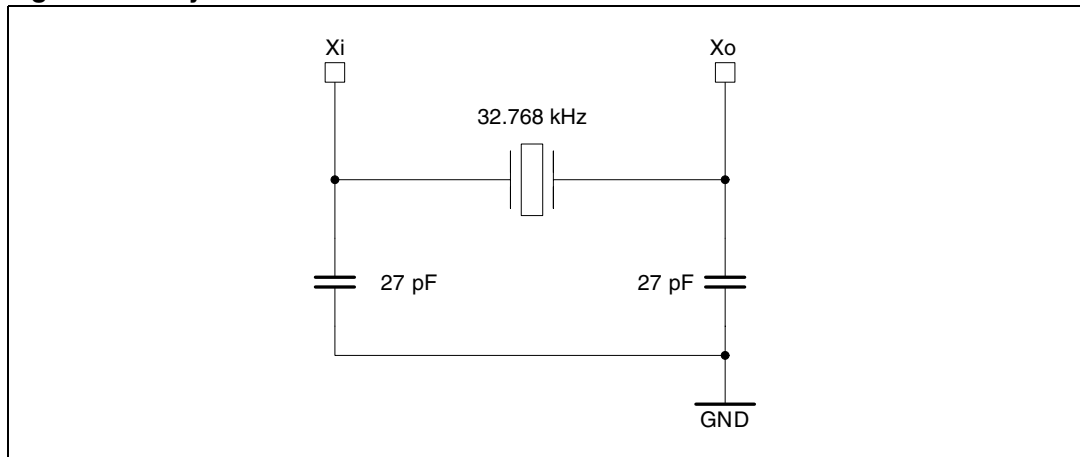
Table 8. Equivalent values

Supplier	Rm (Ohms)	Lm (mH)	Cm (fF)	Co (pF)	Q (K)
Epson (E31821)	9.3	5.9	4.8	1.7	120
Raltron (M3000)	9.6	2.6	10.8	3.5	45
KSS (KSS3KF)	5	3.2	8.7	2.7	121

8.4 RTC oscillator

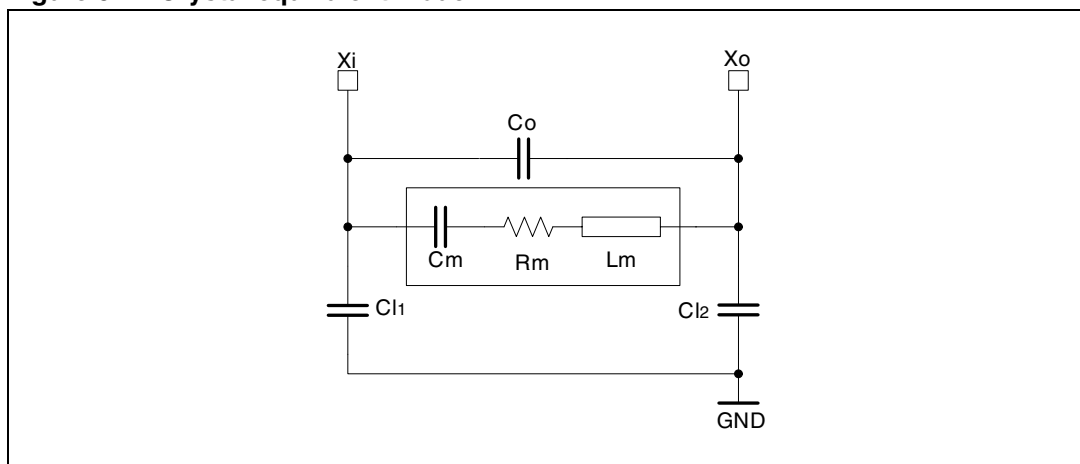
8.4.1 Crystal connection

Figure 5. Crystal connection



8.4.2 Crystal equivalent model

Figure 6. Crystal equivalent model



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Note: C_o is the parasitic capacitance of the crystal package
 C_{l1} and C_{l2} are the capacitance on each resonator PAD

Table 9. Equivalent values

Supplier	R_m (KOhms)	L_m (mH)	C_m (fF)	C_o (pF)
Ecliptek	<65	10	1.9	0.85

8.5 Ethernet controller

The Ethernet MAC controller provides the following features:

- Compliant with the IEEE 802.3-2002 standard
- MII interface to the external PHY
- Supports 10/100 Mbps data transfer rates
- Local FIFO available (4 Kbyte RX, 2 Kbyte TX)
- Supports both half-duplex and full-duplex operation. In half-duplex operation, CSMA/CD protocol is provided for, as well as packet bursting and frame extension at 100 Mbps
- Programmable frame length to support both standard and jumbo ethernet frames with size up to 16 Kbyte
- A variety of flexible addresses filtering modes are supported
- A set of control and status registers (CSRs) to control GMAC core operation
- Native DMA with single-channel transmit and receive engines, providing 32/64/128-bit data transfers
- DMA implements dual-buffer (ring) or linked-list (chained) descriptor chaining
- An AHB slave acting as programming interface to access all CSRs, for both DMA and GMAC core subsystems
- An AHB master for data transfer to system memory
- 32-bit AHB master bus width, supporting 32, 64, and 128-bit wide data transactions

8.6 USB2 host controller

SPEAR BASIC has two fully independent USB 2.0 hosts and each one is constituted with 5 major blocks:

- EHCI capable of managing high-speed transfers (HS mode, 480 Mbps)
- OHCI that manages the full and the low speed transfers (12 and 1.5 Mbps)
- Local 2-Kbyte FIFO
- Local DMA
- Integrated USB2 transceiver (PHY)

Both hosts can manage an external power switch, providing a control line to enable or disable the power, and an input line to sense any over-current condition detected by the external switch.

One host controller at time can perform high speed transfer.

8.7 USB2 device controller

The USB2 device controller provides the following features:

- Supports the 480 Mbps high-speed mode (HS) for USB 2.0, as well as the 12 Mbps full-speed (FS) and the low-speed (LS modes) for USB 1.1
- Supports 16 physical endpoints and configurations to achieve logical endpoints
- Integrated USB transceiver (PHY)
- Local FIFO having size of 4 Kbyte shared among all the endpoints
- DMA mode and slave-only mode are supported
- In DMA mode, the UDC supports descriptor-based memory structures in application memory
- In both modes, an AHB slave is provided by UDC-AHB, acting as programming interface to access to memory-mapped control and status registers (CSRs)
- An AHB master for data transfer to system memory is provided, supporting 8, 16, and 32-bit wide data transactions on the AHB bus
- A USB plug detect (UPD) which detects the connection of a cable

Table 10. Endpoint assignments

EP0	Control (IN/OUT).
EP1	Software configurable to: – Bulk in – Interrupt in – Isochronous
EP3	
EP5	
EP7	
EP9	
EP11	
EP13	
EP15	
EP2	
EP4	
EP6	
EP8	
EP10	
EP12	
EP14	

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8.8 32-Kbyte boot ROM

The code contained in this ROM is executed at the boot time. It initializes the system and can then boot from the serial Flash through the SMI or from the USB device interface. To use the latter possibility a suitable driver should be installed on the host platform.

8.9 Serial memory interface

The main features of SMI are listed below:

- supports the following SPI-compatible Flash and EEPROM devices:
 - STMicroelectronics M25Pxxx, M45Pxxx
 - STMicroelectronics M95xxx, except M95040, M95020 and M95010
 - ATMEL AT25Fxx
 - YMC Y25Fxx
 - SST SST25LFxx
- acts always as a SPI master and up to 2 SPI slave memory devices are supported (through as many chip select signals), with up to 16 MB address space each
- the SMI clock signal (*SMICLK*) is generated by SMI (and input to all slaves) using a clock provided by the AHB bus
- *SMICLK* can be up to 50 MHz in fast read mode (or 20 MHz in normal mode). It can be controlled by 7 programmable bits.

8.10 JPEG (codec)

The main features of the JPEG codec are:

- compliance with the baseline JPEG standard (ISO/IEC 10918-1)
- single-clock per pixel encoding/decoding
- support for up to four channels of component color
- 8-bit/channel pixel depths
- programmable quantization tables (up to four)
- programmable Huffman tables (two AC and two DC)
- programmable minimum coded unit (MCU)
- configurable JPEG headers processing
- support for restart marker insertion
- use of two DMA channels and of two 8 x 32-bits FIFO's (local to the JPEG) for efficient transferring and buffering of encoded/decoded data from/to the codec core.

8.11 Cryptographic co-processor (C3)

SPEAR BASIC has an hardware cryptographic co-processor with the following features:

- Supported cryptographic algorithms:
 - Advanced encryption standard (AES) cipher in ECB, CBC, CTR modes.
 - Data encryption standard (DES) cipher in ECB and CBC modes.
 - SHA-1, HMAC-SHA-1, MD5, HMAC-MD5 digests.
- Instruction driven DMA based programmable engine.
- AHB master port for data access from/to system memory.
- AHB slave port for co-processor register accesses and initial engine-setup.
- The co-processor is fully autonomous (DMA input reading, cryptographic operation execution, DMA output writing) after being set up by the host processor.
- The co-processor executes programs written by the host in memory, it can execute an unlimited list of programs.
- The co-processor supports hardware chaining of cryptographic blocks for optimized execution of data-flow requiring multiple algorithms processing over the same set of data (for example encryption + hashing on the fly).

8.12 Low jitter PLL

Within the USB Hosts and device a local low jitter PLL is provided to meet the USB2.0 specification requirements.

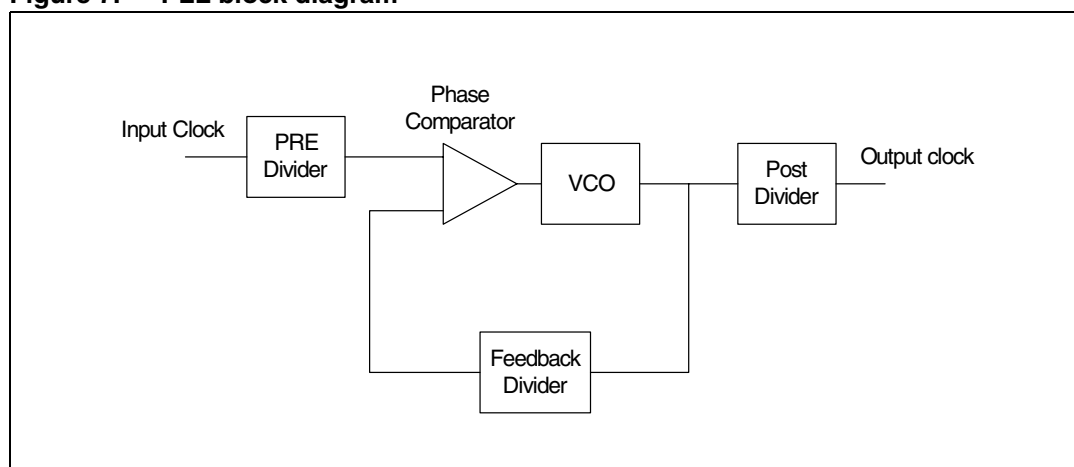
8.13 Main PLL

Two PLLs are provided so that the external memory bus can run at a different frequency to the internal AHB. To reduce the system emission both the PLL are offering four operational modes:

- Normal mode
- Fractional mode
- Double side dithering mode
- Single side dithering mode

8.13.1 PLL block diagram

Figure 7. PLL block diagram



8.13.2 Normal mode

In this mode, an 8-bit feedback divider is used. The PLL output frequency is always a multiple of the input frequency.

8.13.3 Fractional mode

In this mode, a 16-bit feedback divider and a more sophisticated control logic is used. The output frequency can have any value.

8.13.4 Double side dithering mode

This mode is based on the fractional mode. Frequency modulation (triangular shape) is applied to reduce the EMI. For example, if the fundamental frequency is 300 MHz and the modulation is set to 5% the output frequency varies from 285 MHz to 315 MHz.

8.13.5 Single side dithering mode

This mode is similar to the double side dithering mode, but it takes the fundamental frequency as the maximum value allowing a simplified calculation of all the system frequencies (DDR timing). For example, setting the fundamental frequency to 300 MHz and the modulation set to 5%, the output frequency varies from 270 MHz to 300 MHz.

8.14 ADC controller

The ADC controller provides the following features:

- Successive approximation ADC
- 10-bit resolution @ 1 Msps
- Hardware supporting up to 13.5 bits resolution at 8 KSPS by oversampling and accumulation
- Eight analog input (AIN) channels, ranging from 0 to 2.5 V
- $INL \pm 1$ LSB, $DNL \pm 1$ LSB
- Programmable conversion speed, (min. conversion time is 1 μ s)
- Programmable average results from 1 (No average) up to 128
- Programmable auto scan for all the eight channels.

8.15 UART

One SW flow control UART (one of these having IrDA features)

- Separate 16x8 (16 location deep x 8-bit wide) transmit and 16x12 receive FIFOs to reduce CPU interrupts
- Speed up to 460.8 Kbps.

8.16 IrDA

IrDA compliant serial link (FIR/MIR/SIR) from 9.6Kbps to 4 Mbps speed-rate.

8.17 SPI

An SPI interface is provided. The main features are:

- Maximum speed of 50 Mbps
- Programmable choice of interface operation:
 - SPI,
 - Microwire
 - TI synchronous serial
- Programmable data frame size from 4 to 16-bit.
- Master and slave mode capability.
- A connection to general purpose DMA is provided to reduce the CPU load.

8.18 I²C

An I²C interface is provided. The main features are:

- I²C v2.0 compatible.
- Supports three modes:
 - Standard (100 Kbps)
 - Fast (400 Kbps)
 - High-speed (3.4 Mbps)
- Master and slave mode configuration possible.
- Bulk data transfer capability.
- Connection with general purpose DMA is provided to reduce the CPU load.

8.19 DDR memory controller

SPEAr BASIC-STD integrates a high performance multi-channel memory controller that supports low power DDR and DDR2 double data rate memory devices. The multi-port architecture ensures that memory is shared efficiently among different high-bandwidth client modules.

8.20 Reconfigurable logic array

8.20.1 Overview

The configurable logic array consists of an embedded macro where a custom project can be implemented by mapping up to 300 K equivalent gates.

This macro is interfaced with the rest of the system by some AHB bus, some memory channels and it has a direct connection to the ARM processor internal bus. In this way is also possible to customize the TCM memory or add a coprocessor using this macro.

[Table 11](#) shows the memory cuts are available to this block:

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Table 11. Reconfigurable logic array interfaces

Instances	Type	Word	Bit	Notes
1	dual port	2048	32	One port hard-wired to the AMBA bus for NAND boot phase
2	dual port	96	128	Typically used for hardware accelerators
8	dual port	128	8	Typically used for hardware accelerators
2	dual port	2048	32	Generic dual port memory cuts
4	dual port	1024	32	Generic dual port memory cuts
8	dual port	2048	8	Generic dual port memory cuts
2	dual port	1024	32	Generic dual port memory cuts
4	single port	512	32	Generic single port memory cuts

The array is also connected to 102 I/O (3.3 V capable/tolerant and 4 mA sink/source).

The following clocks can be used in the integrated logic:

- Up to 5 external clocks provided through the device pins
- 4 separate clocks from the integrated frequency synthesizer
- PLL1 frequency
- PLL2 frequency
- 48 MHz (USB PLL)
- 24 MHz (Main oscillator)
- 32.768 KHz (RTC oscillator)
- APB clock (programmable)
- AHB clock (programmable)
- Any of the GPIOs

8.20.2 Custom project development

The flow to develop a custom project to embed in the SPEAr BASIC device is similar to the standard ASIC flow.

The configurable logic is an empty module of the whole system-on-chip. The pinout and the maximum number of gates are fixed. The HDL project is synthesized using a dedicated library and post synthesis simulation is possible to verify the custom net-list.

The verification procedure, after place and route phase, is the same as standard ASIC back end flow.

8.20.3 Customization process

The layers used for the IP configuration range from 2 metal layers with 1 via, up to 4 metal layers with 4 vias. Diffusion and remaining metal/vias are invariant across multiple custom designs. Density and performance scale with the number of customization layers.

The configurable logic included in the SPEAr BASIC chip is a 300 Kgate equivalent array when customized using 4 metals – 4 vias.

9 Standard customization

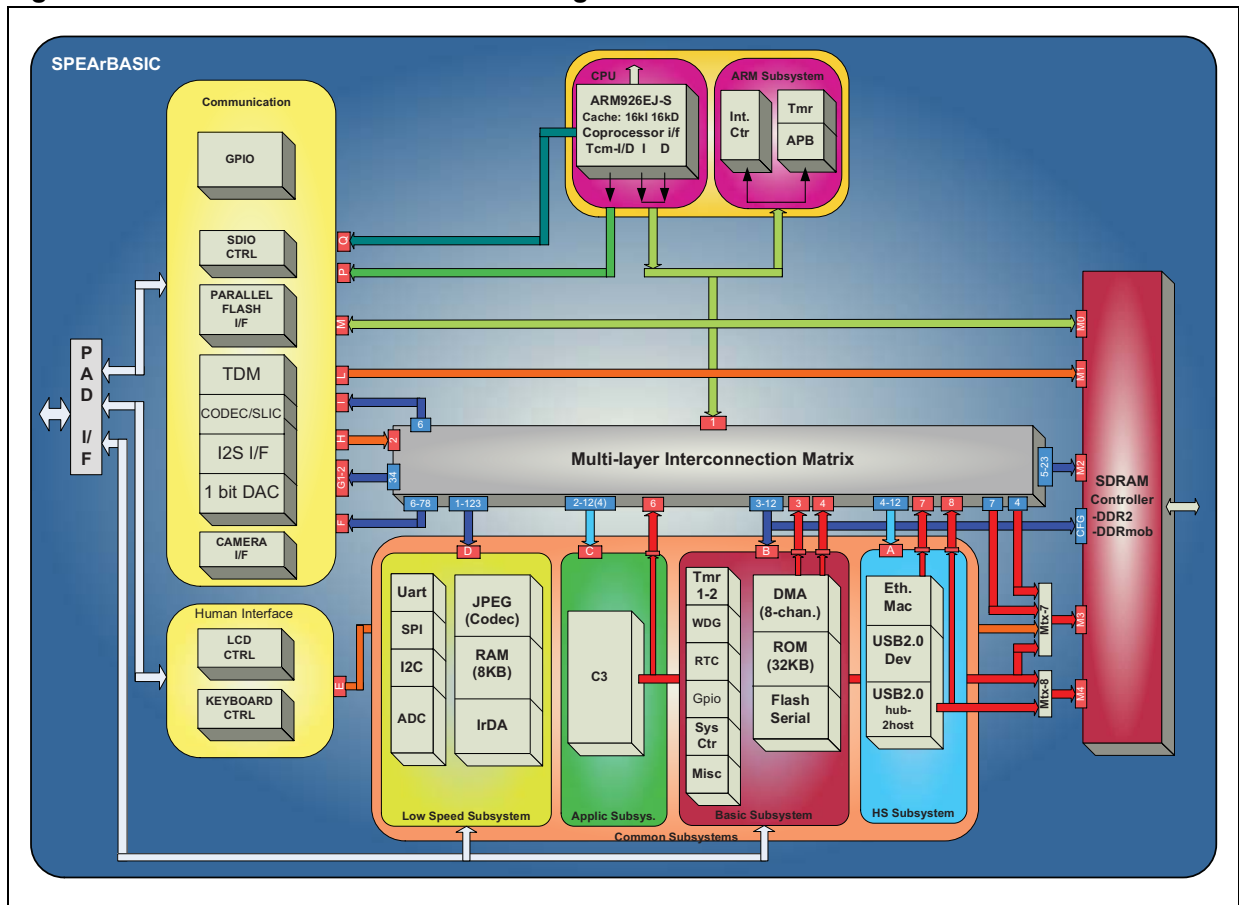
9.1 Features

The following functionalities are implemented in the SPEAr BASIC standard customization:

- 8/16-bits parallel Flash interface allowing connection of NOR or NAND Flash
- Possible NAND Flash booting
- Up to 1024*768, 24-bits per pixel LCD controller, TFT and STN panels
- SDIO interface supporting SPI, SD1, SD4 and SD8 mode with card detect, write protect, LED control and interrupt capability.
- 9*9 keyboard controller
- 8 GPIOs with interrupt capability
- Up to 1024 timeslots, master or slave TDM. Any input timeslot can be switched to any output timeslot, and/or can be buffered for computation (up to 16 channels of 1 to 4 timeslots buffered during 30 ms). Up to 16 buffers can be played in output timeslots.
- 18 GPIOs for direct (up to 8) CODEC and/or (up to 8) SLIC management
- I2S interface based on Philips protocol (data delayed by one bit only) allowing up to 64 ms data-buffer both for left and right channels. The I2S interface uses the same memory than SDIO interface and usage is exclusive.
- Second-order noise shaper with *32 to *256 over-sampling for binary or two's complement data. Outputs are complementary with 4 mA capability. DAC uses the same memory then TDM bufferization leading to some limitations to work simultaneously.
- Camera interface ITU-601 with external or embedded synchronization (ITU-656 or CSI2). Picture limit is given by the line length that must be stored in a 2048*32 buffer.

9.2 Block diagram

Figure 8. SPEAr BASIC standard block diagram



9.3 Standard customization memory map

Table 12. RAS_M – communication subsystem

Start address	End address	Peripheral	Notes	Bus
0x4000.0000	0x4FFF.FFFF	C3		AHB
0x5000.0000	0x5000.FFFF	Telecom register		AHB
0x5001_0000	0x5001_0FFF	TDM	Action memory	AHB
0x5003_0000	0x5003_7FFF	TDM	Buffer memory	AHB
0x5004_0000	0x5004_0FFF	TDM	Sync memory	AHB
0x5005_0000	0x5005_0FFF	I2S	I2S memory bank 1	AHB
0x5005_1000	0x5005_1FFF	I2S	I2S memory bank 2	AHB
0x6000.0000	0x6FFF.FFFF	CLCD		AHB
0x7000.0000	0x7FFF.FFFF	SDIO		AHB
0x8000.0000	0x83FF.FFFF	Static memory controller	NAND Bank0	AHB
0x8400.0000	0x87FF.FFFF	Static memory controller	NAND Bank1	AHB
0x8800.0000	0x8BFF.FFFF	Static memory controller	NAND Bank2	AHB
0x8C00.0000	0x8FFF.FFFF	Static memory controller	NAND Bank3	AHB
0x9000.0000	0x90FF.FFFF	Static memory controller	NOR Bank0	AHB
0x9100.0000	0x91FF.FFFF	Static memory controller	NOR Bank1	AHB
0x9200.0000	0x92FF.FFFF	Static memory controller	NOR Bank2	AHB
0x9300.0000	0x93FF.FFFF	Static memory controller	NOR Bank3	AHB
0x9400.0000	0x98FF.FFFF	Static memory controller	Register	AHB
0x9900.0000	0x9FFF.FFFF	Registers		AHB
0xA000.0000	0xA8FF.FFFF	Keyboard		APB
0xA900.0000	0xAFFF.FFFF	GPIO		APB
0xB000.0000	0xBFFF.FFFF	-	Reserved	

9.4 PL_GPIO sharing scheme

Table 13. PL_CLK mapping

PL_CLK	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
0	25 MHz	25 MHz	25 MHz	25 MHz	25 MHz	25 MHz
1	TDM_CLK	TDM_CLK	TDM_CLK	TDM_CLK	TDM_CLK	TDM_CLK
2	TDM_nCLK	TDM_nCLK	TDM_nCLK	TDM_nCLK	TDM_nCLK	TDM_nCLK
3	TDM_CLK2K	TDM_CLK2K	TDM_CLK2K	TDM_CLK2K	TDM_CLK2K	TDM_CLK2K

Table 14. PL_GPIO mapping

PL_GPIO	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
97	FSMC_nCS1	not used	not used	not used	FSMC_nCS1	not used
96	FSMC_D0	KBD_C0	KBD_C0	KBD_C0	FSMC_D0	KBD_C0
95	FSMC_D1	KBD_C1	KBD_C1	KBD_C1	FSMC_D1	KBD_C1
94	FSMC_D2	KBD_C2	KBD_C2	KBD_C2	FSMC_D2	KBD_C2
93	FSMC_D3	KBD_C3	KBD_C3	KBD_C3	FSMC_D3	KBD_C3
92	FSMC_D4	KBD_C4	KBD_C4	KBD_C4	FSMC_D4	KBD_C4
91	FSMC_D5	KBD_C5	KBD_C5	KBD_C5	FSMC_D5	DIO_D0
90	FSMC_D6	KBD_C6	KBD_C6	KBD_C6	FSMC_D6	DIO_D1
89	FSMC_D7	KBD_C7	KBD_C7	KBD_C7	FSMC_D7	DIO_D2
88	FSMC_D8	KBD_C8	KBD_C8	KBD_C8	GPIO_8_0	DIO_D3
87	FSMC_D9	KBD_R0	KBD_R0	KBD_R0	GPIO_8_1	KBD_R0
86	FSMC_D10	KBD_R1	KBD_R1	KBD_R1	GPIO_8_2	KBD_R1
85	FSMC_D11	KBD_R2	KBD_R2	KBD_R2	GPIO_8_3	KBD_R2
84	FSMC_D12	KBD_R3	KBD_R3	KBD_R3	GPIO_8_4	KBD_R3
83	FSMC_D13	KBD_R4	KBD_R4	KBD_R4	GPIO_8_5	KBD_R4
82	FSMC_D14	KBD_R5	KBD_R5	KBD_R5	GPIO_8_6	KBD_R5
81	FSMC_D15	KBD_R6	KBD_R6	KBD_R6	GPIO_8_7	KBD_R6
80	CLCD_D0	not used	not used	CLCD_D0	FSMC_A0	CLCD_D0
79	CLCD_D1	not used	not used	CLCD_D1	FSMC_A1	CLCD_D1
78	CLCD_D2	not used	not used	CLCD_D2	FSMC_A2	CLCD_D2
77	CLCD_D3	not used	not used	CLCD_D3	FSMC_A3	CLCD_D3
76	CLCD_D4	not used	not used	CLCD_D4	FSMC_A4	CLCD_D4
75	CLCD_D5	not used	not used	CLCD_D5	FSMC_A5	CLCD_D5
74	CLCD_D6	not used	not used	CLCD_D6	FSMC_A6	CLCD_D6
73	CLCD_D7	not used	not used	CLCD_D7	FSMC_A7	CLCD_D7

Table 14. PL_GPIO mapping (continued)

PL_GPIO	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
72	CLCD_D8	IT_D0	IT_D0	CLCD_D8	IT_D0	CLCD_D8
71	CLCD_D9	IT_D1	IT_D1	CLCD_D9	IT_D1	CLCD_D9
70	CLCD_D10	IT_D2	IT_D2	CLCD_D10	IT_D2	CLCD_D10
69	CLCD_D11	IT_D3	IT_D3	CLCD_D11	IT_D3	CLCD_D11
68	CLCD_D12	IT_D4	IT_D4	CLCD_D12	IT_D4	CLCD_D12
67	CLCD_D13	IT_D5	IT_D5	CLCD_D13	IT_D5	CLCD_D13
66	CLCD_D14	IT_D6	IT_D6	CLCD_D14	IT_D6	CLCD_D14
65	CLCD_D15	IT_D7	IT_D7	CLCD_D15	IT_D7	CLCD_D15
64	CLCD_D16	IT_SPI_I2C4	IT_SPI_I2C4	CLCD_D16	IT_SPI_I2C4	CLCD_D16
63	CLCD_D17	IT_SPI_I2C5	IT_SPI_I2C5	CLCD_D17	IT_SPI_I2C5	CLCD_D17
62	CLCD_D18	IT_SPI_I2C6	IT_SPI_I2C6	CLCD_D18	IT_SPI_I2C6	CLCD_D18
61	CLCD_D19	IT_SPI_I2C7	IT_SPI_I2C7	CLCD_D19	IT_SPI_I2C7	CLCD_D19
60	CLCD_D20	TDM_SYNC4	TDM_SYNC4	CLCD_D20	TDM_SYNC4	CLCD_D20
59	CLCD_D21	TDM_SYNC5	TDM_SYNC5	CLCD_D21	TDM_SYNC5	CLCD_D21
58	FSMC_CL	TDM_SYNC6	TDM_SYNC6	CLCD_D22	FSMC_CL	CLCD_D22
57	FSMC_AL	TDM_SYNC7	TDM_SYNC7	CLCD_D23	FSMC_AL	CLCD_D23
56	FSMC_nW	KBD_R7	KBD_R7	KBD_R7	FSMC_nW	DIO_HSYNC
55	FSMC_nR	KBD_R8	KBD_R8	KBD_R8	FSMC_nR	DIO_VSYNC
54	CLCD_AC	GPIO_10_9	GPIO_10_9	CLCD_AC	GPIO_10_9	CLCD_AC
53	CLCD_CP	GPIO_10_8	GPIO_10_8	CLCD_CP	GPIO_10_8	CLCD_CP
52	CLCD_FP	GPIO_10_7	GPIO_10_7	CLCD_FP	GPIO_10_7	CLCD_FP
51	CLCD_LP	GPIO_10_6	GPIO_10_6	CLCD_LP	GPIO_10_6	CLCD_LP
50	CLCD_LE	GPIO_10_5	GPIO_10_5	CLCD_LE	GPIO_10_5	CLCD_LE
49	CLCD_PWR	GPIO_10_4	GPIO_10_4	CLCD_PWR	GPIO_10_4	CLCD_PWR
48	CLCD_D22	IT_SPI_I2C0	IT_SPI_I2C0	IT_SPI_I2C0	IT_SPI_I2C0	DIO_D4
47	CLCD_D23	IT_SPI_I2C1	IT_SPI_I2C1	IT_SPI_I2C1	IT_SPI_I2C1	DIO_D5
46	GPIO7	IT_SPI_I2C2	IT_SPI_I2C2	IT_SPI_I2C2	IT_SPI_I2C2	DIO_D6
45	GPIO6	IT_SPI_I2C3	IT_SPI_I2C3	IT_SPI_I2C3	IT_SPI_I2C3	DIO_D7
44	GPIO5	DAC_O0	DAC_O0	DAC_O0	DAC_O0	DAC_O0
43	GPIO4	DAC_O1	DAC_O1	DAC_O1	DAC_O1	DAC_O1
42	GPIO3	I2S_DIN	I2S_DIN	I2S_DIN	I2S_DIN	I2S_DIN
41	GPIO2	I2S_LRCK	I2S_LRCK	I2S_LRCK	I2S_LRCK	I2S_LRCK
40	GPIO1	I2S_CLK	I2S_CLK	I2S_CLK	I2S_CLK	I2S_CLK
39	GPIO0	I2S_DOUT	I2S_DOUT	I2S_DOUT	I2S_DOUT	I2S_DOUT
38	TDM_SYNC1	TDM_SYNC1	TDM_SYNC1	TDM_SYNC1	TDM_SYNC1	TDM_SYNC1

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Table 14. PL_GPIO mapping (continued)

PL_GPIO	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
37	TDM_DOUT	TDM_DOUT	TDM_DOUT	TDM_DOUT	TDM_DOUT	TDM_DOUT
36	TDM_SYNC0	TDM_SYNC0	TDM_SYNC0	TDM_SYNC0	TDM_SYNC0	TDM_SYNC0
35	TDM_CLK	TDM_CLK	TDM_CLK	TDM_CLK	TDM_CLK	TDM_CLK
34	TDM_DIN	TDM_DIN	TDM_DIN	TDM_DIN	TDM_DIN	TDM_DIN
33	SD_CMD	SD_CMD	SD_CMD	SD_CMD	SD_CMD	SD_CMD
32	SD_CLK	SD_CLK	SD_CLK	SD_CLK	SD_CLK	SD_CLK
31	SD_D0	SD_D0	SD_D0	SD_D0	SD_D0	SD_D0
30	SD_D1	SD_D1	SD_D1	SD_D1	SD_D1	SD_D1
29	SD_D2	SD_D2	SD_D2	SD_D2	SD_D2	SD_D2
28	SD_CD_D3	SD_CD_D3	SD_CD_D3	SD_CD_D3	SD_CD_D3	SD_CD_D3
27	MII_TXCLK	MII_TXCLK	SD_D4	SD_D4	GPIO_8_0	SD_D4
26	MII_TXD0	MII_TXD0	SD_D5	SD_D5	GPIO_8_1	SD_D5
25	MII_TXD1	MII_TXD1	SD_D6	SD_D6	GPIO_8_2	SD_D6
24	MII_TXD2	MII_TXD2	SD_D7	SD_D7	GPIO_8_3	SD_D7
23	MII_TXD2	MII_TXD2	GPIO_8_4	GPIO_8_4	GPIO_8_4	GPIO_8_4
22	MII_TXEN	MII_TXEN	GPIO_8_5	GPIO_8_5	GPIO_8_5	GPIO_8_5
21	MII_TXER	MII_TXER	GPIO_8_6	GPIO_8_6	GPIO_8_6	DIO_D8
20	MII_RXCLK	MII_RXCLK	GPIO_8_7	GPIO_8_7	GPIO_8_7	DIO_D9
19	MII_RXDV	MII_RXDV	GPIO_10_0	GPIO_10_0	GPIO_10_0	DIO_D10
18	MII_RXER	MII_RXER	GPIO_10_1	GPIO_10_1	GPIO_10_1	DIO_D11
17	MII_RXD0	MII_RXD0	GPIO_10_2	GPIO_10_2	GPIO_10_2	DIO_D12
16	MII_RXD1	MII_RXD1	GPIO_10_3	GPIO_10_3	GPIO_10_3	DIO_D13
15	MII_RXD2	MII_RXD2	GPIO_10_4	GPIO_10_4	GPIO_10_4	GPIO_10_4
14	MII_RXD3	MII_RXD3	GPIO_10_5	GPIO_10_5	GPIO_10_5	GPIO_10_5
13	MII_COL	MII_COL	GPIO_10_6	GPIO_10_6	GPIO_10_6	GPIO_10_6
12	MII_CRS	MII_CRS	GPIO_10_7	GPIO_10_7	GPIO_10_7	GPIO_10_7
11	MII_MDC	MII_MDC	GPIO_10_8	GPIO_10_8	GPIO_10_8	GPIO_10_8
10	MII_MDIO	MII_MDIO	GPIO_10_9	GPIO_10_9	GPIO_10_9	GPIO_10_9
9	SSP_MOSI	SSP_MOSI	SSP_MOSI	SSP_MOSI	SSP_MOSI	SSP_MOSI
8	SSP_CLK	SSP_CLK	SSP_CLK	SSP_CLK	SSP_CLK	SSP_CLK
7	SSP_SS0	SSP_SS0	SSP_SS0	SSP_SS0	SSP_SS0	SSP_SS0
6	SSP_MISO	SSP_MISO	SSP_MISO	SSP_MISO	SSP_MISO	SSP_MISO
5	I2C_SDA	I2C_SDA	I2C_SDA	I2C_SDA	I2C_SDA	I2C_SDA
4	I2C_SCL	I2C_SCL	I2C_SCL	I2C_SCL	I2C_SCL	I2C_SCL
3	UART_RX	UART_RX	UART_RX	UART_RX	UART_RX	UART_RX

Table 14. PL_GPIO mapping (continued)

PL_GPIO	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
2	UART_TX	UART_TX	UART_TX	UART_TX	UART_TX	UART_TX
1	FSMC_nCS2	IRDA_RX	IRDA_RX	IRDA_RX	IRDA_RX	IRDA_RX
0	FSMC_RnB	IRDA_TX	IRDA_TX	IRDA_TX	IRDA_TX	IRDA_TX

9.4.1 LCD controller

Main features

- Compliance to the AMBA specification (Rev 2.0) onwards for easy integration into SoC implementation
- Dual 16-deep programmable 32-bit wide FIFOs for buffering incoming display data
- Supports single and dual panel mono super twisted nematic (STN) displays with 4 or 8-bit interfaces
- Supports single and dual-panel color and monochrome STN displays
- Supports thin film transistor (TFT) color displays
- Resolution programmable up to 1024 x 768
- 15 gray-level mono, 3375 color STN, and 32 K color TFT support
- 1, 2, or 4 bits per pixel (bpp) palettized displays for mono STN
- 1, 2, 4 or 8 bpp palettized color displays for color STN and TFT
- 16 bpp true-color non-palettized, for color STN and TFT
- 24 bpp true-color non-palettized, for color TFT
- Programmable timing for different display panels
- 256 entry, 16-bit palette RAM, arranged as a 128 x 32-bit RAM physically frame, line and pixel clock signals
- AC bias signal for STN and data enable signal for TFT panels patented gray scale algorithm
- Supports little and big-endian as well as WinCE data formats.

Programmable parameters

- Horizontal front and back porch
- Horizontal synchronization pulse width
- Number of pixels per line
- Vertical front and back porch
- Vertical synchronization pulse width
- Number of lines per panel
- Number of panel clocks per line
- Signal polarity, active high or low
- AC panel bias
- Panel clock frequency
- Bits per pixel
- Display type, STN mono/color or TFT
- STN 4 or 8-bit interface mode
- STN dual or single panel mode
- WinCE mode
- Interrupt generation event.

LCD panel resolutions

- 320x200, 320x240
- 640x200, 640x240, 640x480
- 800x600
- 1024x768.

Types of LCD panel supported

- Active matrix TFT panels with up to 24-bit bus interface
- Single-panel monochrome STN panels (4-bit and 8-bit bus interface)
- Dual-panel monochrome STN panels (4-bit and 8-bit bus interface per panel)

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9.4.2 SD card controller

This controller conforms to the SD host controller standard specification version 2.0. It handles SDIO/SD protocol at transmission level, packing data, adding cyclic redundancy check (CRC), start/end bit, and checking for transaction format correctness.

The SD card controller provides programmed IO method and DMA data transfer method.

In the programmed IO method, the ARM processor transfers data using the buffer data port register. Host controller support for DMA can be determined by checking the DMA support in the capabilities register. DMA allows a peripheral to read or write memory without the intervention from the CPU.

The system address register points to the first data address, and data is then accessed sequentially from that address.

Key features

- Meets SD host controller standard specification version 2.0
- Meets SDIO card specification version 2.0
- Meets SD memory card specification draft version 2.0
- Meets SD memory card security specification version 1.01
- Meets MMC specification version 3.31 and 4.2
- Supports both DMA and Non-DMA mode of operation
- Supports MMC plus and MMC mobile
- Card detection (insertion/removal)
- Password protection of cards
- Host clock rate variable between 0 and 52 MHz
- Supports 1-bit, 4-bit and 8-bit SD modes and SPI mode
- Supports MultiMediaCard interrupt mode
- Allows card to interrupt host in 1-bit, 4-bit, 8-bit SD modes and SPI mode.
- Up to 100 Mbit/s data rate using 4 parallel data lines (sd4-bit mode)
- Up to 416 Mbit/s data rate using 8-bit parallel data lines (sd8-bit mode)
- Cyclic redundancy check CRC7 for command and CRC16 for data integrity
- Designed to work with I/O cards, read-only cards and read/write cards
- Error correction code (ECC) support for MMC4.2 cards
- Supports read wait control, suspend/resume operation
- Supports FIFO overrun and Under run condition by stopping the SD clock

9.4.3 Flexible static memory controller

Main features of the FSMC are listed below:

- Provides an interface between AHB system bus and external parallel memory devices.
- Interfaces static memory-mapped devices including RAM, ROM and synchronous burst Flash.
- For SRAM, ROM and Flash 8/16-bit wide, external memory and data paths are provided.
- FSMC performs only one access at a time and only one external device is accessed.
- Little-endian and big-endian memory architectures.
- AHB burst transfer handling to reduce access time to external devices.
- Supplies an independent configuration for each memory bank.
- Programmable timings to support a wide range of devices.
 - Programmable wait states (up to 31).
 - Programmable bus turnaround cycles (up to 15).
 - Programmable output enable and write enable delays (up to 15).
- Independent chip select control for each memory bank.
- Shares the address bus and the data bus with all the external peripherals.
- Only chips selects are unique for each peripheral.
- External asynchronous wait control.
- Configurable size at reset for boot memory bank using external control pins.

9.4.4 Keyboard interface

The keyboard interface uses 18 pins. These pins can be either used as standard GPIOs or to drive a 9*9 keyboard (81 keys). The keyboard scan period can be adjusted between 10 ms and 80 ms.

When in keyboard mode, pressing a key generates an interrupt when enabled through the IT_DMA block.

Two successive scan must be validated with the same key pressed before a key press is detected. After detection, two “no key pressed” cycles must be observed before allowing a new keypress detection.

Any new keypress event latches the data into the KBREG register and sets the interrupt bit, even if the previously pressed key has not been read and the interrupt register cleared.

If several keys are pressed, only the first detected one is registered.

The pressed key value can be read through in the KBREG register. The interrupt is cleared in the interrupt handler by clearing the STATUSREG register.

[Table 15](#) shows the KBREG values.

Table 15. KBREG coding

	COL8	COL7	COL6	COL5	COL4	COL3	COL2	COL1	COL0
ROW8	80	79	78	77	76	75	74	73	72
ROW7	71	70	69	68	67	66	65	64	63
ROW6	62	61	60	59	58	57	56	55	54
ROW5	53	52	51	50	49	48	47	46	45
ROW4	44	43	42	41	40	39	38	37	36
ROW3	35	34	33	32	31	30	29	28	27
ROW2	26	25	24	23	22	21	20	19	18
ROW1	17	16	15	14	13	12	11	10	9
ROW0	8	7	6	5	4	3	2	1	0

9.4.5 TDM interface

The TDM block implements time division multiplexing with up to 1024 time slots. It uses 11 pins.

Table 16. TDM block pins

Pins	Description
SYNC7-0	Dedicated frame synchro for CODECs without timeslot recognition
CLK	TDM clock
DIN	TDM input
DOUT	TDM output (tri-state)

The TDM interface can be the master or a slave of the CLK or SYNC0 signals.

It is a master when generating SYNC1 to SYNC7, which are seven additional sync signals for devices that do not recognize time slots, or which need a special synchronization waveform.

DIN receives the data.

DOUT transmits the data. This line can be high impedance on timeslot not used.

Timeslots can be used in two ways: switching or bufferization. The information about timeslot usage is written in a 1024*32 memory, termed the '*action memory*'. Switching and bufferization can be used concurrently for different timeslots on the same TDM. The only limitation is that an output timeslot can not be switched and bufferized at the same time.

Clock signal: device can be master or slave.

In master mode the CLK signal can be generated from different sources:

- ClkR_Osc1: MCLK clock from external MCLK crystal
- ClkR_Gpio4: external oscillator from PL_CLK4 pin.
- ClkR_Synt_3: From frequency synthesiser (source is AHB frequency).

All three signals can be divided by the TDM_CLK block in order to obtain the correct frequency.

In slave mode, the clock is received on the TDM_CLK pin.

The clock used internally is present on the PL_CLK pins.

Sync signal: device can be master or slave.

SYNC0 can be master or slave. SYNC1 to SYNC7 are additional generated synchro dedicated to devices that does not recognize the timeslots or which need special waveforms.

SYNC1 to SYNC3 are built from SYNC0.

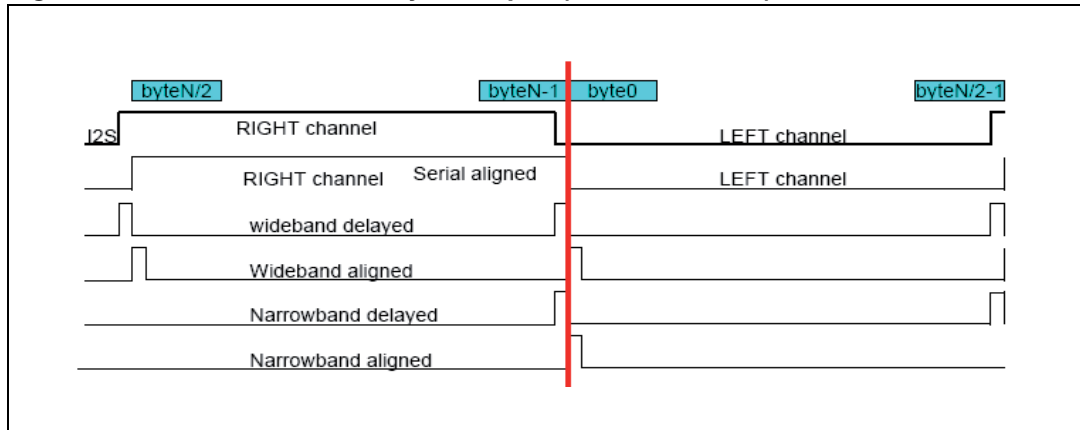
Sync0 in slave and master mode and Sync1 to Sync3 support several pre-defined wave shapes.

SYNC4 to SYNC7 are generated using the SYNC memory (1024*32) where each bit is set to 0 or 1 to generate the right pattern on the pin during a frame.

The following pre-defined shapes are available:

- short frame narrow-band delayed and non delayed
- short frame wide-band delayed and non delayed
- I2S or serial aligned long frame.

Figure 9. Pre-defined frame sync shapes (slave or master)



SYN4 to SYNC7 are generated from the sync memory. The sync memory has 1024 words per four bytes. Byte0 of each location is used to generate SYNC4. Byte1 for SYNC5, Byte2 for SYNC6 and Byte3 for SYNC7. The MSB of each byte is issued first. The LSB is issued the last. This covers the 1024 possible time slots for the four sync signals.

TDM timeslot switching

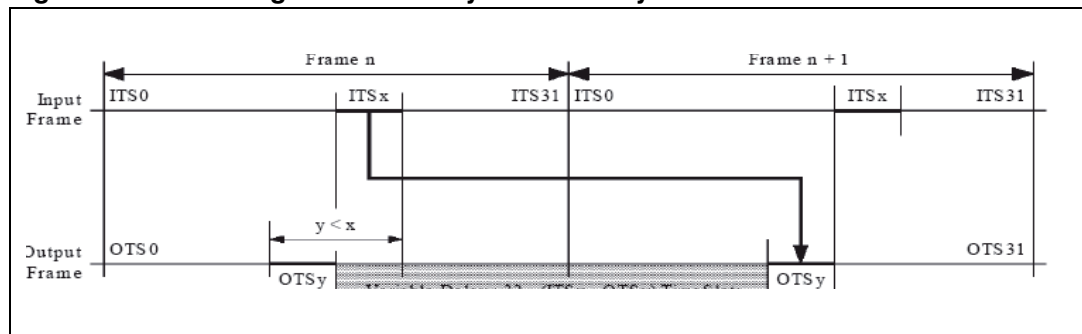
Any of the output time slots can receive any input timeslot of the previous frame. The connection memory is part of the action memory, informing which timeslot has to be output. The data memory contains two banks. One storing the actual frame from the DIN pin (if switching has been validated for this timeslot in the action memory), the other outputting the data from the previous frame on DOUT (if the switching has been validated and high impedance bit is not set in the action memory).

The delay between out_TS_y receiving IN_TS_x for a TDM containing N+1 timeslots is constant:

$$\text{Delay}(\text{TS}) = y + (N+1 - x)$$

with x and y between 0 and N.

Figure 10 shows an example with N+1 = 32.

Figure 10. Switching constant delay between TSy and TSx

Note: The last timeslot of a frame can be played in the first timeslot of the next frame.

TDM timeslot bufferization

Bufferization means that data from DIN is stored in an input buffer and data from an output buffer is played on DOUT. When the number of sample stored/played reaches the buffer size, the processor is interrupted in order to read the input buffer and prepare a new output buffer (or a DMA request is raised).

Up to 16 channels can be stored or played. It is not mandatory that an input-bufferized channel is also output bufferized (it can be switched or high impedance).

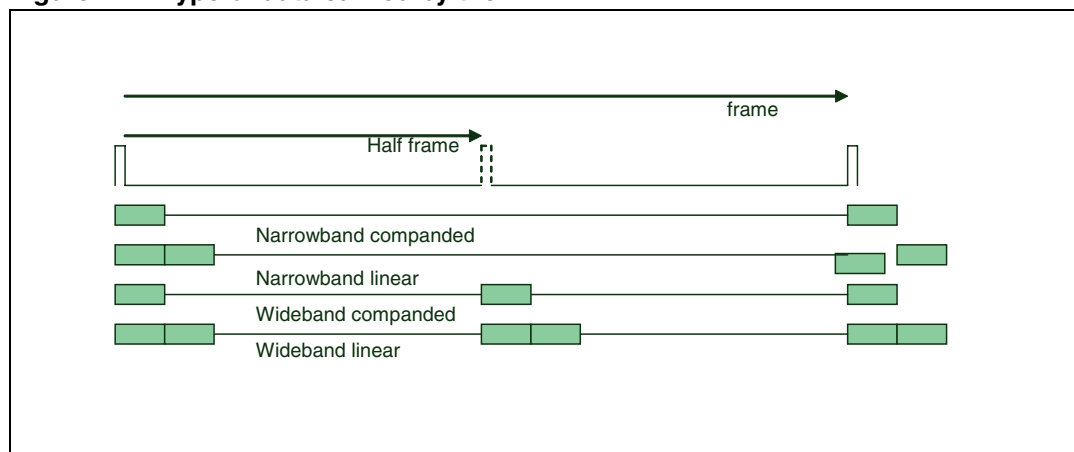
Channels can contain one byte (timeslot) when the data is companded, two bytes when the data is either stereo companded or mono linear (16-bits) or four bytes when the data is stereo linear. The timeslots need not be successive, but must be byte aligned.

When using 16 channels, 512 ms buffers can be used for stereo linear mode. Using 8, 4, 2 or 1 channel increases the buffer size to 1024, 2048, 4096 or 8192 ms (always for stereo linear mode). If data is on two bytes per frame, the values are doubled. If data is mono companded the data are multiplied by four.

All the channels must have the same buffer size. Thus if a vocoder for one channel requires 30 ms packets, and another channel requires 20 ms, a 10 ms buffer must be created, and DMA used to generate the voice packet in the DDR.

Otherwise, if all the channels require the same packet size, the data can be directly computed inside the buffer and do not need to be transferred to DDR. The only constraint is to maintain operation the real time.

Figure 11. Type of data carried by the TDM



Two banks are used to exchange the samples with the processor. The number of sample stored in a buffer is programmable.

When the TDM reads and stores the data in one bank, the processor is owner of the other bank, allowing it to read the received data before writing a new buffer to be played.

The processor can compute the data directly in the buffer.

When the two banks are switched, this can generate either an interrupt or a DMA transfer. When this event occurs, if the processor has not finished to compute the previous input buffer and to store the new output buffer, the computation is out of real time. The software must to check that operations are done in real time.

To avoid synchronization issues, the MSB of the buffer address can be managed by the device itself, the processor always accessing the right bank at addresses 0x0000 to 0x3FFF.

9.4.6 I2S interface

The I2S block is very similar to TDM block, but the frame sync is limited to Philips I2S definition.

www.DataSheet4U.com The I2S block can be master or slave for the clock.

The I2S block can be master or slave for the sync signal.

Bufferization is limited to 1024 samples (512 left and 512 right samples representing 64 ms of voice). Data is stored always on 32-bits. Left and right channels are stored in two different buffers. Two banks are used to exchange data with the processor.

The I2S interface is composed of 4 signals which are shown in [Table 17](#).

Table 17. I2S interface pins

Pins	Description
I2S_LRCK	Left and right channels synchronization (master/slave)
I2S_CLK	I2S clock (master/slave)
I2S_DIN	I2S input
I2S_DOUT	I2S output (tri-state)

- **I2S_LRCK** in master mode can be adjusted for duration of 8, 16 or 32-bits low or high. The data width can be smaller than I2S_LRCK width.
- **I2S_DIN** receives the data. Data can be 8, 16 or 32-bits wide, and is always stored as 32-bit words. A shift left operation to left-align the data is possible.
- **DOUT** transmits the data. Data can be 8, 16 or 32-bits, anyway data must be always stored in 32-bits wide in the buffer. A shift left operation is possible to left align the data. The DOUT line can be high impedance when out of the samples bits.
- **CLK** signal In master mode can be generated from different sources:
 - ClkR_Osci1: MCLK clock from external MCLK crystal
 - ClkR_Gpio4: external oscillator from PL_CLK4 pin.
 - ClkR_Synt_2: from frequency synthesizer (source is AHB frequency),
 - TDM_CLK: I2S and TDM interfaces use the same clock.

The three first signals can be divided by the I2S_CLK block in order to reach the correct frequency.

In slave mode, the clock is received on the I2S_CLK pin (same pin used in master or slave mode).

Two banks are used to exchange the samples with the processor. The number of sample stored in a buffer is programmable.

When the I2S interface reads and stores the data in one bank, the processor is owner of the other bank, allowing it to read the received data before writing a buffer to be played.

The processor can compute the data directly in the buffer.

When the two banks are switched, this can generate an interrupt or DMA transfer. When this event occurs, if the processor has not finished computing the previous input buffer and storing the new output buffer, the computation is out of real time. The software must check that operations are done in real time.

To avoid synchronization issues. The MSB of the buffers address can be managed by the device itself. The processor always accesses the right bank between addresses 0x0000 and 0xFFFF.

9.4.7 SPI_I2C cell

The SPI interface has only one slave select signal, SS0.

The I²C interface does not allow control of several devices with the same address what is frequent for CODECs.

This IP allows management extension of up to 8 SPI devices, or 8 I²C devices at the same address (total SPI+I²C devices=8).

The SPI extension is made by generating three more slave select signals SS1, SS2 and SS3.

The I²C extension is done by repeating the I2C_SCL signal if the considered pin is set active.

Otherwise the pin remains low, so that the start condition is not met.

Each of the 8 pins can reproduce either the SPI SS0 signal, or the I²C I2C_SCL signal. The selection is made through a register.

9.4.8 GPIO_IT cell

GPIO_IT is an 8-bit supervised input bus. It can be programmed to generate a change interrupt (ITch) when a change is detected on any of the eight bus signals. If it is important that the change persists for more than a determined time before an interrupt is generated, a 'persist' interrupt (ITp) can be programmed.

The signal is latched twice, and the two latched signals are compared. If they are different, an ITch interrupt is generated if the line is programmed to generate a change interrupt (and it is not masked). The programmer can then read both the first and the second latch registers.

The number of clocks before validating a persistent change is programmable. An ITp interrupt is generated if the line is programmed to generate a persist interrupt (and it is not masked). When the persistency counter reaches the persistence time, the data is latched and the programmer can read the latched data.

This interface is principally intended for supervision of the hook detection of up to 8 SLICs. However it is also useful for switch debouncing and simple interrupt generation when a signal toggles.

The GPIO_IT interface is clocked by the TDM clock.

9.4.9 One bit DAC

The one-bit DAC is a second-order noise shaper based on the TDM hardware. The action memory determines whether a new sample needs to be sent to the DAC during the next byte. Samples are read from the buffer memory.

Input data must be 32-bits wide, either in 2's complement or binary form.

Optionally, the order of the noise shaper can be set to 1.

Operation without using the TDM

DAC cell is capable of operating without using the TDM. In this case, the input data can be over sampled by the processor then over sampled by the DAC by a factor between 32 and 256. For example, 64 kHz over sampled data leads to a 2048 kHz output waveform when the DAC over sampling factor is set to 32.

Operation in conjunction with the TDM

When used in conjunction with the TDM, a bufferization channel must be reserved for the DAC. In this case the input sampling frequency must be either 8 kHz (standard TDM) or 16 kHz (when connecting wide-band CODECs for instance). The number of bits in a frame must be fixed between 32 and 256, leading to an over-sampling factor of 32 to 256. For example an 8 kHz input and a 256-bit frame generates a 2048 kHz output.

DAC performances

Table 18. DAC performances

Symbol	Min	Typ	Max
Input bits		32	
oversampling	32		256
S/N ratio		82 dB ⁽¹⁾	
THD		72 dB ⁽¹⁾	
dynamic	80% of full scale		

1. Measured on a 1 kHz sine wave *64 over sampled by the processor and *32 by the DAC.

9.4.10 ADC enhanced control

The ADC is a 10-bit, 8 channel cell described in [Section 8.14](#).

In order to synchronize the TDM or the DAC and the ADC, there is a mechanism allowing channel 0 to be controlled by the TDM clock.

The ADC sampling rate can be adjusted from the sync frequency (generally 8 kHz), up to TDM CLK frequency. For example, if the SYNC signal is at 8 kHz and the CLK signal is at 2048, the ADC sampling can be requested every 2-bits, leading to an over sampling of 128. In this case the resolution of the ADC is increased to 13.5-bits.

9.4.11 Camera interface

The camera interface receives data from a sensor in parallel mode (8 to 14-bits) by storing a full line in a buffer memory, then requesting a DMA transfer or interrupting the processor.

When all the lines of a frame are transferred, a frame sync interrupt is generated.

The camera interface accepts both hardware synchronization (HSYNC and VSYNC signals) or embedded synchronos (ITU656 or CSI2).

[Figure 12](#), [Figure 13](#), [Figure 14](#), [Figure 15](#) shows the three possible synchronizations:

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Figure 12. External HSYNC synchronization

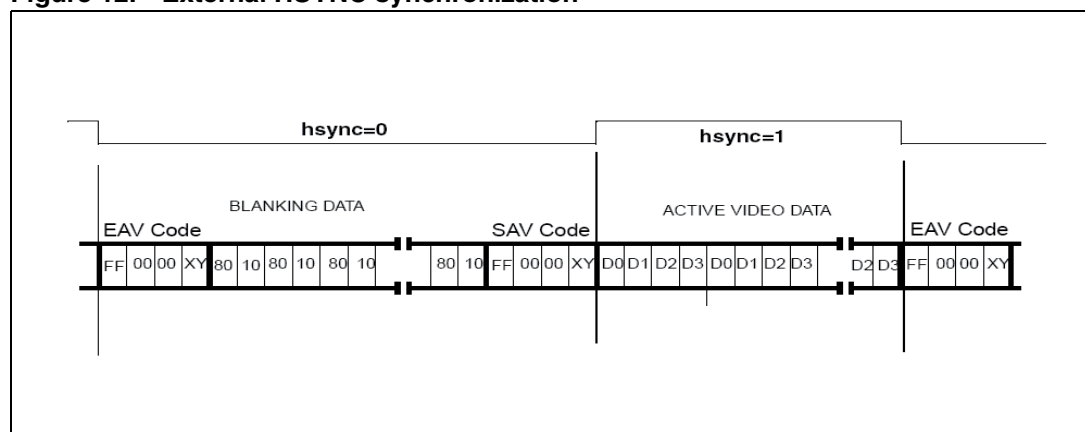


Figure 13. External VSYNC synchronization

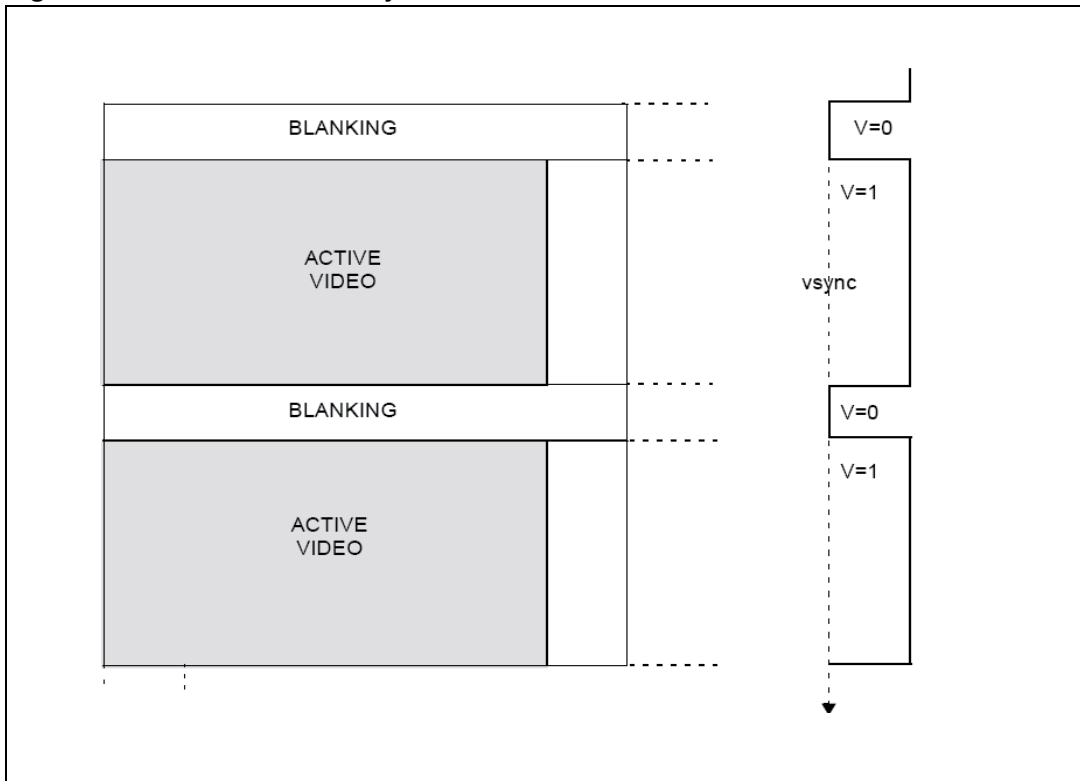
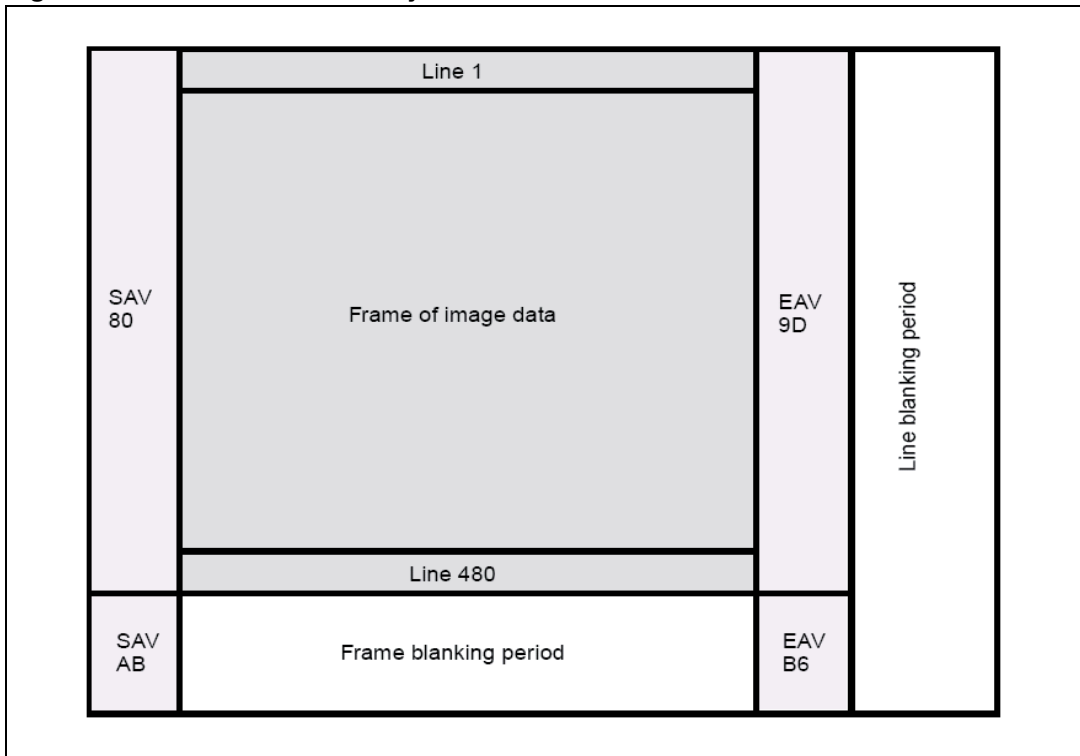
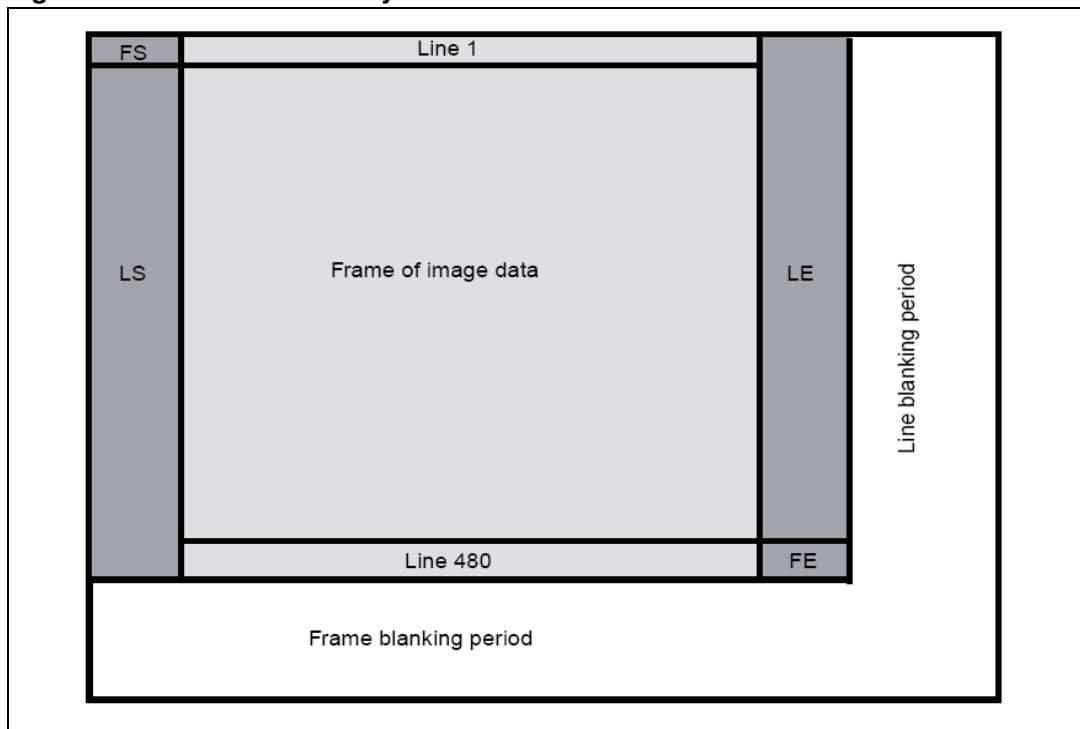


Figure 14. ITU656 embedded synchronization



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Figure 15. CSI2 embedded synchronization



The data carried by the bus can be either raw Bayer, JPEG compressed or one of several other common data formats. See [Table 19](#).

Data is stored in a 2048*32 buffer memory. The incoming format, as well as the number of banks inside the buffer memory impacts the maximum image size.

One or two banks can be used. The only constraint is that the processor or the DMA read the memory before a new line is stored.

Table 19. Maximum picture size according data format and buffer size

Format of Incoming data	Incoming data size	Storage size	Max 4/3 pict size (buf=2048)	Max 4/3 pict size (buf=1024)
Raw bayer10	10 -14 bits/pixel	2 bytes	12.58 Mpix	3.14 Mpix
Raw bayer8	8 bits/pixel	1 byte	50.33 Mpix	12.58 Mpix
RGB888	3 byte/pixel	4 bytes	3.14 Mpix	0.79 Mpix
RGB565	2 bytes/pixel	2 bytes	12.58 Mpix	3.14 Mpix
RGB444	2 byte/pixel	2 bytes	12.58 Mpix	3.14 Mpix
YCbCr444	3 bytes/pixel	4 bytes	3.14 Mpix	0.79 Mpix
YCbCr422	4 bytes/2pixel	2*2 bytes	12.58 Mpix	3.14 Mpix
YCbCr400	1 byte/pixel	1 byte	50.33 Mpix	12.58 Mpix
MPEG	/Squeeze	raw	>>100 Mpix	>> 100 Mpix

The camera interface can be assigned to two different set of pins. When using data greater than 8-bits, it is not possible to use the MII interface.

Table 20. Camera interface pinout

Pinout	Description
HSYNC	Horizontal synchro (line)
VSYNC	Vertical synchro (frame)
PixCLK	Pixel clock
DIO0	Data0
DIO1	Data1
DIO2	Data2
DIO3	Data3
DIO4	Data4
DIO5	Data5
DIO6	Data6
DIO7	Data7
DIO8	Data8 extension
DIO9	Data9 extension
DIO10	Data10 extension
DIO11	Data11 extension
DIO12	Data12 extension
DIO13	Data13 extension

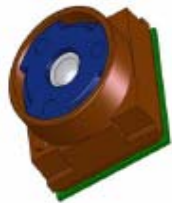


Figure 16. Camera interface waveforms

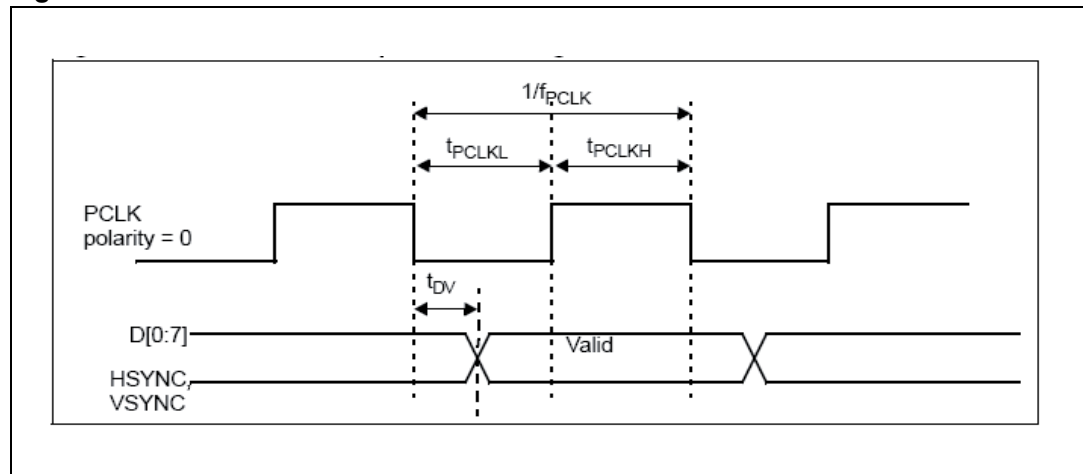


Table 21. Camera interface timing specification

Symbol	Description	Min	Max	Unit
f_{PCLK}	PCLK frequency		100	MHz
t_{PCLKL}	PCLK low width	$1/f_{PCLK} - 3$	$1/f_{PCLK} + 3$	ns
t_{PCLKH}	PCLK high width	$1/f_{PCLK} - 3$	$1/f_{PCLK} + 3$	ns
t_{DV}	PCLK to data	-3	3	ns

9.4.12 Interrupt and DMA request management

This IP collects the interrupt request of several IPs in order to merge them on the interrupt0 line of the interrupt controller. The interrupt handler that must determine the root of the interrupt.

The IPs using interrupt0 line are the following:

- Keyboard,
- Legacy GPIOs,
- GPIO_IT bus,
- I2S,
- TDM,
- Camera interface.

The IP is also connected on DMA_REQ channels 2 to 4 and transmits the request from the following IPs:

- I2S,
- TDM,
- Camera interface.

DMA requests can be DMA burst request and/or DMA single request.

Events of the different IPs able to generate an interrupt are the following:

- Keyboard,
- Legacy GPIOs,
- IT_GPIO persistent change supervision,
- IT_GPIO change supervision,
- I2S buffer bank switching,
- TDM buffer bank switching,
- Camera interface new line available,
- Camera interface end of frame,
- Camera interface vertical sync appears active.

The following types of IP DMA requests are supported:

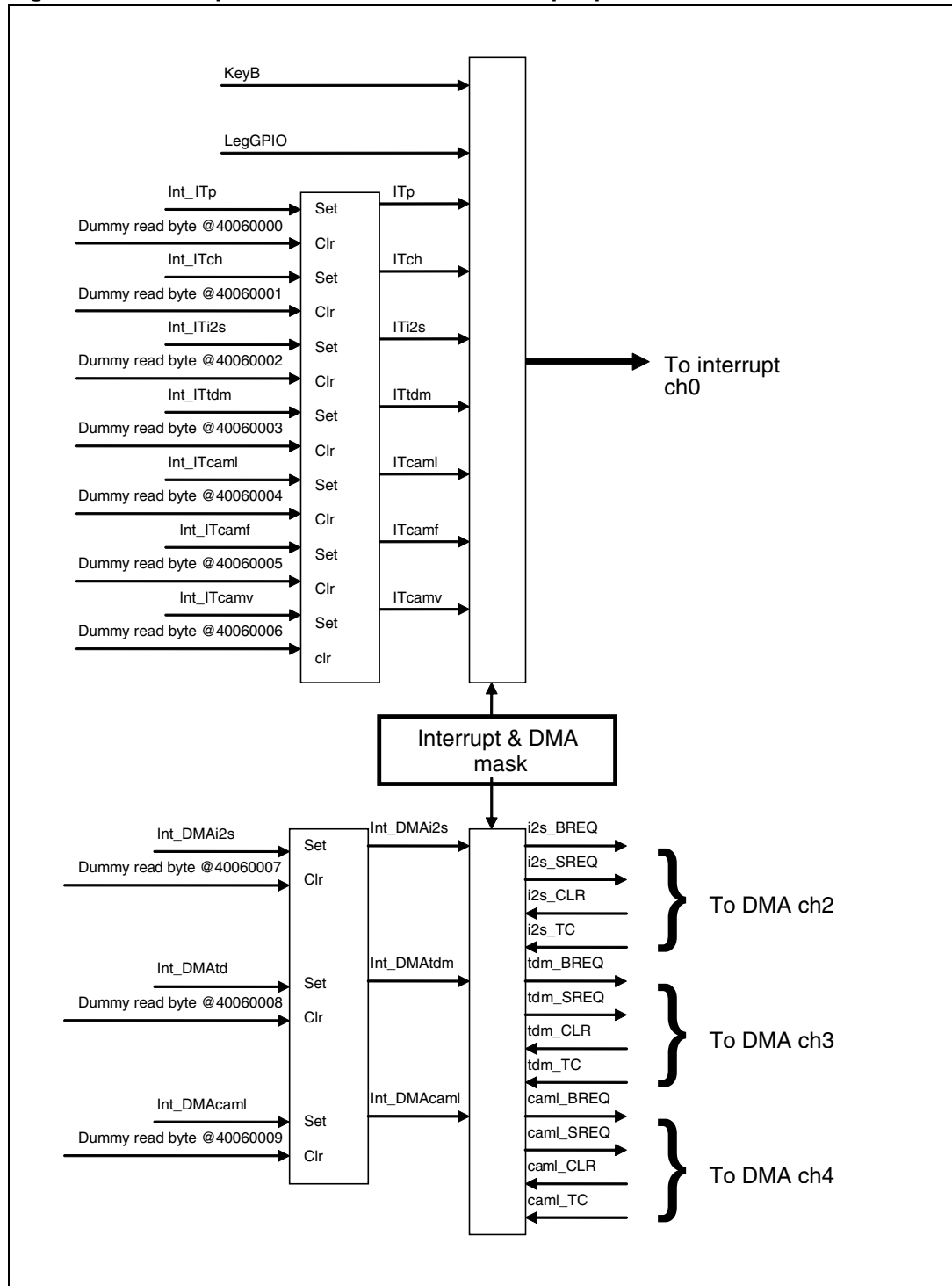
- I2S buffer bank switching,
- TDM buffer bank switching,
- Camera interface new line available.

Keyboard and Legacy GPIOs can only generate interrupts (no DMA requests). These interrupts are cleared by writing inside the keyboard or legacy GPIOs registers. They are masked in this block.

All other features managed by this block can generate interrupts. These interrupts are cleared by a dummy byte access in the 0x5006xxxx area from the interrupt handler, and masked by the mask register of this block.

I2S, TDM and end of line from camera interface can launch a DMA transfer. DMA transfer are masked by the mask register of this block and cleared by the DMA controller (DMA_CLR and DMA_TC signals).

Figure 17. Interrupt and DMA block for telecom peripherals



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9.5 TDM timing

Figure 18. TDM signals description

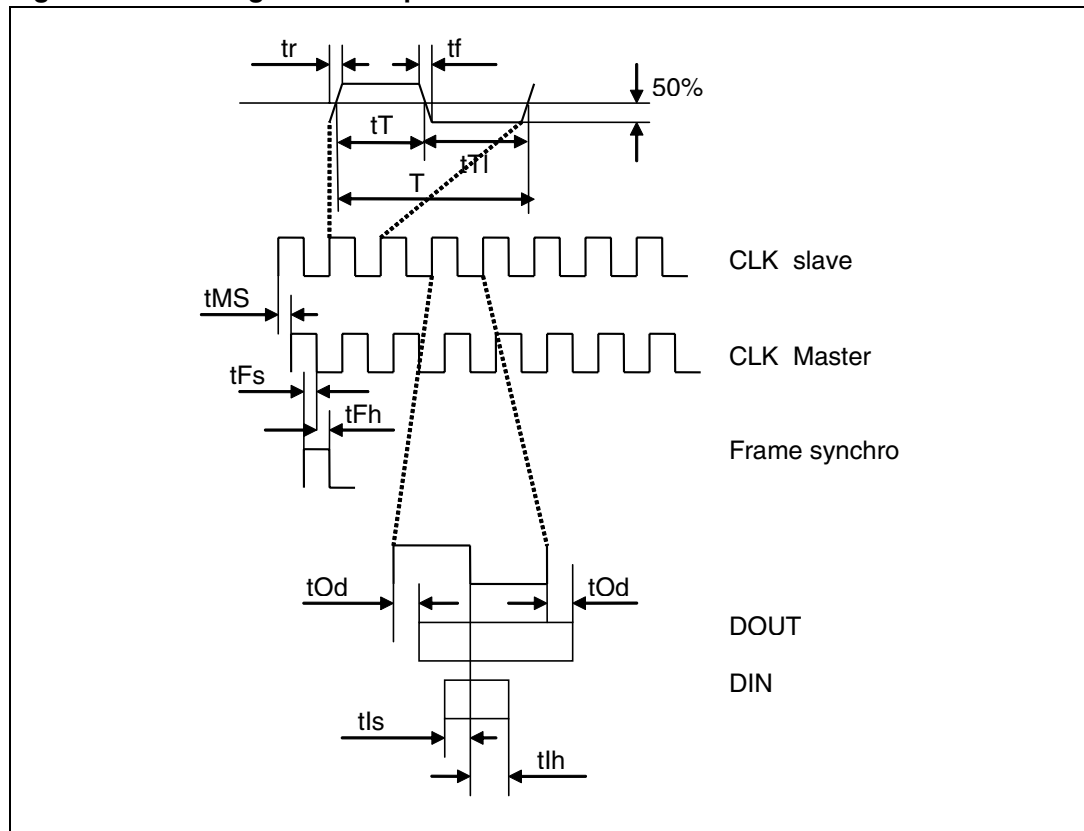


Table 22. TDM timing specification (1024 TS = 65536 kHz = 15.26 ns)

Symbol	Description	Min	Typ	Max	Unit
t	Clock frequency	15.26			ns
t_{Th}/t_{Tl}	High to low clock ratio	75	100	125	ns
t_r, t_f	Clock rising and falling time			3	ns
t_{MS}	Clock slave to master delay			3	ns
t_{Fs}	Frame synchro setup time	3		$t - 3$	ns
t_{Fh}	Frame synchro hold time	3		Frame - t - 3	ns
t_{Od}	Output data delay/clock			3 (5pF)	ns
t_{Is}	Input data setup time	3			ns
t_{Ih}	Input data hold time	3			ns

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9.5.1 I2S interface timings

Figure 19. TDM signals description

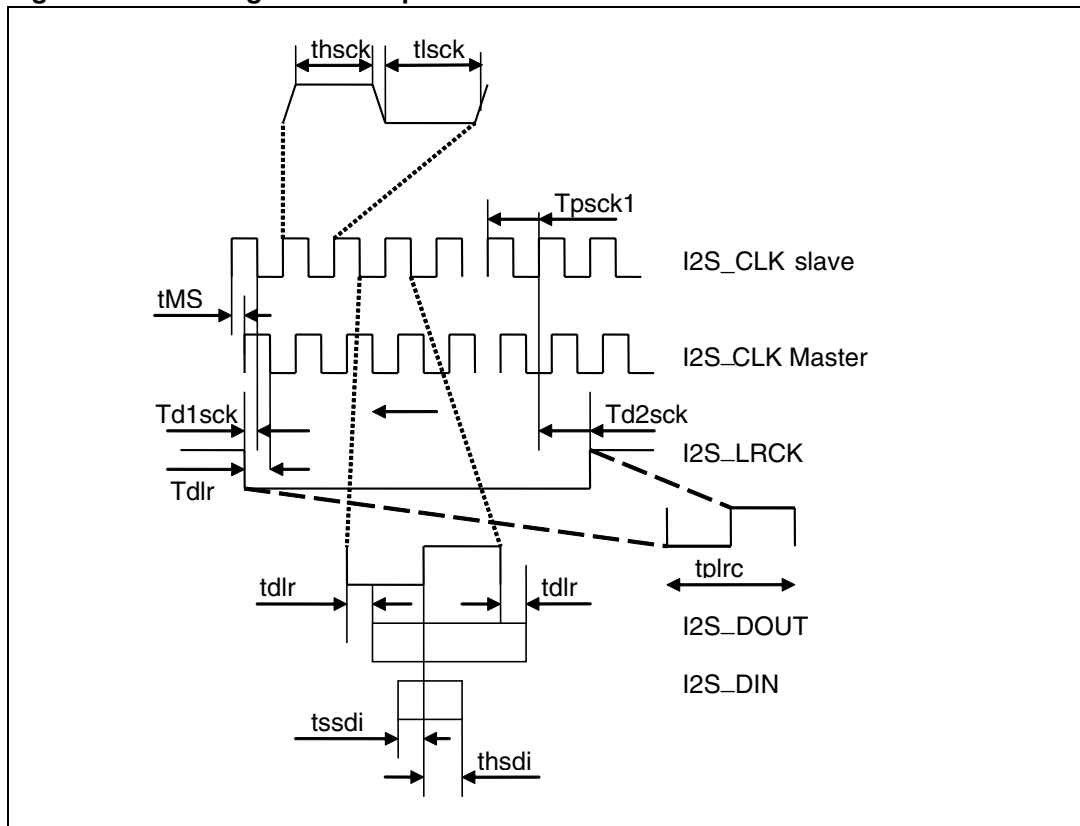


Table 23. I2S timing specification

Symbol	Description	Min	Typ	Max	Unit
t_{psck1}	Clock frequency	50			ns
t_{hsc1} , t_{lsck}	High or low clock time	20			ns
t_{plrk}	lrck period	20		127	μ s
I_{rckDC}	lrck duty cycle	40		60	%
t_{d1sck}	slave lrck to clk falling	-10		600	ns
t_{d2sck}	clk rising to lrck rising	20			ns
t_{dlr}	clk falling to lrck edge			10	ns
t_{ssdi} , t_{hsdi}	Setup or hold time data in	10			ns

10 Electrical characteristics

10.1 Absolute maximum ratings

This product contains devices to protect the inputs against damage due to high static voltages. However it is advisable to take normal precaution to avoid application of any voltage higher than the specified maximum rated voltages.

Table 24. Absolute maximum rating

Symbol	Description	Value	Unit
V _{DD core}	Supply voltage core	1.6	V
V _{DD I/O}	Supply voltage I/O	4.8	V
V _{DD PLL}	Supply voltage PLL		V
V _{DD D_{DR}}	Supply voltage DRAM interface	4.8	V
V _{DD R_{TC}}	Supply voltage RTC	2.4	V
T _J	Junction temperature	-40 to 125	°C
T _{STG}	Storage temperature	-55 to 150	°C

The average chip-junction temperature, T_J, can be calculated using the following equation:

$$T_J = T_A + (P_D \cdot \Theta_{JA})$$

where:

- T_A is the ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance, which is 34 °C/W
- P_D = P_{INT} + P_{PORT}
 - P_{INT} is the chip internal power
 - P_{PORT} is the power dissipation on Input and Output pins, user determined

If P_{PORT} is neglected, an approximate relationship between P_D is:

$$P_D = K / (T_J + 273 \text{ °C})$$

And, solving first equations:

$$K = P_D \cdot (T_A + 273 \text{ °C}) + \Theta_{JA} \times P_D^2$$

K is a constant for the particular case, which can be determined through last equation by measuring P_D at equilibrium, for a known T_A.

Using this value of K, the value of P_D and T_J can be obtained by solving first and second equation, iteratively for any value of T_A.

10.2 DC electrical characteristics

Supply voltage specifications.

The recommended operating conditions are listed in the [Table 25](#):

Table 25. Recommended operating condition

Symbol	Description	Min	Typ	Max	Unit
V _{DD} core	Supply voltage core	1.14	1.2	1.26	V
V _{DD} I/O	Supply voltage I/O	3	3.3	3.6	V
V _{DD} PLL	Supply voltage PLL	2.25	2.5	2.75	V
V _{DD} OSC	Supply voltage oscillator	2.25	2.5	2.75	V
V _{DD} DDR	Supply voltage DRAM interface	1.7	1.8	1.9	V
V _{DD} RTC	Supply voltage RTC	1.2	1.5	1.8	V
T _{OP}	Operating temperature	-40		85	°C

10.3 General purpose I/O characteristics

The 3.3 V I/Os are compliant with JEDEC standard JESD8b

Table 26. Low voltage TTL DC input specification (3V < V_{DD} < 3.6V)

Symbol	Description	Test condition	Min	Max	Unit
V _{il}	Low level input voltage			0.8	V
V _{ih}	High level input voltage		2		V
V _{hyst}	Schmitt trigger hysteresis		300	800	mV

Table 27. Low voltage TTL DC output specification (3V < V_{DD} < 3.6V)

Symbol	Description	Test condition	Min	Max	Unit
V _{ol}	Low level output voltage	I _{ol} = XmA ⁽¹⁾		0.3	V
V _{oh}	High level output voltage	I _{oh} = -XmA ⁽¹⁾	V _{DD} - 0.3		V

1. For the max current value (XmA) refer to [Section 6: Pins description](#).

Table 28. Pull-up and pull-down characteristics

Symbol	Description	Test condition	Min	Max	Unit
R _{pu}	Equivalent pull-up resistance	V _i = 0V	29	67	KΩ
R _{pd}	Equivalent pull-down resistance	V _i = V _{dde3V3}	29	103	KΩ

10.4 LPDDR and DDR2 pad electrical characteristics

Table 29. DC characteristics

Symbol	Description	Test condition	Min	Max	Unit
V_{il}	Low level input voltage	SSTL18	-0.3	$V_{ref}-0.125$	V
V_{ih}	High level input voltage	SSTL18	$V_{ref}+0.125$	$V_{dde1}V8+0.3$	V
V_{hyst}	Input voltage hysteresis		200		mV

Table 30. Driver characteristics

Symbol	Description	Test condition	Min	Typ	Max	Unit
R_o	Output impedance			45		Ω

Table 31. On die termination

Symbol	Description	Test condition	Min	Typ	Max	Unit
RT1	Termination value of resistance for on die termination			75		Ω
RT2	Termination value of resistance for on die termination			150		Ω

Table 32. Reference voltage

Symbol	Description	Test condition	Min	Typ	Max	Unit
V_{REFIN}	Voltage applied at core/pad		0.49 * V_{dde}	0.500 * V_{dde}	0.51 * V_{dde}	V

10.5 Power up sequence

The only requirement is that the various power supplies reach the correct range in less than 10 ms.

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10.6 PowerGood

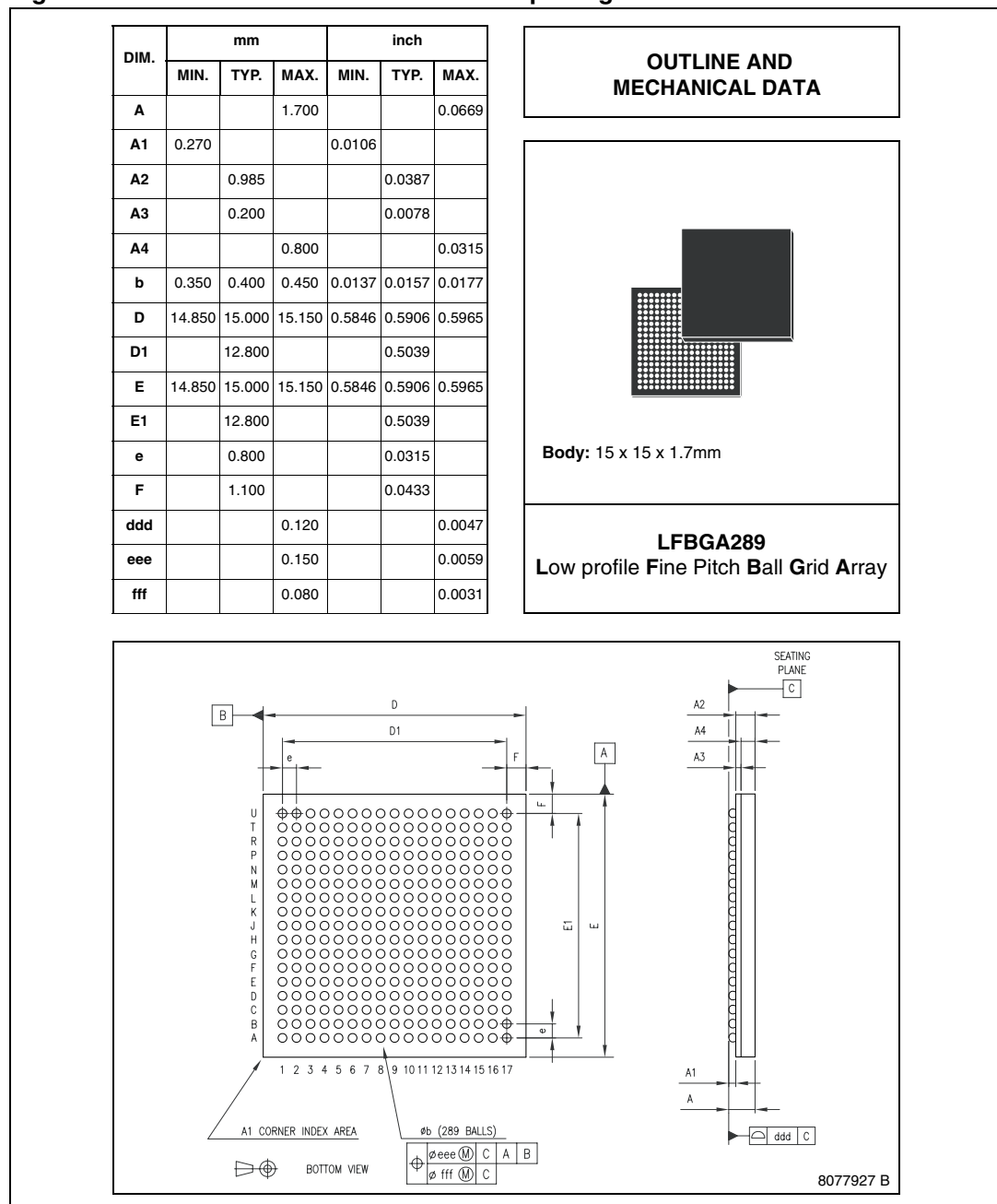
The PowerGood signal should remain active for at least 10 ms after all the power supplies are in the correct range and should become active within 10 μ s of any of the power supplies going out of the correct range.

11 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 20. LFBGA289 mechanical data and package dimensions



Order code

SPEAR-09-B042

12 Order code

Table 33. Ordering information

Order code	Package	Packing
SPEAR-09-B042	LFBGA289 (15x15mm)	Tray

13 Revision history

Table 34. Document revision history

Date	Revision	Changes
20-May-2008	1	Initial release.

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