DATA SHEET

旭曜科技
ORISE TECH

SPFD5408A

720-channel 6-bit Source Driver with System-on-chip for Color Amorphous TFT-LCDs

Preliminary

MAR. 06, 2007

Version 0.3

Table of Contents

720-CHANNEL DRIVER WITH SYSTEM-ON-CHIP (SOC) FOR COLOR AMORPHOUS TFT LCD

1. GENERAL DESCRIPTION

The SPFD5408A, a 262144-color System-on-Chip (SoC) driver LSI designed for small and medium sizes of TFT LCD display, is capable of supporting up to 240xRGBx320 in resolution which can be achieved by the designated RAM for graphic data. The 720-channel source driver has true 6-bit resolution, which generates 64 Gamma-corrected values by an internal D/A converter.

The SPFD5408A is able to operate with low IO interface power supply up to 1.6V and incorporate with several charge pumps to generate various voltage levels that form an on-chip power management system for gate driver and source driver.

The built-in timing controller in SPFD5408A can support several interfaces for the diverse request of medium or small size portable display. SPFD5408A provides system interfaces, which include 8-/9-/16-/18-bit parallel interfaces and serial interface (SPI), to configure system. Not only can the system interfaces be used to configure system, they can also access RAM at high speed for still picture display. In addition, the SPFD5408A incorporates 6, 16, and 18-bit RGB interfaces for picture movement display. The SPFD5408A also supports a function to display eight colors and a standby mode for power control consideration.

2. FEATURE

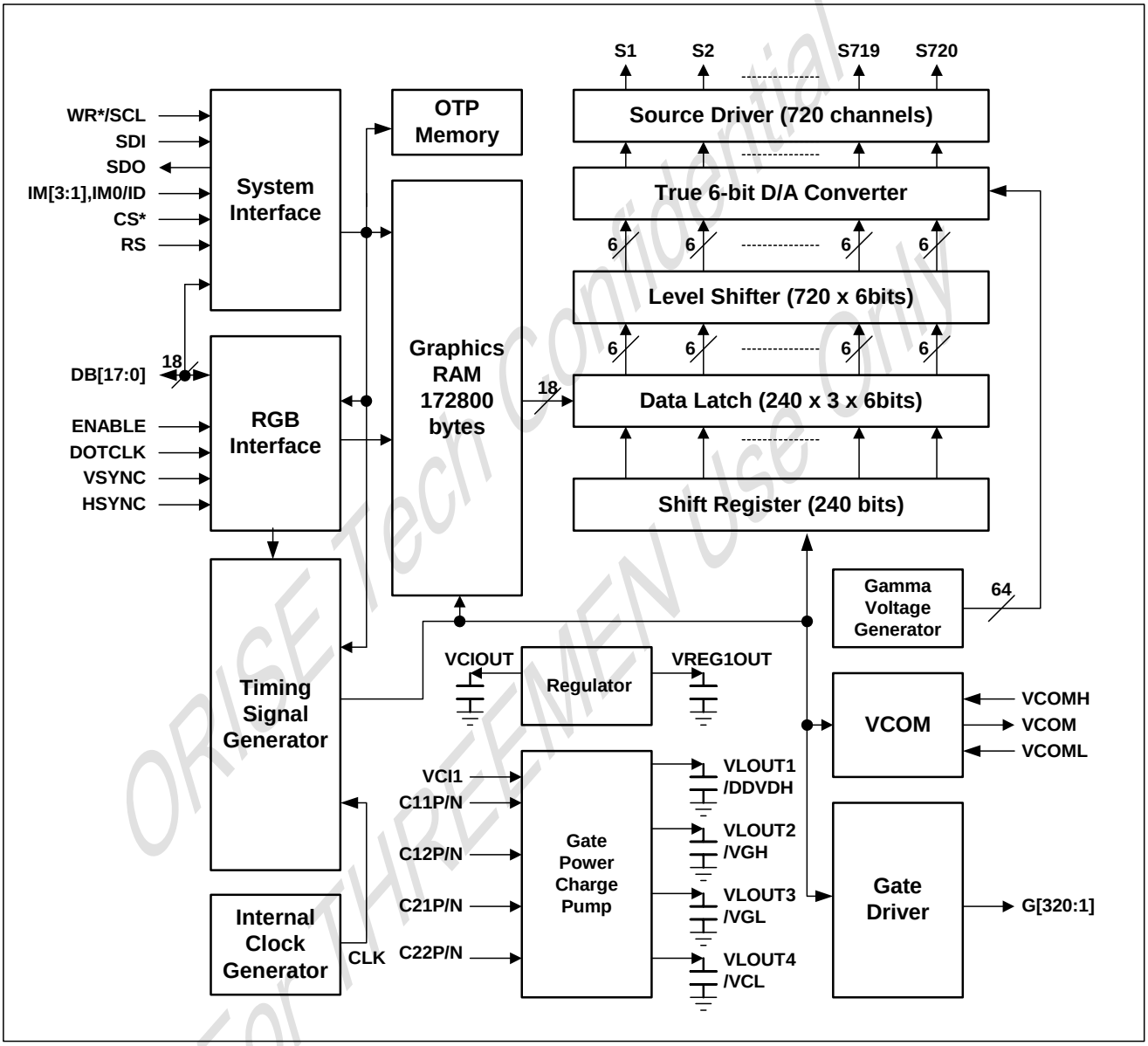
- One-chip solution for amorphous TFT-LCD.
- Supports resolution up to 240xRGBx320, incorporating a 720-channel source driver and a 320-channel gate driver
- Outputs 64 γ -corrected values using an internal true 6-bit resolution D/A converter to achieve 262K colors
- Built-in 172800 bytes internal RAM
- Line Inversion AC drive / frame inversion AC drive
- System interfaces
  - High-speed interfaces to 8-, 9-, 16-, and 18-bit parallel ports
  - Serial Peripheral Interface (SPI)
- Interfaces for moving picture display
  - 6-, 16-, and 18-bit RGB interfaces
- Diverse RAM accessing for functional display
  - Window address function to display at any area on the screen via a moving picture display interface
  - Window address function to limit the data rewriting area and reduce data transfer
  - Moving and still picture can display at the same time
  - Vertical scrolling function
  - Partial screen display
- Power supply
  - Logic power supply voltage (Vcc): 2.5 ~ 3.3 V
  - I/O interface supply voltage (IOVcc): 1.65 ~ 3.3 V
  - Analog power supply voltage (Vci): 2.5 ~ 3.3 V
- Resize function(x 1/2, x 1/4)
- On-chip power management system
  - Power saving mode (standby / 8-color mode, etc)
  - Low power consumption structure for source driver.
- Built-in Charge Pump circuits
  - Source driver voltage level : DDVDH-GND=4.5V ~ 6V.
  - Gate driver voltage level (VGH, VGL)
    VGH = 10.0V ~20.0V
    VGL = -4.5V ~ -13.5V
    VGH – VGL < 28.0V
  - Built-in internal oscillator and hardware reset
- Built–in One-Time-Programming (OTP) function for VCOM amplitude and VcomH voltage adjustment. User identification code,4 bits, VCOM level adjustment, 5 bits x 2 sets

3. ORDERING INFORMATION

Product Number	Package Type
SPFD5408A-C	Chip Form with Gold Bump

4. BLOCK DIAGRAM

4.1. Block Function



4.2. System Interface

4.2.1. The SPFD5408A supports three high-speed system interfaces:

1. 80-system high-speed interfaces with 8-, 9-, 16-, 18-bit parallel ports.
2. Serial Peripheral Interface (SPI).

The SPFD5408A has a 16-bit index register (IR) and two 18-bit data registers, a write-data register (WDR) and a read-data register (RDR). The IR register is used to store index information from control registers. The WDR register is used to temporarily store data to be written for register control and internal GRAM. The RDR register is used to temporarily store data read from the GRAM. When graphic data is written to the internal GRAM from MCU/graphic engine, the data is first written to the WDR and then automatically written to the internal GRAM in internal operation. When graphic data read operation is executed, graphic data is read via the RDR from the internal GRAM. Therefore, invalid data is first read out to the data bus when the SPFD5408A executes the 1st read operation. Thus, valid data can be read out after the SPFD5408A executes the 2nd read operation.

4.2.2. External Display Interface

The SPFD5408A supports external RGB interface for picture movement display.

The SPFD5408A allows switching between one of the external display interfaces and the system interface via pin configuration so that the optimum interface is selected for still / moving picture displayed on the screen.

When the RGB interface is chosen, display operations are synchronized with external supplied signals, VSYNC, HSYNC, and DOTCLK. Moreover, valid display data (DB17-0) is written to GRAM, which synchronized with signal (DE) enabling.

4.2.3. Address Counter (AC)

SPFD5408A features an Address Counter (AC) giving an address to the internal GRAM. The address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

4.2.4. Graphics RAM (GRAM)

SPFD5408A features a 172800-byte (240 x 320 x 18 / 8) Graphic RAM (GRAM).

4.2.5. Grayscale Voltage Generating Circuit

SPFD5408A has true 6-bit resolution D/A converter, which generates 64 Gamma-corrected values and cooperates with OP-AMP structure to enhance display quality. The grayscale voltage can be adjusted by grayscale data set in the γ-correction register.

4.2.6. Timing Controller

SPFD5408A has a timing controller, which can generate a timing signal for internal circuit operation such as gate output timing, RAM accessing timing, etc.

4.2.7. Oscillator (OSC)

The SPFD5408A also features an internal oscillator to generate RC oscillation with an internal resistor. In standby mode, RC oscillation is halted to reduce power consumption.

4.2.8. Source Driver Circuit

SPFD5408A consists of a 720-output source driver circuit (S1 ~ S720). Data in the GRAM are latched when the 720th bit data is input. The latched data controls the source driver and generates a drive waveform.

4.2.9. Gate Driver Circuit

SPFD5408A consists of a 320-output gate driver circuit (G1~G320). The gate driver circuit outputs gate driver signals at either VGH or VGL level.

4.2.10. LCD Driving Power Supply Circuit

The LCD driving power supply circuit generates the voltage levels DDVDH, VLOUT1, VLOUT2 and VCOM for driving an LCD. All this voltages can be adjusted by register setting.

5. SIGNAL DESCRIPTIONS

<table>
<tr><th>Signal</th><th>Pin No.</th><th>I/O</th><th>Connected with</th><th>Function</th></tr>
<tr><td colspan="5">System Configuration Input Signal</td></tr>
<tr><td>IM3~1, IM0/ID</td><td>4</td><td>I</td><td>GND/ IOVcc</td><td>Select a mode to interface to an MPU. In serial interface operation, the IM0 pin is used to set the ID bit of device code.
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0/ I D</th><th>Interface Mode</th><th>DB Pin</th><th>Colors</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80-system 16-bit interface</td><td>DB17-10, DB8-1</td><td>262,144 see Note 1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>80-system 8-bit interface</td><td>DB17-10</td><td>262,144 see Note 2</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>*(ID)</td><td>Clock synchronous serial interface</td><td>-</td><td>65,536</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80-system 18-bit interface</td><td>DB17-0</td><td>262,144</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>80-system 9-bit interface</td><td>DB17-9</td><td>262,144</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
</table>
Notes: 1. 65,536 colors in one transfer mode
2. 65,536 colors in two transfers mode</td></tr>
<tr><td>/RESET</td><td>1</td><td>I</td><td>MPU or external RC circuit</td><td>RESET pin. This is an active low signal.</td></tr>
<tr><td colspan="5">Interface input Signals</td></tr>
<tr><td>/CS</td><td>1</td><td>I</td><td>MPU</td><td>Chip select signal.
Low: the SPFD5408A is accessible
High: the SPFD5408A is not accessible
Must connect to the GND or IOVCC level when not used.
This pin has weak pull high/low resistors and can be modified to high / low by metal layer change for customer’s request.</td></tr>
<tr><td>RS</td><td>1</td><td>I</td><td>MPU</td><td>Register select signal.
Low: Index register or internal status is selected.
High: Control register is selected.
Must connect to the GND or IOVCC level when not used.
This pin has weak pull high/low resistors and can be modified to high / low by metal layer change for customer’s request.</td></tr>
<tr><td>(/WR) / (SCL)</td><td>1</td><td>I</td><td>MPU</td><td>(A) In 80-system interface mode, a write strobe signal can be input via this pin and initializes a write operation when the signal is low.
(B) In SPI mode, served as a synchronizing clock signal.</td></tr>
</table>

<table>
<tr><th>Signal</th><th>Pin No.</th><th>I/O</th><th>Connected with</th><th>Function</th></tr>
<tr><td></td><td></td><td></td><td></td><td>This pin has weak pull high/low resistors and can be modified to high / low by metal layer change for customer’s request.</td></tr>
<tr><td>/RD</td><td>1</td><td>I</td><td>MPU</td><td>In 80-system interface mode, a read strobe signal can be input via this pin and initializes a read operation when the signal is low.
Must connect to the GND or IOVCC level when not in use.
This pin has weak pull high/low resistors and can be modified to high / low by metal layer change for customer’s request.</td></tr>
<tr><td>SDI</td><td>1</td><td>I</td><td>MPU</td><td>Series Data is the input on the rising edge of the SCL signal in SPI mode.
Must connect to the GND or IOVCC level when not in use.
This pin has weak pull high/low resistors and can be modified to high / low by metal layer change for customer’s request.</td></tr>
<tr><td>SDO</td><td>1</td><td>O</td><td>MPU</td><td>Series Data is the output on the rising edge of the SCL signal in SPI mode.</td></tr>
<tr><td>DB0-DB17</td><td>1</td><td>I/O</td><td>MPU</td><td>Served as an 18-bit parallel bi-directional data bus. Data bus pin assignment corresponding to different modes are summarized in the table:
<table>
<tr><th>Mode</th><th>Pin Assignment</th></tr>
<tr><td>8-bit system interface</td><td>DB17-DB10</td></tr>
<tr><td>9-bit system interface</td><td>DB17-DB9</td></tr>
<tr><td>16-bit system interface</td><td>DB17-DB10, DB8-DB1</td></tr>
<tr><td>18-bit system interface</td><td>DB17-DB0</td></tr>
<tr><td>18-bit External (RGB) interface</td><td>DB17-DB12</td></tr>
<tr><td>16-bit External (RGB) interface</td><td>DB17-10, DB8-DB1</td></tr>
<tr><td>18-bit External (RGB) interface</td><td>DB17-DB0</td></tr>
</table>
Must connect to the GND or IOVCC level when not in use.
These pins have weak pull high/low resistors and can be modified to high / low by metal layer change for customer’s request.</td></tr>
<tr><td>VSYNC</td><td>1</td><td>I</td><td>MPU</td><td>In external interface mode, served as a vertical synchronize signal input
Must connect to the IOVCC level when not in use.
This pin has weak pull high/low resistors and can be modified to high / low by metal layer change for customer’s request.</td></tr>
<tr><td>HSYNC</td><td>1</td><td>I</td><td>MPU</td><td>In external interface mode, served as a horizontal synchronized signal input
Must connect to the IOVCC level when not used.
This pin has weak pull high/low resistors and can be modified to high / low by metal layer change for customer’s request.</td></tr>
<tr><td>ENABLE</td><td>1</td><td>I</td><td>MPU</td><td>In external interface mode, polarity of ENABLE signal is synchronized with valid graphic data input.
Low: Valid data on DB17-DB0
High: Invalid data on DB17-DB0
Moreover, setting EPL bit can change the polarity of the ENABLE signal.
Must connect to the GND or IOVCC level when not in use.
This pin has weak pull high/low resistors and can be modified to high / low by metal layer change for customer’s request.</td></tr>
<tr><td>DOTCLK</td><td>1</td><td>I</td><td>MPU</td><td>In external interface mode, served as a dot clock signal.
When DPL = “0”: Input data on the rising edge of DOTCLK
When DPL = “1”: Input data on the falling edge of DOTCLK
It is fixed to the IOVcc level when not in use.</td></tr>
</table>

Signal	Pin No.	I/O	Connected with	Function
				This pin has weak pull high/low resistors and can be modified to high / low by metal layer change for customer's request.
FMARK	1	O	MPU	Frame head pulse signal, which is used when writing data to the internal RAM.
Charge Pump and Power Supply Signal				
C11P/N, C12P/N C13P/N C21P/N, C22P/N C23P/N	12	-	Step-up capacitor	Connect boost capacitors for the internal DC/DC converter circuit to these pins. Leave the pins open when DC/DC converter circuits are not used.
VCIOUT	1	O	Stabilizing capacitor, VCI1	Output voltage from the step-up circuit 1, generated from the reference voltage. VC bits set the output factor. Make sure to connect to stabilizing capacitor.
VCI1	1	I/O	VCIOUT	Reference voltage of step-up circuit 1. Make sure the output voltage levels from VLOUT1, VLOUT2, and VLOUT3 do not exceed the respective setting ranges.
VLOUT1	1	O	Stabilizing capacitor, DDVDH	Output voltage from the step-up circuit 1, generated from VCI1. The step-up factor is set by BT. Make sure to connect to stabilizing capacitor. VLOUT1 = 4.5V ~ 6.0V
DDVDH	1	I	VLOUT1	Power supply for the source driver liquid crystal drive unit and VCOM drive. Connect to VLOUT1. DDVDH = 4.5V ~ 6.0V
VLOUT2	1	O	Stabilizing capacitor, VGH	Output voltage from the step-up circuit 2, generated from VCI1 and DDVDH. The step-up factor is set by BT. Make sure to connect to stabilizing capacitor. VLOUT2 = max 15.0V
VGH	1	I	VLOUT2	Liquid crystal drive power supply. Connect to VLOUT2.
VLOUT3	1	O	Stabilizing capacitor, VGL	Output voltage from the step-up circuit 2, generated from VCI1 and DDVDH. The step-up factor is set by BT bits. Make sure to connect to stabilizing capacitor. VLOUT3 = min –12.5V
VGL	1	I	VLOUT3	Liquid crystal drive power supply. Connect to VLOUT3.
VCL	1	O	Stabilizing capacitor	VCOML drive power supply. Make sure to connect to stabilizing capacitor. VCL = -1.9V ~ -3.0V
VCILVL		I	Reference power supply	VCILVL must be at the same electrical potential as VCI. VCILVL = 2.5V ~ 3.3V. Connect to external power supply. In case of COG, connect to VCI on the FPC to prevent noise.
VPP2		I	Power supply or open	OTP power supply.
Source/Gate Driver and VCOM Signals				
G1~G320	320	O	LCD	Output gate driver signals, which has the swing from VGH to VGL
S1~S720	720	O	LCD	Output source driver signals. The D/A converted 64-gray-scale analog voltage is output.
VREG1 OUT	1	O	Stabilizing capacitor	Output voltage generated from the reference voltage (VCILVL or VCIR). The factor is determined by instruction (VRH bits). VREG1OUT is used for (1) source driver grayscale reference voltage, (2) VCOMH level reference voltage, and (3) VCOM amplitude reference voltage. Connect to a stabilizing capacitor when in use. VREG1OUT = 4.0V ~ (DDVDH – 0.5)V

Signal	Pin No.	I/O	Connected with	Function
VCOM	1	O	TFT panel common electrode	Power supply to TFT panel's common electrode. VCOM alternates between VCOMH and VCOML. The alternating cycle is set by internal register. Also, the VCOM output can be started and halted by register setting.
VCOMH	1	O	Stabilizing capacitor	The High level of VCOM amplitude. The output level can be adjusted by either external resistor (VCOMR) or electronic volume. Make sure to connect to stabilizing capacitor.
VCOML	1	O	Stabilizing capacitor	The Low level of VCOM amplitude. The output level can be adjusted by instruction (VDV bits). VCOML = (VCL+0.5)V ~ 0V. Make sure to connect to stabilizing capacitor.
VCOMR	1	I	Variable resistor or open	Connect a variable resistor when adjusting the VCOMH level between VREG1OUT and GND.
VGS	1	I	GND	Reference level for the grayscale voltage generating circuit.
VCC	1	-	Power supply	Internal logic power: VCC = 2.5V ~3.3V. VCC > IOVCC.
GND	1	-	Power supply	Internal logic GND: GND = 0V.
RGND	1	-	Power supply	Internal RAM GND. RGND must be at the same electrical potential as GND. In case of COG, connect to GND on the FPC to prevent noise.
VDD	1	O	Stabilizing capacitor	Internal logic regulator output, which is used as the power supply to internal logic. Connect a stabilizing capacitor.
IOVCC	1	-	Power supply	Power supply to the interface pins: RESET*, CS*, WR, RD*, RS, DB17-0, VSYNC, HSYNC, DOTCLK, ENABLE. IOVCC = 1.65V ~ 3.3V. VCC ≥IOVCC. In case of COG, connect to VCC on the FPC if IOVCC=VCC, to prevent noise.
IOGND	1	-	Power supply	GND for the interface pins: RESET*, CS*, WR, RD*, RS, DB17-0, VSYNC, HSYNC, DOTCLK, ENABLE. IOGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
AGND	1	-	Power supply	Analog GND (for logic regulator and liquid crystal power supply circuit): AGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
VCI	1	I	Power supply	Power supply to the liquid crystal power supply analog circuit. Connect to an external power supply of 2.5V ~ 3.3V.
VCILVL	1	I	Reference power supply	VCILVL must be at the same electrical potential as VCI. VCILVL = 2.5V ~ 3.3V. Connect to external power supply. In case of COG, connect to VCI on the FPC to prevent noise.
Misc. Signal				
V0T, V31T	2	I/O	Open	Test pins. Leave them open. SPFD5408A use these pins to do self-test. No any signal on panel can cross these pins, otherwise function fail.
VTEST	1	I/O	Open	Test pins. Leave them open. SPFD5408A use these pins to do self-test. No any signal on panel can cross these pins, otherwise function fail.
VREFC	1	I/O	Open	Test pins. Leave them open.
VREF	1	I/O	Open	Test pins. Leave them open.
VDDTEST	1	I/O	Open	Test pins. Leave them open.
VREFD	1	I/O	Open	Test pins. Leave them open. SPFD5408A use these pins to do self-test. No any signal on panel can cross these pins, otherwise function fail.
VMON	1	I/O	Open	Test pins. Leave them open. SPFD5408A use these pins to do self-test. No any signal on panel can cross these pins, otherwise function fail.
TESTA5	1	I/O	Open	Test pins. Leave them open. SPFD5408A use these pins to do self-test. No any signal on panel can cross these pins, otherwise function fail.

Signal	Pin No.	I/O	Connected with	Function
IOVCCDUM1~2	2	I/O	Open	Test pins. Leave them open.
VCCDUM1	1	I/O	Open	Test pins. Leave them open.
IOGNDDUM1~3	3	I/O	Open	Test pins. Leave them open.
OSC1DUM1~4	4	I/O	Open	Test pins. Leave them open. SPFD5408A use these pins to do self-test. No any signal on panel can cross these pins, otherwise function fail.
OSC2DUM1~2	2	I/O	Open	Test pins. Leave them open. SPFD5408A use these pins to do self-test. No any signal on panel can cross these pins, otherwise function fail.
AGNDDUM1~4	4	I/O	Open	Test pins. Leave them open.
DUMMYR1~10	10	I/O	Open	Test pins. Leave them open. SPFD5408A use these pins to do self-test. No any signal on panel can cross these pins, otherwise function fail.
VGLDMY1~4	4	I/O	Open	Test pins. Leave them open.
TESTO1~38	38	I/O	Open	Test pins. Leave them open.
TEST1~2	2	I	IOGND	Test pins. Connect to IOGND.
TEST3	1	I	IOVCC	Test pins. Connect to IOVCC.
TEST4	1	I	IOVCC	Test pins. Connect to IOVCC.
TEST5	1	I	IOGND	Test pins. Connect to IOGND.
TSC	1	I	IOGND	Test pins. Connect to IOGND.
TS0~8	9	I/O	Open	Test pins. Leave them open. SPFD5408A use these pins to do self-test. No any signal on panel can cross these pins, otherwise function fail.

6. INSTRUCTIONS

6.1. Outline

The SPFD5408A supports 18-bit data bus interface to access command register to configure system. When the command register accessing is desired, sending the command information to specify which index register would be accessed and following the data to that control register. Moreover, register accessing operation should cooperate with RS, /WR, /RD signal for SPFD5408A to recognize the control instruction. And command instruction can be accomplished by using all system interfaces (18-bit, 16-bit, 9-bit, 8-bit 80 system and SPI). The corresponding pin assignment of different system interface are shown in **Figure 6-1** to **Figure 6-6**

The instruction can be categorized into 8 groups. And the 8 groups are:

1. Specify the index of register
2. Read a status
3. Display control
4. Power management Control
5. Graphics data processing
6. Set internal GRAM address
7. Transfer data to and from the internal GRAM
8. Internal grayscale γ-correction

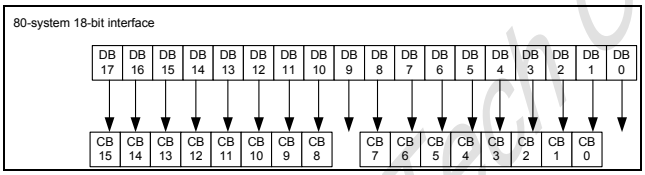


Figure 6-1

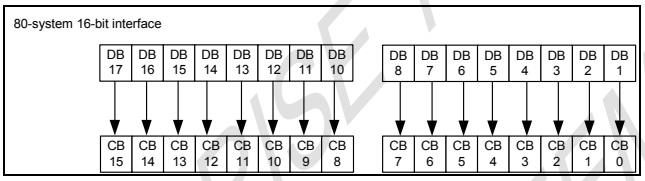


Figure 6-2

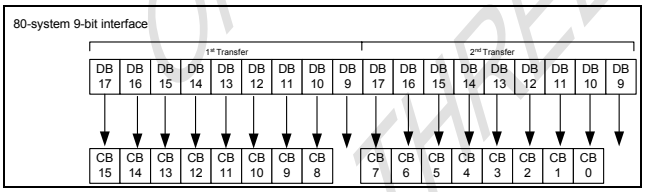


Figure 6-3

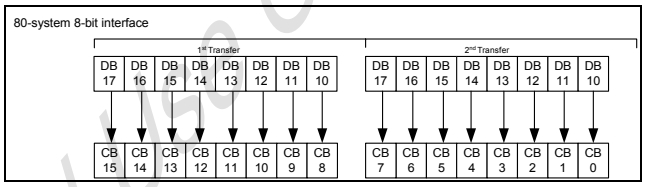


Figure 6-4

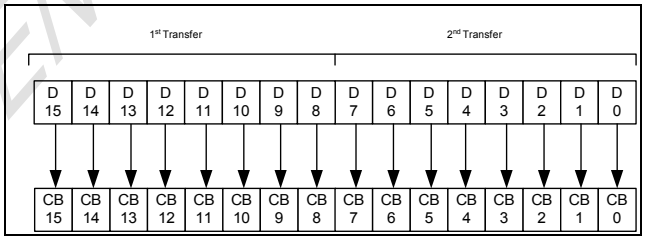


Figure 6-5

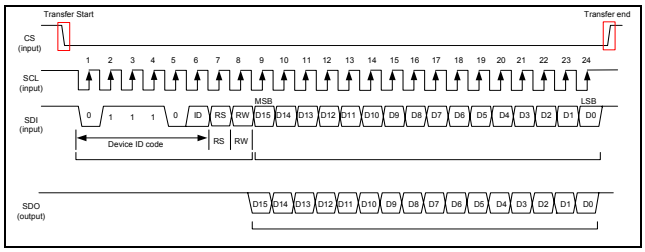


Figure 6-6

6.2. Instruction

Table 6-1 Instruction List Table

Register No	Register	Upper 8-bit								Lower 8-bit							
		CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
00h	ID Read	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1
01h	Driver Output Control	0	0	0	0	0	SM (0)	0	SS (0)	0	0	0	0	0	0	0	0
02h	LCD AC Drive Control	0	0	0	0	0	1	B/C (0)	EOR (0)	0	0	0	0	0	0	0	NW0 (0)
03h	Entry Mode	TRIREG (0)	DFM (0)	0	BGR (0)	0	0	HWM (0)	0	ORG (0)	0	I/D1 (1)	I/D0 (1)	AM (0)	0	0	0
04h	Resizing Control	0	0	0	0	0	0	RCV1 (0)	RCV0 (0)	0	0	RCH1 (0)	RCH0 (0)	0	0	RSZ1 (0)	RSZ0 (0)
07h	Display control (1)	0	0	PTDE1 (0)	PTDE0 (0)	0	0	0	BASEE (0)	0	VON (0)	GON (0)	DTE (0)	COL (0)	0	D1 (0)	D0 (0)
08h	Display control (2)	0	0	0	0	FP3 (1)	FP2 (0)	FP1 (0)	FP0 (0)	0	0	0	0	BP3 (1)	BP2 (0)	BP1 (0)	BP0 (0)
09h	Display control (3)	0	0	0	0	0	PTS2 (0)	PTS1 (0)	PTS0 (0)	0	0	PTG1 (0)	PTG0 (0)	ISC3 (0)	ISC2 (0)	ISC1 (0)	ISC0 (0)
0Ah	Display control (4)	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE (0)	FMI2 (0)	FMI1 (0)	FMI0 (0)
0Ch	External interface control (1)	0	ENC2 (0)	ENC1 (0)	ENC0 (0)	0	0	0	RM (0)	0	0	DM1 (0)	DM0 (0)	0	0	RIM1 (0)	RIM0 (0)
0Dh	Frame Maker Position	0	0	0	0	0	0	0	FMP8 (0)	FMP7 (0)	FMP6 (0)	FMP5 (0)	FMP4 (0)	FMP3 (0)	FMP2 (0)	FMP1 (0)	FMP0 (0)
0Fh	External interface control (2)	0	0	0	0	0	0	0	0	0	0	0	VSPL (0)	HSPL (0)	0	EPL (0)	DPL (0)
10h	Power Control (1)	0	0	0	SAP (0)	BT3 (0)	BT2 (0)	BT1 (0)	BT0 (0)	APE (0)	0	AP1 (0)	AP0 (0)	0	DSTB (0)	SLP (0)	0
11h	Power Control (2)	0	0	0	0	0	DC12 (0)	DC11 (0)	DC10 (0)	0	DC02 (0)	DC01 (0)	DC00 (0)	0	VC2 (0)	VC1 (0)	VC0 (0)
12h	Power Control (3)	0	0	0	0	0	0	0	0	0	0	0	PON (0)	VRH3 (0)	VRH2 (0)	VRH1 (0)	VRH0 (0)
13h	Power Control (4)	0	0	0	VDV4 (0)	VDV3 (0)	VDV2 (0)	VDV1 (0)	VDV0 (0)	0	0	0	0	0	0	0	0
17h	Power Control (5)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PSE (0)
20h	GRAM address Set Horizontal Address	0	0	0	0	0	0	0	0	AD7 (0)	AD6 (0)	AD5 (0)	AD4 (0)	AD3 (0)	AD2 (0)	AD1 (0)	AD0 (0)
21h	GRAM address Set Vertical Address	0	0	0	0	0	0	0	AD16 (0)	AD15 (0)	AD14 (0)	AD13 (0)	AD12 (0)	AD11 (0)	AD10 (0)	AD9 (0)	AD8 (0)
22h	GRAM data																
28h	NVM read data (1)	0	0	0	0	0	0	0	0	0	0	0	0	UID3 (0)	UID2 (0)	UID1 (0)	UID0 (0)
29h	NVM read data (2)	0	0	0	0	0	0	0	0	0	0	0	VCM14 (0)	VCM13 (0)	VCM12 (0)	VCM11 (0)	VCM10 (0)
2Ah	NVM read data (3)	0	0	0	0	0	0	0	0	VCMSEL(0)	0	0	VCM24 (0)	VCM23 (0)	VCM22 (0)	VCM21 (0)	VCM20 (0)
30h	γ Control (1)	0	0	0	V1RP4	V1RP3	V1RP2	V1RP1	V1RP0	0	0	0	V1RN4	V1RN3	V1RN2	V1RN1	V1RN0
31h	γ Control (2)	0	0	V2RP5	V2RP4	V2RP3	V2RP2	V2RP1	V2RP0	0	0	V2RN5	V2RN4	V2RN3	V2RN2	V2RN1	V2RN0
32h	γ Control (3)	0	0	V3RP5	V3RP4	V3RP3	V3RP2	V3RP1	V3RP0	0	0	V3RN5	V3RN4	V3RN3	V3RN2	V3RN1	V3RN0
33h	γ Control (4)	0	0	V4RP5	V4RP4	V4RP3	V4RP2	V4RP1	V4RP0	0	0	V4RN5	V4RN4	V4RN3	V4RN2	V4RN1	V4RN0
34h	γ Control (5)	0	0	V5RP5	V5RP4	V5RP3	V5RP2	V5RP1	V5RP0	0	0	V5RN5	V5RN4	V5RN3	V5RN2	V5RN1	V5RN0
35h	γ Control (6)	0	0	0	V6RP4	V6RP3	V6RP2	V6RP1	V6RP0	0	0	0	V6RN4	V6RN3	V6RN2	V6RN1	V6RN0
36h	γ Control (7)	0	0	0	V7RP4	V7RP3	V7RP2	V7RP1	V7RP0	0	0	0	V7RN4	V7RN3	V7RN2	V7RN1	V7RN0
37h	γ Control (8)	0	0	0	V8RP4	V8RP3	V8RP2	V8RP1	V8RP0	0	0	0	V8RN4	V8RN3	V8RN2	V8RN1	V8RN0
38h	γ Control (9)	0	0	0	0	V9RP3	V9RP2	V9RP1	V9RP0	0	0	0	0	V9RN3	V9RN2	V9RN1	V9RN0
39h	γ Control (10)	0	0	0	0	V10RP3	V10RP2	V10RP1	V10RP0	0	0	0	0	V10RN3	V10RN2	V10RN1	V10RN0
3Ah	γ Control (11)	0	0	0	0	V11RP3	V11RP2	V11RP1	V11RP0	0	0	0	0	V11RN3	V11RN2	V11RN1	V11RN0
3Bh	γ Control (12)	0	0	0	0	V12RP3	V12RP2	V12RP1	V12RP0	0	0	0	0	V12RN3	V12RN2	V12RN1	V12RN0
3Ch	γ Control (13)	0	0	0	0	V13RP3	V13RP2	V13RP1	V13RP0	0	0	0	0	V13RN3	V13RN2	V13RN1	V13RN0
3Dh	γ Control (14)	0	0	0	0	V14RP3	V14RP2	V14RP1	V14RP0	0	0	0	0	V14RN3	V14RN2	V14RN1	V14RN0
		0	0	0	0	V15RP3	V15RP2	V15RP1	V15RP0	0	0	0	0	V15RN3	V15RN2	V15RN1	V15RN0
		0	0	0	0	V16RP3	V16RP2	V16RP1	V16RP0	0	0	0	0	V16RN3	V16RN2	V16RN1	V16RN0
50h	Window Horzontal RAM address start	0	0	0	0	0	0	0	0	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	HSA2 (0)	HSA1 (0)	HSA0 (0)
51h	Window Horzontal RAM address start	0	0	0	0	0	0	0	0	HEA7 (1)	HEA6 (1)	HEA5 (1)	HEA4 (0)	HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (1)
52h	Window Vertical RAM address start	0	0	0	0	0	0	0	VSA8 (0)	VSA7 (0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)
53h	Window Vertical RAM address start	0	0	0	0	0	0	0	VEA8 (1)	VEA7 (0)	VEA6 (0)	VEA5 (1)	VEA4 (1)	VEA3 (1)	VEA2 (1)	VEA1 (1)	VEA0 (1)

60h	Driver Output Control	GS (0)	0	NL5 (0)	NL4 (0)	NL3 (0)	NL2 (0)	NL1 (0)	NL0 (0)	0	0	SCN5 (0)	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)
61h	Image Display Control	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL (0)	VLE (0)	REV (0)
6Ah	Vertical Scoll ing Control	0	0	0	0	0	0	0	VL8 (0)	VL7 (0)	VL6 (0)	VL5 (0)	VL4 (0)	VL3 (0)	VL2 (0)	VL1 (0)	VL0 (0)
80h	Display Position 1	0	0	0	0	0	0	0	PTDP 08 (0)	PTDP 07 (0)	PTDP 06 (0)	PTDP 05 (0)	PTDP 04 (0)	PTDP 03 (0)	PTDP 02 (0)	PTDP 01 (0)	PTDP 00 (0)
81h	GRAM start line address 1	0	0	0	0	0	0	0	PTSA 08 (0)	PTSA 07 (0)	PTSA 06 (0)	PTSA 05 (0)	PTSA 04 (0)	PTSA 03 (0)	PTSA 02 (0)	PTSA 01 (0)	PTSA 00 (0)
82h	GRAM end line address 1	0	0	0	0	0	0	0	PTEA 08 (0)	PTEA 07 (0)	PTEA 06 (0)	PTEA 05 (0)	PTEA 04 (0)	PTEA 03 (0)	PTEA 02 (0)	PTEA 01 (0)	PTEA 00 (0)
83h	Display Position 2	0	0	0	0	0	0	0	PTDP 18 (0)	PTDP 17 (0)	PTDP 16 (0)	PTDP 15 (0)	PTDP 14 (0)	PTDP 13 (0)	PTDP 12 (0)	PTDP 11 (0)	PTDP 10 (0)
84h	GRAM start line address 2	0	0	0	0	0	0	0	PTSA 18 (0)	PTSA 17 (0)	PTSA 16 (0)	PTSA 15 (0)	PTSA 14 (0)	PTSA 13 (0)	PTSA 12 (0)	PTSA 11 (0)	PTSA 10 (0)
85h	GRAM end line address 2	0	0	0	0	0	0	0	PTEA 18 (0)	PTEA 17 (0)	PTEA 16 (0)	PTEA 15 (0)	PTEA 14 (0)	PTEA 13 (0)	PTEA 12 (0)	PTEA 11 (0)	PTEA 10 (0)
90h	Panel interface Control 1	0	0	0	0	0	0	DIVI1 (0)	DIVI0 (0)	0	0	0	RTNI4 (1)	RTNI3 (0)	RTNI2 (0)	RTNI1 (0)	RTNI0 (0)
92h	Panel Interface Control 2	0	0	0	0	0	NOWI2(0)	NOWI 1(0)	NOWI 0(0)	0	0	0	0	0	0	0	0
93h	Panel Interface Control 3	0	0	0	0	0	0	VEQW11(0)	VEQW10(0)	0	0	0	0	0	MCPI2 (0)	MCPI1 (0)	MCPI0 (0)
95h	Panel Interface Control 4	0	0	0	0	0	0	DIVE1(0)	DIVE0 (0)	0	0	RTNE5 (0)	RTNE4 (1)	RTNE3 (1)	RTNE2 (1)	RTNE1 (1)	RTNE0 (0)
97h	Panel Interface Control 5	0	0	0	0	NOW E3(0)	NOWE2(0)	NOW E1(0)	NOW E0(0)	0	0	0	0	0	0	0	0
98h	Panel Interface Control 6	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPE2 (0)	MCPE1 (0)	MCPE0 (0)
A4h	Calibration control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CALB (0)

The following are detailed explanations of instructions with illustrations of instruction bits (CB15-0) assigned to each interface.

6.2.1. Index Register (IR)

R/W	RS	CB15	CCB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	0	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the index (R00h ~ RFFh) of a control register. The index range is from “000_0000” to “111_1111” in binary format.

6.2.2. ID Read Register (SR)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R	0	0	1	0	1	0	1	0	0	0	0	0	0	1	0	0	0

The IC code of SPFD5408A can be accessed by read operation. ‘5408H can be read out when read ID operation is exectured.

6.2.3. Driver Output Control Register (R01h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0

SS: Shift direction of the source driver output selection.

When SS = “0”, source driver shift from S1 to S528. When SS = “1”, source driver shift from S528 to S1. Moreover, SS can cooperate with BGR for different color filter configuration of LCD panel. The combination of SS and BGR bit are summarized at **Table 6-**2.

Table 6-2

SS=0;BGR=0;	S1	S2	S3	▶	S526	S527	S528
SS=0;BGR=1;	S1	S2	S3	▶	S526	S527	S528
SS=1,BGR=0;	S1	S2	S3	◀	S526	S527	S528
SS=1,BGR=1;	S1	S2	S3	◀	S526	S527	S528

SM: Set the scan mode of the gate driver output. Moreover, SM can cooperate with GS for different LCD panel gate line layout. The combination of GS and SM bit are summarized at **Table 6-**3

Table 6-3

SM	GS	Shift Direction (begin,…..,end)
0	0	G1, G2, G3, G4……G317, G318, G319, G320
0	1	G320, G319, G318, G317……G4, G3, G2, G1
1	0	G1, G3, G5, …G317, G319, …G2, G4,.. G318, G320
1	1	G320, G318, G316,..G4, G2, ..G319, G317,...G3, G1

6.2.4. LCD Driving Waveform Control (R02h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	1	B/C	EOR	0	0	0	0	0	0	0	NW0

NW0: SPFD5408A provides 1-line inversion for Vcom.

EOR: In N-line inversion, in order to insure that every pixel can avoid DC bias, SPFD5408A provides EOR (EOR=1) to force Vcom to toggle at the beginning of the frame.

B/C: This bit .is to set the Vcom toggle at frame rate format of N-line inversion format.
B/C=0: Frame inversion.
B/C=1: 1-line inversion.

6.2.5. Entry Mode (R03h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	TRIREG	DFM	0	BGR	0	0	HWM	0	ORG	0	I/D1	I/D0	AM	0	0	0

Table 6-4

Operation mode	ID1	ID0	AM	Function
Mode 1	0/1	0	0	Replace horizontal data
Mode2	0/1	1	1	Replace vertical data
Mode3	0/1	0	0	Conditionally replace horizontal data
Mode	0/1	1	1	Conditionally replace vertical data

AM: To set the update direction when writing data to GRAM. If AM=1, data will write in vertical direction. If AM=0, data will write in horizontal direction. Moreover, if a fixed window GRAM accessing is desired, the writing direction can be set by ID1-0 and AM bits.

I/D1-0: To specify address counter increment /decrement automatically function while GRAM is accessing. I/D[0] indicates the increment or decrement in horizontal direction. I/D[1] indicates the increment or decrement in vertical direction.
I/D[0]=0: decrement in horizontal direction automatically
I/D[0]=1: increment in horizontal direction automatically
I/D[1]=0: decrement in vertical direction automatically
I/D[1]=1: increment in vertical direction automatically
ID[1-0] setting can cooperate with Am bit to set the data updating direction.

ORG: SPFD5408A provides the option of start address definition when window function is selected.
ORG=0: RAM address setting (R20h, R21h) should set to the window start address, as normal operation case.
ORG=1: RAM address setting (R20h, R21h) should set to (00000h) no matter where the window start address is. In this case, the window start postion is treated as (00000h), regardless the physical location in GRAM.

HWM: SPFD5408A provides a high speed GRAM accessing mode that updated GRAM data in 1-line unit. Be aware that data can be written to GRAM if accessing GRAM operation is halted before writing complete data for 1-line. Make sure the AMis set to “0”, when HWM function is set to “1”.

BGR: To set the order of RGB dot location in GRAM.
BGR=0: same assignment of RGB allocation of WM17-0
BGR=1: inverse assignment of RGB allocation of WM17-0

DFM: In combination with TRIREG setting to set the different data transfer mode.

TRIREG: to set 1–3 time transfer mode for system interface. TRI bit should cooperate with DFM1-0 to meet the specific transfer mode.
For 8-bit databus interface mode:
TRIREG=0: 2 time transfer mode for 16-bit GRAM data.
TRIREG=1: 3 time transfer mode for 16-bit GRAM data
For 16-bit databus interface mode:
TRIREG=0: 1 time transfer mode for 16-bit GRAM data.
TRIREG=1: 2 time transfer mode for 16-bit GRAM data
Note: Set TRIREG=0, when using neither 8-bit nor 16-bit.

6.2.6. Scalling Control register (R04h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	RCV1	RCV0	0	0	RCH1	RCH0	0	0	RSZ1	RSZ0

RSZ [1:0]: SPFD5408A provides scalling factor to give the display more flexibility to show different picture size. For detail, refer to “Scalling function”.

RSZ1	RSZ0	Scalling Factor
0	0	No Scalling
0	1	1/2 times
1	0	Setting Disable
1	1	1/4 times

RCH [1:0]: To set the surplus pixel number in horizontal direction when scalling mode is selected. When scalling mode is not selected, make sure RCH[1:0]= “00”

RCH1	RCH0	Surplus pixel number in Horzontal direction
0	0	0 Pixel
0	1	1 Pixels
1	0	2 Pixels
1	1	3 Pixels

RCH [1:0]: To set the surplus pixel number in Vertical direction when scalling mode is selected. When scalling mode is not selected, make sure RCV[1:0]= “00”

RCV1	RCV0	Surplus pixel number in Vertical direction
0	0	0 Pixel
0	1	1 Pixel
1	0	2 Pixels
1	1	3 Pixels

6.2.7. Display Control (R07h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	PTDE1	PTDE0	0	0	0	BASEE	0	VON	GON	DTE	COL	0	D1	D0

D1-0: To set the internal operation, source driver output and VCOM output function. When D1-0=00; SPFD5408A is set to standby mode. The combination of D1-0 and AM bit is summarized at **Table 6-5**.

Table 6-5

D1	D0	BASEE	Source, VCOM output	Internal Operation	FLM
0	0	*	GND	Terminated	OFF
0	1	*	GND	Normal Operation	ON
1	0	*	Non-lit display	Normal Operation	ON
1	1	0	Non-lit display	Normal Operation	ON
		1	Normal display	Normal Operation	ON

COL: 8-color mode selection. When CL=1 SPFD5408A enter to 8-color mode. When CL=0, SPFD5408A is in normal operation mode.

DTE, GON: Specify the high/low level of gate driver output signal. The combination of DTE and GON bit is summarized at **Table 6-6**.

Table 6-6

APE	DTE	GON	Gate Output
0	*	*	VGL(=GND)
1	0	0	VGL
	0	1	VGL
	1	0	VGL
	1	1	VGH/VGL

BASEE: To enable Base image display

BASEE	
0	(1) Non-lit display (2) Partial image display
1	Base image is display on the LCD

PTDE1-0: To set the partial-display enables function.

PTDE [0]: "0" Partial image 1 display "Off".
"1" Partial image 1 display "On".

PTDE [1]: "0" Partial image 2 display "Off".
"1" Partial image 2 display "On".

VON: To Control VCOM output signal. The combination of APE, AP[1:0] and VON bit is summarized at **Table 6-67**

Table 6-7

APE	AP [1:0]	VON	VCOM Output
0	*	*	GND
1	0	0	GND
	0	1	Setting disable
	1~3	0	VCOML
	1~3	1	VCOMH/VCOML

6.2.8. Display Control 2 (R08h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0

FP3-0: Set the amount of blank period of front porch

BP3-0: Set the amount of blank period of back porch

Table 6-8 summarized the function of FP3-0/BP3-0 setting.

When setting this register, make sure that:

BP + FP ≤ 16 lines

FP ≥ 2 lines

BP ≥ 2 lines

In external display interface mode, a back porch (BP) period starts on the falling edge of the VSYNC signal, followed by a display operation period. After driving the number of lines set with NL bits, a front porch period starts. After the front porch period, a blank period continues until the next input of VSYNC signal. Be aware that different interface mode, has different BP/ FP setting. **Table 6-9** summarized the setting for each interface mode.

Table 6-8

FP3	FP2	FP1	FP0	Number of lines for the Front Porch
BP3	BP2	BP1	BP0	Number of lines for the Back Porch
0	0	0	0	Setting disabled
0	0	0	1	Setting disabled
0	0	1	0	2 lines
0	0	1	1	3 lines
0	1	0	0	4 lines
0	1	0	1	5 lines
0	1	1	0	6 lines

FP3	FP2	FP1	FP0	Number of lines for the Front Porch
BP3	BP2	BP1	BP0	Number of lines for the Back Porch
0	1	1	1	7 lines
1	0	0	0	8 lines
1	0	0	1	9 lines
1	0	1	0	10 lines
1	0	1	1	11 lines
1	1	0	0	12 lines
1	1	0	1	13 lines
1	1	1	0	14 lines
1	1	1	1	Setting disabled

Table 6-9

Operation of Internal clock	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP ≤ 16 lines
RGB interface	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP ≤ 16 lines
VSYNC interface	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP = 16 lines

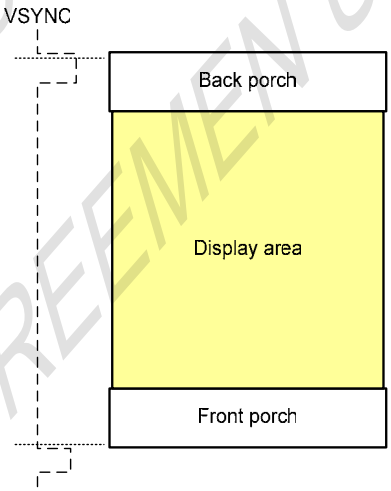


Figure 6-7 Front porch and back porch function diagram

6.2.9. Display Control 3 (R09h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	PTS2	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0

ISC3-0: To set the gate driver scan cycle in non-display area.

Table 6-10 summarized the function of ISC3-0 setting

Table 6-10

ISC3	ISC2	ISC1	ISC0	Scan cycle	fFLM=60Hz
0	0	0	1	Setting disable	
0	0	1	0	3frames	50 mS
0	0	1	1	5 frames	84 mS
0	1	0	0	7 frames	117 mS
0	1	0	1	9 frames	150 mS
0	1	1	0	11 frames	184 mS
0	1	1	1	13 frames	217 mS
1	0	0	0	15 frames	251 mS
1	0	0	1	19 frames	317 mS
1	0	1	0	21 frames	351 mS
1	0	1	1	23 frames	384 mS
1	1	0	0	25 frames	418 mS

ISC3	ISC2	ISC1	ISC0	Scan cycle	fFLM=60Hz
1	1	0	1	27 frames	451 mS
1	1	1	0	29 frames	484 mS
1	1	1	1	31 frames	518 mS

PTG1-0: To set the gate driver scan mode in non-display area.
Table 6-11 summarized the function of PTG1-0 setting

Table 6-11

PTG1	PTG0	Gate outputs in non-display area	Source outputs in non-display area	Vcom output
0	0	Normal scan	Based on the PT2-0 bits setting	VcomH/VcomL
0	1	Setting Disable		
1	0	Interval scan	Based on the PT2-0 bits setting	VcomH/VcomL
1	1	Setting Disable		

PTS2-0: To set the source driver output level in non-display area of partial display mode. **Table 6-2** summarized the function of PTS2-0 setting.

Table 6-2

PTS2	PTS1	PTS0	Source output in non-display area		Operation amplifier in non-display area
			+ polarity	- polarity	
0	0	0	V63	V0	V0-V63
0	0	1	Invalid setting	Invalid setting	-
0	1	0	GND	GND	V0-V63
0	1	1	High impedance	High impedance	V0-V63
1	0	0	V63	V0	V0, V63
1	0	1	Invalid setting	Invalid setting	-
1	1	0	GND	GND	V0, V63
1	1	1	High impedance	High impedance	V0, V63

6.2.10. Frame Cycle Control (R0Ah)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI2	FMI1	FMI0

FMI [2:0]: SPFD5408 provide FMARK signal to prevent tearing effect. FMI [2:0] can set FMARK output interval.

FMI2	FMI1	FMI0	Output interval
0	0	0	1 frame
0	0	1	2 frames
0	1	1	4 frames
1	0	1	6 frames
Other Setting			Setting Disable

FMARKOE: Initialized the output signal FMARK from FMARK pin.
FMARK="0": Output FMARK disable
FMARK="1". Output FMARK enables.

6.2.11. External Display Interface Control 1 (R0Ch)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	ENC2	ENC1	ENC0	0	0	0	RM	0	0	DIM1	DIM0	0	0	RIM1	RIM0

RIM1-0: To set the different transfer modes of RGB interface.

Table 6-3 summarized the function of RIM1-0 setting.

Table 6-3

RIM1	RIM0	RGB Interface Mode	Colors	Data Bus
0	0	18-bit RGB interface (one transfer/pixel)	262K	DB 17-0
0	1	16-bit RGB interface (one transfer/pixel)	65K	DB 17-13; DB 11-1
1	0	6-bit RGB interface (three transfers/pixel)	262K	DB17-12
1	1	Setting disabled	-	-

DM1-0: To specify the display interface mode. DM1-0 Setting can switch the display interface among system interface, RGB interface and VSYNC interface.

Table 6-4 summarized the function of DM1-0 setting.

Table 6-4

DM1	DM0	Display Interface
0	0	Internal clock operation
0	1	RGB interface
1	0	VSYNC interface
1	1	Setting disabled

RM: Select the interface to access the SPFD5408A's internal GRAM. Set RM to "1" when writing display data via the RGB interface. The SPFD5408A allows for setting the RM bit not constrained by the mode used for the display operation. This means it is possCBle to rewrite display data via a system interface by setting RM = "0" even while display operations are performed via the RGB interface.

Table 6-5 summarized the function of RM bit setting.

Table 6-5

RM	Interface for RAM Access
0	System interface/VSYNC interface
1	RGB interface

ENC2-0: Set the RAM data write cycle in RGB interface mode.

Table 6-6 summarized the function of ENC2-0 setting.

Table 6-6 ENC1-0 bits

ECN2	ECN1	ECN0	RAM data write cycle
0	0	0	1 frame
0	0	1	2 frames
0	1	0	3 frames
0	1	1	4 frames
1	0	0	5 frames
1	0	1	6 frames
1	1	0	7 frames
1	1	1	8 frames

Table 6-7

Display State	Operation Mode	RAM Access (RM)	Display Operation Mode (DM1-0)
Still pictures	Internal clock operation	System interface (RM = 0)	Internal clock operation (DM1-0 = 00)
Moving pictures	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
Rewrite still picture area while displaying moving pictures.	RGB interface (2)	System interface (RM = 0)	RGB interface (DM1-0 = 01)
Moving pictures	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)

Note1: Instructions are set only via the system interface.
Note2: The RGB-I/F and the VSYNC-I/F are not used simultaneously.
Note3: Do not make changes to the RGB-I/F mode setting (RIM-0) while the RGB I/F is in operation.
Note4: See the "External Display Interface" section for the flowcharts to follow when switching from one mode to another.
Note5: Use the high-speed write mode (HWM/LHWM = "1") when writing data in RGB or VSYNC interface mode.

6.2.12. Frame Maker Position (R0Dh)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0

FMP 8-0: indicates the output position of frame cycle signal (frame maker) relation with back porch. When FMP[8:0] =9'h000, FMARK is outputted at the start of back porch. When FMP[8:0] =9'h001, FMARK is outputted one line after the start of back porch.

FMP [8:0]	RAM data write cycle
9'h000	immedated
9'h001	1 line
9'h002	2 line
9'h175	373 lines
9'h176	374 lines
9'h177	375 lines

6.2.13. External Display Interface Control 2 (R0Fh)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL

EPL: The polarity of ENABLE signal selection in RGB interface mode.
EPL = "0": ENABLE: Low active
EPL = "1": ENABLE: High active

VSPL: The polarity of VSYNC signal selection in RGB interface mode.
VSPL = "0": Low active.
VSPL = "1": High active.

DPL: Select the data latch edge of the DOTCLK signal in RGB interface mode.
DPL = "0": rising edge of the DOTCLK.
DPL ="1": falling edge of the DOTCLK.

HSPL: The polarity of HSYNC signal selection in RGB interface mode.
HSPL = "0": Low active.
HSPL = "1": High active.

6.2.14. Power Control 1 (R10h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	SAP	BT3	BT2	BT1	BT0	APE	0	AP1	AP0	0	DSTB	SLP	0

SLP: Sleep mode selection. When SLP =1, SPFD5408A set to sleep mode. In sleep mode, all internal operations are terminated except internal RC oscillation. Be sure that a display off sequence should be executed before set SLP to "1". In sleep mode, no instruction can be accepted except R11h, R13h, bit 3-0 of R12h and R10h (except SAP2-0). Set STB=0 can exit sleep mode. Moreover, when exit from sleep mode, data in GRAM and in instruction registers are keep the same with these before set to SLP mode.

DSTB: Deep Standby mode selection. When DSTB =1, SPFD5408A set to deep standby mode. In this mode, all internal operations are terminated including internal RC oscillation. Be sure that a display off sequence should be executed before set DSTB to "1". Set DSTB=0 can exit standby mode. Be sure that start oscillation following by 10ms delay should be executed before set DSTB to "0". Moreover, when exit from deep standby mode, data in GRAM and register might be lost, reset and re-sending command and data into GRAM is necessary.

AP1-0: Operational amplifier DC bias current adjustment. Set AP1-0 = "00" to stop operational amplifier and DC/DC charge pump circuits to reduce current consumption during no display period. **Table 6-8** summarized the function of AP1-0 setting

Table 6-8

AP1	AP0	Constant current in power supply circuit	Constant current in Gamma circuit
0	0	Halt	Halt
0	1	0.5	0.62
1	0	0.75	0.71
1	1	1	1

APE: Enable bit for both liquid crystal power supply and gamma voltage generation circuit.

APE="0", Enable liquid crystal power supply and gamma voltage generation circuit.

APE="1", Halt liquid crystal power supply and gamma voltage generation circuit.

BT3-0: Set the voltage level of DDVDH, VGH, VGL and DD4OUT.

Table 6-9 summarized the function of BT3-0 setting

BT3	BT2	BT1	BT0	DDVDH	VGH	VGL	VCL	Capacitor connection pins
0	0	0	0	VCI1 x 2 [x2]	DDVDH x 3 [VCI1 x 6]	-(VCI1+DDVDHx 2) [VCI1x -5]	-VCI1	C23 can be eliminated
0	0	0	1	VCI1 x 2 [x2]	DDVDH x 4 [VCI1 x 8]	-(DDVDHx 2) [VCI1x -4]	-VCI1	
0	0	1	0	VCI1 x 2 [x2]	DDVDH x 4 [VCI1 x 8]	-(VCI1+DDVDH) [VCI1x -3]	-VCI1	
0	0	1	1	VCI1 x 2 [x2]	DDVDH x 3 + VCI1 [VCI1 x 7]	-(VCI1+DDVDHx 2) [VCI1x -5]	-VCI1	
0	1	0	0	VCI1 x 2 [x2]	DDVDH x 3 + VCI1 [VCI1 x 7]	-(DDVDHx 2) [VCI1x -4]	-VCI1	
0	1	0	1	VCI1 x 2 [x2]	DDVDH x 3 + VCI1 [VCI1 x 7]	-(VCI1+DDVDH) [VCI1x -3]	-VCI1	
0	1	1	0	VCI1 x 2 [x2]	DDVDH x 3 [VCI1 x 6]	-(DDVDHx 2) [VCI1x -4]	-VCI1	C23 can be eliminated
0	1	1	1	VCI1 x 2 [x2]	DDVDH x 3 [VCI1 x 6]	-(VCI1+DDVDH) [VCI1x -3]	-VCI1	C23 can be eliminated
1	0	0	0	VCI1 x 3 [x3]	DDVDH x 3 [VCI1 x 9]	-(VCI1+DDVDHx 2) [VCI1x -7]	-VCI1	C23 can be eliminated

1	0	0	1	VCI1 x 3 [x3]	DDVDH x 4 [VCI1 x 12]	-(DDVDHx 2) [VCI1x -6]	-VCI1	
1	0	1	0	VCI1 x 3 [x3]	DDVDH x 4 [VCI1 x 12]	-(VCI1+DDVDH) [VCI1x -4]	-VCI1	
1	0	1	1	VCI1 x 3 [x3]	DDVDH x 3 + VCI1 [VCI1 x 10]	-(VCI1+DDVDHx 2) [VCI1x -7]	-VCI1	
1	1	0	0	VCI1 x 3 [x3]	DDVDH x 3 + VCI1 [VCI1 x 10]	-(DDVDHx 2) [VCI1x -6]	-VCI1	
1	1	0	1	VCI1 x 3 [x3]	DDVDH x 3 + VCI1 [VCI1 x 10]	-(VCI1+DDVDH) [VCI1x -4]	-VCI1	
1	1	1	0	VCI1 x 3 [x3]	DDVDH x 3 [VCI1 x 9]	-(DDVDHx 2) [VCI1x -6]	-VCI1	C23 can be eliminated
1	1	1	1	VCI1 x 3 [x3]	DDVDH x 3 [VCI1 x 9]	-(VCI1+DDVDH) [VCI1x -4]	-VCI1	C23 can be eliminated

SAP: Enable bit for gamma voltage generation circuit.

SAP="0", Enable gamma voltage generation circuit.

SAP="1", Halt gamma voltage generation circuit.

6.2.15. Power Control 2 (R11h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0

VC2-0: Set the voltage of VCIOUT. VCIOUT is generated by VCILVL. **Table 6-20** summarized the function of VC2-0 setting

Table 6-20

VC2	VC1	VC0	VDCOUT
0	0	0	0.94 x VciLVL
0	0	1	0.89 x VciLVL
0	1	0	Setting Disable
0	1	1	Setting Disable
1	0	0	0.76 x VciLVL
1	0	1	Setting Disable
1	1	0	Setting Disable
1	1	1	1.00 x VCILVL

0	1	1	Oscillation clock / 8
1	0	0	Oscillation clock / 16
1	0	1	Invalid Setting
1	1	0	Halt Step-up Circuit 1
1	1	1	Invalid Setting

DC02-00: Set DC/DC charge pump circuit 1 operating frequency. **Table 6-210** summarized the function of DC02-00 setting

Table 6-210

DC02	DC01	DC00	DC/DC charge pump circuit 1 frequency (fDCDC1)
0	0	0	Oscillation clock
0	0	1	Oscillation clock / 2
0	1	0	Oscillation clock / 4

DC12-10: Set DC/DC charge pump circuit 2 operating frequency. **Table 6-11** summarized the function of DC02-00 setting

Note: Be aware that DC/DC charge pump 1 frequency ≥ DC/DC charge pump 2 frequency

Table 6-11

DC12	DC11	DC10	Step-up circuit 2 step-up frequency (fDCDC2)
0	0	0	Oscillation clock / 16
0	0	1	Oscillation clock / 32
0	1	0	Oscillation clock / 64
0	1	1	Oscillation clock / 128
1	0	0	Oscillation clock / 256
1	0	1	Setting disabled
1	1	0	Halt Step-up Circuit 2
1	1	1	Setting disabled

Note: Be sure fDCDC1≥fDCDC2 when setting DC02-00, DC12-10.

6.2.16. Power Control 3 (R12h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	VCMR[0]	VREG1R	0	PSON	PON	VRH3	VRH2	VRH1	VRH0

VRH3-0: Set the voltage level of VS. VS is generated by REGP. **Table 6-12** summarized the function of VRH3-0 setting

Table 6-12

VRH3	VRH2	VRH1	VRH0	VREG1OUT voltage		VRH3	VRH2	VRH1	VRH0	VREG1OUT voltage	
				VCILVL	VCIR					VCILVL	VCIR
0	0	0	0	Halt	Halt	1	0	0	0	VCILVLx1.6	2.5Vx1.6
0	0	0	1	Halt	Halt	1	0	0	1	VCILVLx1.65	2.5Vx1.65
0	0	1	0	Halt	Halt	1	0	1	0	VCILVLx1.7	2.5Vx1.7
0	0	1	1	Halt	Halt	1	0	1	1	VCILVLx1.75	2.5Vx1.75
0	1	0	0	Setting disable	Setting disable	1	1	0	0	VCILVLx1.8	2.5Vx1.8
0	1	0	1	Setting disable	Setting disable	1	1	0	1	VCILVLx1.85	2.5Vx1.85
0	1	1	0	Setting disable	Setting disable	1	1	1	0	VCILVLx1.9	2.5Vx1.9
0	1	1	1	Setting disable	Setting disable	1	1	1	1	Setting disable	Setting disable

PON: VDD3OUT ON/OFF control. Set PON = “0” to stop VDD3OUT. Set PON = “1” to start VDD3OUT.

PSON: Power Supply control bit for ON/OFF. When turning on power supply, Set PSE = “1” and Set PSON = “1” to start internal power supply operation..

VREG1R: Select reference voltage for VREG1OUIT

VREG1R = “0” (default): VCILVL (External) as reference voltage for VREG1OUT.

VREG1R = ”1”: VCIR (internal) as reference voltage for VREG1OUT.

VCMR[0]: Select VCOMH external resistance or internal setting for VCOMH voltage level.

VCMR[0] = “0” use VCOMR (External) setting as VCOMH voltage.

VCMR[0] = ”1”: use register (internal) setting as VCOMH voltage.

6.2.17. Power Control 4 (R13h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0

VDV4-0: Set the Vcom amplitude. Vcom amplitude is generated by VREG1OUT.

Table 6-13

VDV4	VDV3	VDV2	VDV1	VDV0	Vcom amplitude
0	0	0	0	0	VREG1OUT x 0.70
0	0	0	0	1	VREG1OUT x 0.72
0	0	0	1	0	VREG1OUT x 0.74
0	0	0	1	1	VREG1OUT x 0.76
0	0	1	0	0	VREG1OUT x 0.78
0	0	1	0	1	VREG1OUT x 0.80
0	0	1	1	0	VREG1OUT x 0.82
0	0	1	1	1	VREG1OUT x 0.84
0	1	0	0	0	VREG1OUT x 0.86
0	1	0	0	1	VREG1OUT x 0.88
0	1	0	1	0	VREG1OUT x 0.90
0	1	0	1	1	VREG1OUT x 0.92
0	1	1	0	0	VREG1OUT x 0.94
0	1	1	0	1	VREG1OUT x 0.96
0	1	1	1	0	VREG1OUT x 0.98
0	1	1	1	1	VREG1OUT x 1.00
1	0	0	0	0	VREG1OUT x 0.94
1	0	0	0	1	VREG1OUT x 0.96
1	0	0	1	0	VREG1OUT x 0.98
1	0	0	1	1	VREG1OUT x 1.00
1	0	1	0	0	VREG1OUT x 1.02
1	0	1	0	1	VREG1OUT x 1.04
1	0	1	1	0	VREG1OUT x 1.06
1	0	1	1	1	VREG1OUT x 1.08
1	1	0	0	0	VREG1OUT x 1.10
1	1	0	0	1	VREG1OUT x 1.12
1	1	0	1	0	VREG1OUT x 1.14
1	1	0	1	1	VREG1OUT x 1.16
1	1	1	0	0	VREG1OUT x 1.18
1	1	1	0	1	VREG1OUT x 1.20
1	1	1	1	0	VREG1OUT x 1.22
1	1	1	1	1	VREG1OUT x 1.24

6.2.18. Power Control 5 (R17h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PSE

PSE: Power supply enable bit

PSE = “1”, and set PSON can start SPFD5408 power supply system.

PSE = ”0”, power supply system reset. .

6.2.19. GRAM Address Set (Horizontal Address) (R20h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

6.2.20. GRAM Address Set (Vertical Address) (R21h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8

AD16–0: To set the initial address counter for GRAM address. Based on AM and I/D[1:0] setting, the address counter is automatically increment or decrement while data are written to the internal GRAM There is no need to updated AD16-0 every data transfer if AD16-0 was set in the beginning of one frame graphic data. Be aware that address counter is not automatically updated if reading data from the internal GRAM instruction is executed. Moreover, the address counter cannot be accessed when the SPFD5408A is in standby mode.

Table 6-14 summarized the function of AD15-0 setting

Note1: The address AD16-0 should be set in the address counter every frame on the falling edge of VSYNC if RGB interface mode is selected.

Note2: The address AD16-0 should be set when executing an instruction if system or VSYNC interface mode is selected.

Table 6-14

AD16–AD0	GRAM Setting
“00000”H – “000EF”H	Bitmap data for G1
“00100”H – “001EF”H	Bitmap data for G2
“00200”H – “002EF”H	Bitmap data for G3
“00300”H – “003EF”H	Bitmap data for G4
:	:
“13600”H – “13CEF”H	Bitmap data for G317
“13700”H – “13DEF”H	Bitmap data for G318
“13800”H – “13EEF”H	Bitmap data for G319
“13900”H – “13FEF”H	Bitmap data for G320

6.2.21. Write Data to GRAM (R22h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	RAM write data (WD17-0) The DB17-0 pin assignment is different in different interface modes.															

WD17-0: SPFD5408A supports 18 bits data format. However, if only 16-bit (565format) is input to GRAM, SPFD5408A will expand the 16 bit data into 18-bit format. Same case when RGB interface is selected. Based on the graphic data in GRAM, the grayscale voltage of source driver is selected. **Table 6-15** summarized the source driver grayscale voltage output versus graphic data in GRAM. **Figure 6-8 ~ Figure 6-18** illustrates the pin assignment among data bus (DB17-0), R22 (WD17-0) and GRAM.

Table 6-15

Data in GRAM	Source Driver Grayscale Output	
RGB	Negative	Positive
000000	V0	V63
000001	V1	V62
000010	V2	V61
000011	V3	V60
000100	V4	V59
000101	V5	V58
000110	V6	V57
000111	V7	V56
001000	V8	V55
001001	V9	V54
001010	V10	V53
001011	V11	V52
001100	V12	V51
001101	V13	V50
001110	V14	V49
001111	V15	V48
010000	V16	V47
010001	V17	V46
010010	V18	V45
010011	V19	V44
010100	V20	V43
010101	V21	V42
010110	V22	V41
010111	V23	V40
011000	V24	V39
011001	V25	V38
011010	V26	V37
011011	V27	V36
011100	V28	V35
011101	V29	V34
011110	V30	V33
011111	V31	V32
100000	V32	V31
100001	V33	V30
100010	V34	V29
100011	V35	V28
100100	V36	V27
100101	V37	V26
100110	V38	V25
100111	V39	V24
101000	V40	V23
101001	V41	V22
101010	V42	V21
101011	V43	V20
101100	V44	V19
101101	V45	V18
101110	V46	V17
101111	V47	V16
110000	V48	V15
110001	V49	V14
110010	V50	V13
110011	V51	V12
110100	V52	V11
110101	V53	V10
110110	V54	V9
110111	V55	V8
111000	V56	V7
111001	V57	V6
111010	V58	V5
111011	V59	V4
111100	V60	V3
111101	V61	V2
111110	V62	V1
111111	V63	V0

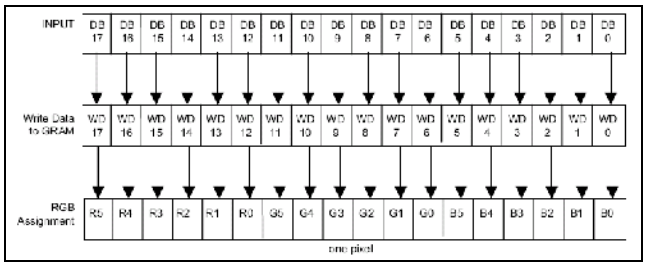


Figure 6-8 18-bit interface (262,144 colors)

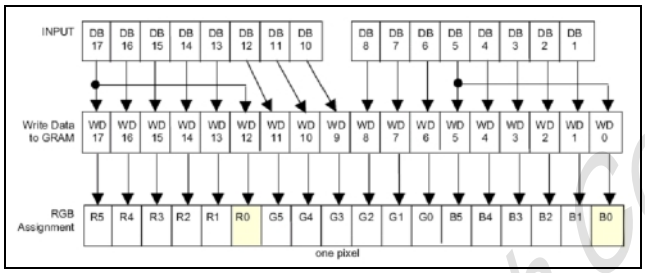


Figure 6-9 16-bit interface(65,536 colors) TRIREG= 0

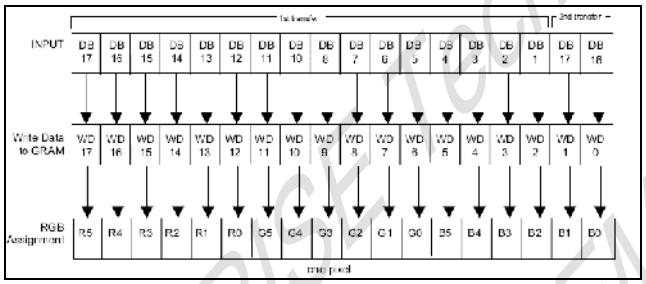


Figure 6-10 16-bit interface(262,144 colors) TRIREG = 1, DFM = 0

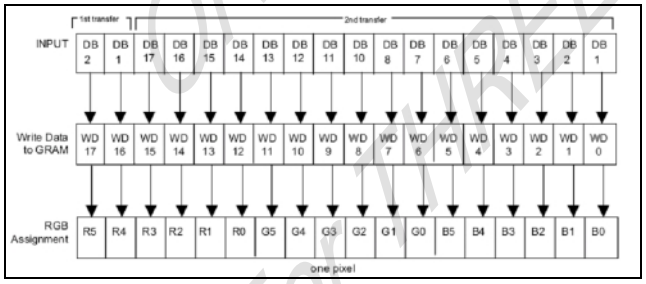


Figure 6-11 16-bit interface(262,144 colors) TRIREG = 1, DFM = 1

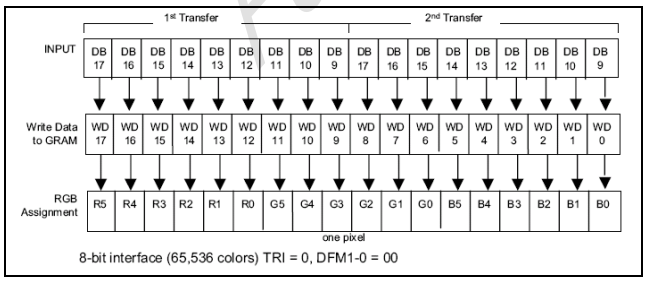


Figure 6-12 9-bit interface (262,144 colors)

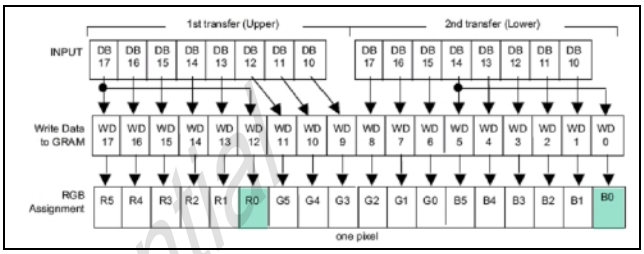


Figure 6-13 8-bit interface (65,536 colors) TRIREG = 0

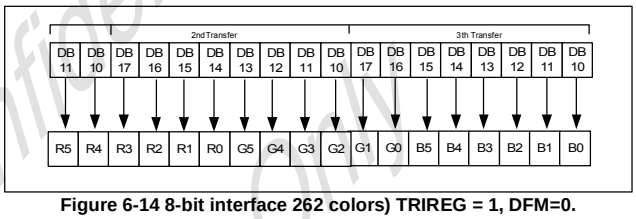


Figure 6-14 8-bit interface 262 colors) TRIREG = 1, DFM=0.

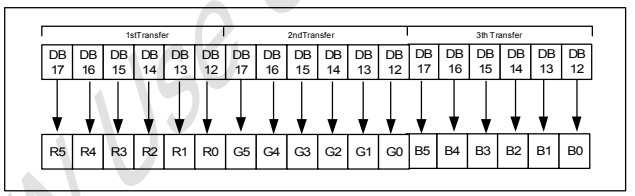


Figure 6-15 8-bit interface (262K colors) TRIREG = 1, DFM=1

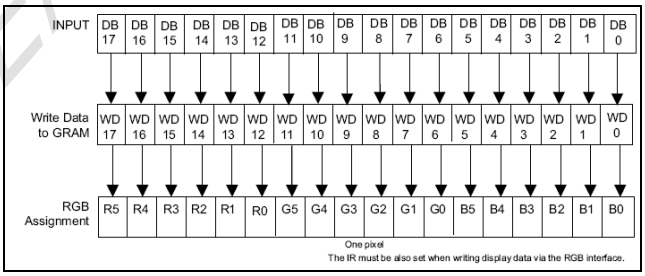


Figure 6-16 18-bit RGB interface (262,144 colors)

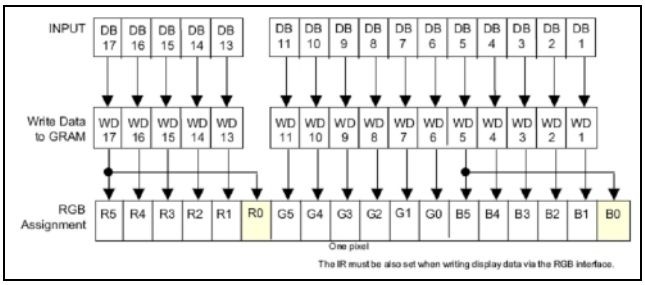


Figure 6-17 16-bit RGB interface (65,563 colors)

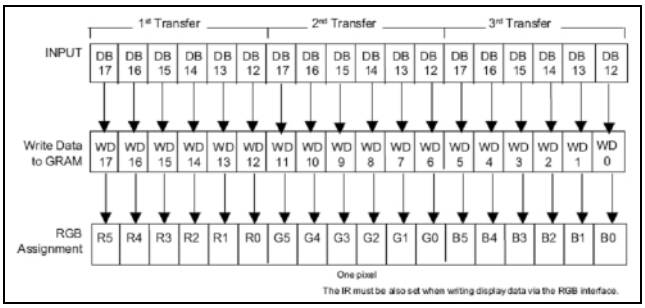


Figure 6-18 6-bit RGB interface (262,144 colors)

SPFD5408A supports external (RGB) interface. In RGB interface mode, all graphic data are stored in GRAM. To meet the diverse requirement of small size LCD panel, SPFD5408A also supports in a fix window using RGB interface and outside the window still use system interface.

In RGB interface mode, data writing to the internal RAM is synchronized with DOTCLK during ENABLE = “Low”. Set ENABLE “High” to terminate writing data to RAM. Wait for a write/read bus cycle time. If accessing internal RAM using the RGB interface is desired after accessing the RAM via the system interface. **Figure 6-8** illustrates the timing diagram while RGB and system interface are both use in the same time.

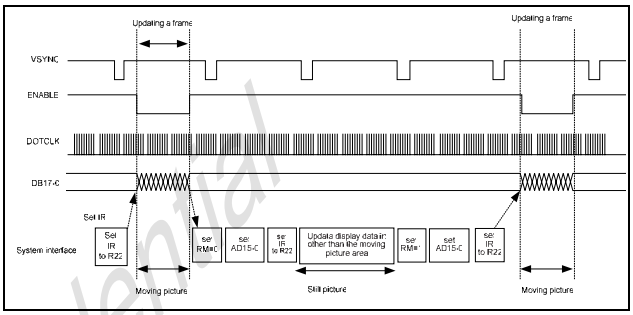


Figure 6-8

6.2.22. Read Data Read from GRAM (R22h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	RAM Read data (RD17-0) The DB17-0 pin assignment is different in different interface modes.															

R22 also served as a register, which store the data read out from GRAM. When data are read out from the GRAM is desired, first sets the RAM address and executes first word read, and issues second word read. When first word read instruction is issued, Invalid data are sent to the data bus DB17-0. Valid data are sent to the data bus as second word data is executed.

The LSBs of R and B dots cannot read out, when the 8 or 16-bit interface is selected,

Note: This register is not available with the RGB interface. **Figure 6-9** and **Figure 6-12** illustrates the pin assignment among data bus (DB17-0), R22 (WD17-0) and GRAM in read data instruction.

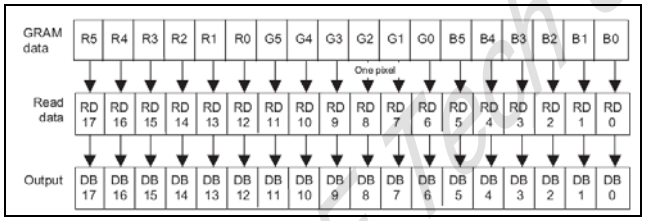


Figure 6-9 18-bit interface

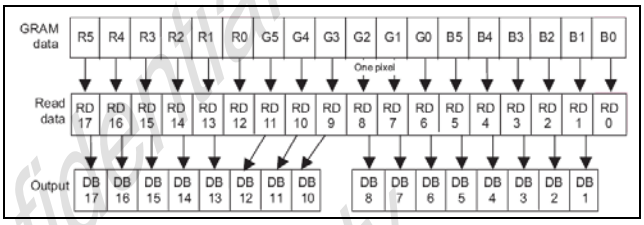


Figure 6-10 16-bit interface

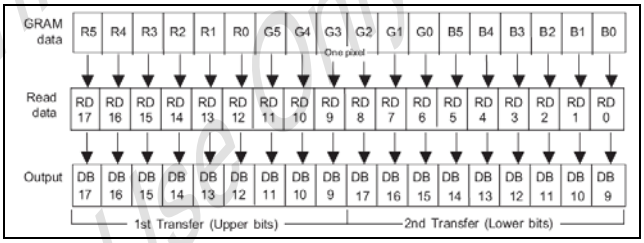


Figure 6-11 9-bit interface

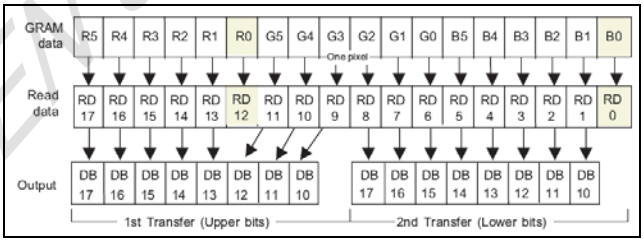


Figure 6-12 8-bit interface / SPI

6.2.23. NVM read data 1 (R28h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	UID3	UID2	UID1	UID0

6.2.24. NVM read data 2 (R29h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	VCM 14	VCM 13	VCM 12	VCM 11	VCM 10

6.2.25. NVM read data 3 (R2Ah)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	VCM SEL	0	0	VCM 24	VCM 23	VCM 22	VCM 21	VCM 20

UID[3:0]: SPFD5408A provides a 4-bit identification code UID[3:0] for user to use. UID[3:0] can be write / read from NVM. UID can be read out via R28h when CALB(RA4h, CB0) is set to 1.

VCM1[4:0]:

6.2.26. γ Control (R30h to R3Fh)

Table 6-15

	R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R30	W	1	0	0	0	V1RP4	V1RP3	V1RP2	V1RP1	V1RP0	0	0	0	V1RN4	V1RN3	V1RN2	V1RN1	V1RN0
R31	W	1	0	0	V2RP5	V2RP4	V2RP3	V2RP2	V2RP1	V2RP0	0	0	V2RN5	V2RN4	V2RN3	V2RN2	V2RN1	V2RN0
R32	W	1	0	0	V3RP5	V3RP4	V3RP3	V3RP2	V3RP1	V3RP0	0	0	V3RN5	V3RN4	V3RN3	V3RN2	V3RN1	V3RN0
R33	W	1	0	0	V4RP5	V4RP4	V4RP3	V4RP2	V4RP1	V4RP0	0	0	V4RN5	V4RN4	V4RN3	V4RN2	V4RN1	V4RN0
R34	W	1	0	0	V5RP5	V5RP4	V5RP3	V5RP2	V5RP1	V5RP0	0	0	V5RN5	V5RN4	V5RN3	V5RN2	V5RN1	V5RN0
R35	W	1	0	0	0	V6RP4	V6RP3	V6RP2	V6RP1	V6RP0	0	0	0	V6RN4	V6RN3	V6RN2	V6RN1	V6RN0
R36	W	1	0	0	0	V7RP4	V7RP3	V7RP2	V7RP1	V7RP0	0	0	0	V7RN4	V7RN3	V7RN2	V7RN1	V7RN0
R37	W	1	0	0	0	V8RP4	V8RP3	V8RP2	V8RP1	V8RP0	0	0	0	V8RN4	V8RN3	V8RN2	V8RN1	V8RN0
R38	W	1	0	0	0	0	V9RP3	V9RP2	V9RP1	V9RP0	0	0	0	0	V9RN3	V9RN2	V9RN1	V9RN0
R39	W	1	0	0	0	0	V10RP3	V10RP2	V10RP1	V10RP0	0	0	0	0	V10RN3	V10RN2	V10RN1	V10RN0
R3A	W	1	0	0	0	0	V11RP3	V11RP2	V11RP1	V11RP0	0	0	0	0	V11RN3	V11RN2	V11RN1	V11RN0
R3B	W	1	0	0	0	0	V12RP3	V12RP2	V12RP1	V12RP0	0	0	0	0	V12RN3	V12RN2	V12RN1	V12RN0
R3C	W	1	0	0	0	0	V13RP3	V13RP2	V13RP1	V13RP0	0	0	0	0	V13RN3	V13RN2	V13RN1	V13RN0
R3D	W	1	0	0	0	0	V14RP3	V14RP2	V14RP1	V14RP0	0	0	0	0	V14RN3	V14RN2	V14RN1	V14RN0
R3E	W	1	0	0	0	0	V15RP3	V15RP2	V15RP1	V15RP0	0	0	0	0	V15RN3	V15RN2	V15RN1	V15RN0
R3F	W	1	0	0	0	0	V16RP3	V16RP2	V16RP1	V16RP0	0	0	0	0	V16RN3	V16RN2	V16RN1	V16RN0

γ Control (R30h to R3Fh): SPFD5408A provides 16 gamma registers to fine tune gamma output voltage.

V1RP[4:0]: register for positive VSD0 fine tune adjustment.
V2RP[5:0]: register for positive VSD1 fine tune adjustment.
V3RP[5:0]: register for positive VSD2 fine tune adjustment.
V4RP[5:0]: register for positive VSD61 fine tune adjustment.
V5RP[5:0]: register for positive VSD62 fine tune adjustment.
V6RP[4:0]: register for positive VSD63 fine tune adjustment
V7RP[4:0]: register for positive VSD13 fine tune adjustment
V8RP[4:0]: register for positive VSD50 fine tune adjustment
V9RP[3:0]: register for positive VSD4 fine tune adjustment
V10RP[3:0]: register for positive VSD8 fine tune adjustment
V11RP[3:0]: register for positive VSD20 fine tune adjustment
V12RP[3:0]: register for positive VSD27 fine tune adjustment
V13RP[3:0]: register for positive VSD364 fine tune adjustment
V14RP[3:0]: register for positive VSD43 fine tune adjustment
V15RP[3:0]: register for positive VSD55 fine tune adjustment
V16RP[3:0]: register for positive VSD59 fine tune adjustment

V1RN[4:0]: register for negative VSD0 fine tune adjustment.
V2RN[5:0]: register for negative VSD1 fine tune adjustment.
V3RN[5:0]: register for negative VSD2 fine tune adjustment.
V4RN[5:0]: register for negative VSD61 fine tune adjustment.
V5RN[5:0]: register for negative VSD62 fine tune adjustment.
V6RN[4:0]: register for negative VSD63 fine tune adjustment
V7RN[4:0]: register for negative VSD13 fine tune adjustment
V8RN[4:0]: register for negative VSD50 fine tune adjustment
V9RN[3:0]: register for negative VSD4 fine tune adjustment
V10RN[3:0]: register for negative VSD8 fine tune adjustment
V11RN[3:0]: register for negative VSD20 fine tune adjustment
V12RN[3:0]: register for negative VSD27 fine tune adjustment
V13RN[3:0]: register for negative VSD364 fine tune adjustment
V14RN[3:0]: register for negative VSD43 fine tune adjustment
V15RN[3:0]: register for negative VSD55 fine tune adjustment
V16RN[3:0]: register for negative VSD59 fine tune adjustment

6.2.27. Window Horzontal RAM Address Start (R50h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0

6.2.28. Window Horzontal RAM Address End (R51h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0

6.2.29. Window Vertical RAM Address Start (R52h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0

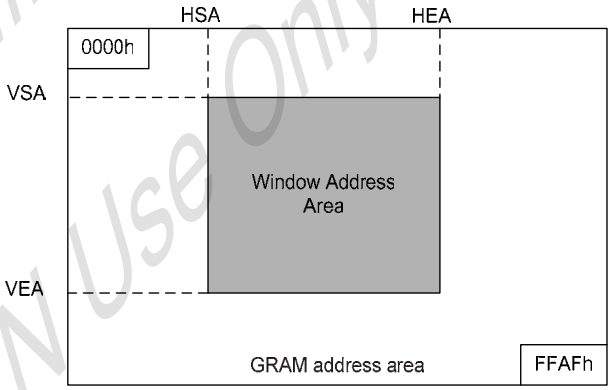
6.2.30. Window Vertical RAM Address End (R53h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0

HSA7-0/HEA7-0: SPFD5408A provides window access function. Set HSA7-0 and HEA7-0 represent the start address and end address of the window function in horizontal direction. To use window-accessing function, HSA and HEA bits must be set before starting RAM write operation. Be aware that "00"h ≤ HSA7-0< HEA7-0 ≤ "EF"h and HEA-HAS>="04h".

VSA8-0/VEA8-0: SPFD5408A provides window access function. Set VSA8-0 and VEA8-0 represent the start address and end address of the window in vertical direction. To use window-accessing function, VSA and VEA bits must be set before starting RAM write operation. Be aware that "00"h ≤ VSA8-0< VEA8-0 ≤ 9'h13F.

Figure 6-24 illustrates the window-accessing function using R44and R45.



6.2.31. Driver Output Control (R60h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0

SCN5-0: Set the SCN5-0 bits can specify the starting position of the gate driver. The start position of gate driver is determined by the combination of the setting of GS and SM. **Table 6-16** summarized the starting position for each SCN5-0 setting.

Table 6-16 (whenSM=0)

SCN5	SCN4	SCN3	SCN2	SCN1	SCN0	Scan Start Position (Gate line)	
						GS = "0"	GS = "1"
0	0	0	0	0	0	G1	G320
0	0	0	0	0	1	G9	G312
0	0	0	0	1	0	G17	G304
0	0	0	0	1	1	G25	G296
0	0	0	1	0	0	G33	G288
0	0	0	1	0	1	G41	G280
0	0	0	1	1	0	G49	G272
0	0	0	1	1	1	G57	G264
0	0	1	0	0	0	G65	G256
0	0	1	0	0	1	G73	G248
0	0	1	0	1	0	G81	G240
0	0	1	0	1	1	G89	G232
0	0	1	1	0	0	G97	G224
0	0	1	1	0	1	G105	G216
0	0	1	1	1	0	G113	G208
0	0	1	1	1	1	G121	G200
0	1	0	0	0	0	G129	G192
0	1	0	0	0	1	G137	G184
0	1	0	0	1	0	G145	G176
0	1	0	0	1	1	G153	G168
0	1	0	1	0	0	G161	G160
0	1	0	1	0	1	G169	G152
0	1	0	1	1	0	G177	G144
0	1	0	1	1	1	G185	G136
0	1	1	0	0	0	G193	G128

SC N5	SC N4	SC N3	SC N2	SC N1	SC N0	Scan Start Position (Gate line)	
						GS = "0"	GS = "1"
0	1	1	0	0	1	G201	G120
0	1	1	0	1	0	G209	G112
0	1	1	0	1	1	G217	G104
0	1	1	1	0	0	G225	G96
0	1	1	1	0	1	G233	G88
0	1	1	1	1	0	G241	G80
0	1	1	1	1	1	G249	G72
1	0	0	0	0	0	G257	G64
1	0	0	0	0	1	G265	G56
1	0	0	0	1	0	G273	G48
1	0	0	0	1	1	G281	G40
1	0	0	1	0	0	G289	G32
1	0	0	1	0	1	G297	G24
1	0	0	1	1	0	G305	G16
1	0	0	1	1	1	G313	G8
1	0	1	0	0	0	Setting disable	
Setting disable							
1	1	1	1	1	1	Setting	

NL5-0: NL4-0: Set the number of gate lines for different resolution of display panel. The combination of NL4-NL0 represents the gate line number are summarized at **Table 6-17**

Table 6-17

NL5	NL4	NL3	NL2	NL1	NL0	Display Size	Lines	Driven gate lines
0	0	0	0	0	0	Setting disabled	Setting disabled	Setting disabled
Setting disable								
0	1	0	1	0	1	720 x 176 dots	176	G1 ~ G176
Setting disable								
0	1	1	1	0	1	720 x 240 dots	240	G1 ~ G240
0	1	1	1	1	0	720 x 248 dots	248	G1 ~ G248
0	1	1	1	1	1	720 x 256 dots	256	G1 ~ G256
1	0	0	0	0	0	720 x 264 dots	264	G1 ~ G264
1	0	0	0	0	1	720 x 272 dots	272	G1 ~ G272
1	0	0	0	1	0	720 x 280 dots	280	G1 ~ G280
1	0	0	0	1	1	720 x 288 dots	288	G1 ~ G288
1	0	0	1	0	0	720 x 296 dots	296	G1 ~ G296
1	0	0	1	0	1	720 x 304 dots	304	G1 ~ G304
1	0	0	1	1	0	720 x 312 dots	312	G1 ~ G312
1	0	0	1	1	1	720 x 320 dots	320	G1 ~ G320
Setting disable								

Note: Back porch and a front porch (set with BP/FP bits respectively) are inserted before/ after driving all gate lines,

GS: Shift direction of the gate driver output selection. When
GS="0", gate driver shift from G1 to G320. When GS = "1", gate driver shift from G320 to G1.

6.2.32. Driver Output Control (R61h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV

REV: To set the grayscale corresponding to normally white or normally black LCD panel from same data input.

Table 6-30 summarized REV bit function.

Table 6-30

REV	GRAM data	Source Driver Output	
		Positive Polarity	Negative Polarity
0	18'h00000	V63	V0
	⋮	⋮	⋮
	18'h3FFFF	V0	V63
1	18'h00000	V0	V63
	⋮	⋮	⋮
	18'h3FFFF	V63	V0

VLE: SPFD5408 provides vertical scrolling function which can be set by VLE bit.

VLE = "1", vertical scrolling function enable. The amout of scrolling line from the first line is determined by VL[8:0].

VLE = "0", normal display.

NDL: set the source duiver output level in non-lit area..

NDL = "1", .

NDL = "0", .

6.2.33. Vertical Scroll Control (R6Ah)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0

VL8-0: SPFD5408A provides scrolling function. The start position for displaying the image is shifted vertically by the number of lines based on the setting of the VL8-0 bits. Be aware that the vertical scrolling function is not available in the external (RGB) display interface mode. **Table 6-31** summarized the function of VL8-0 setting.

Table 6-31

VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	Scrolling lines
0	0	0	0	0	0	0	0	0	0 line
0	0	0	0	0	0	0	0	1	1 line
0	0	0	0	0	0	0	1	0	2 lines
	:	:	:	:	:	:	:	:	:
1	0	0	1	1	1	1	1	1	319 lines
1	0	1	0	0	0	0	0	0	320 lines

Note: VL8-0 bits cannot set more than 320 lines.

6.2.34. Display Position – Partial Display 1 (R80h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTD P08	PTD P07	PTD P06	PTD P05	PTD P04	PTD P03	PTD P02	PTD P01	PTD P00

6.2.35. RAM Address Start – Partial Display 1 (R81h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTS A08	PTS A07	PTS A06	PTS A05	PTS A04	PTS A03	PTS A02	PTS A01	PTS A00

6.2.36. RAM address End – Partail Display 1 (R82h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTE A08	PTE A07	PTE A06	PTE A05	PTE A04	PTE A03	PTE A02	PTE A01	PTE A00

6.2.37. Display Position – Partial Display 2 (R83h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTD P18	PTD P17	PTD P16	PTD P15	PTD P14	PTD P13	PTD P12	PTD P11	PTD P10

6.2.38. RAM Address Start – Partial Display 2 (R84h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTS A18	PTS A17	PTS A16	PTS A15	PTS A14	PTS A13	PTS A12	PTS A11	PTS A10

6.2.39. RAM Address End – Partial Display 2 (R85h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTE A18	PTE A17	PTE A16	PTE A15	PTE A14	PTE A13	PTE A12	PTE A11	PTE A10

PTDP0[8:0]: Set the physical starting position of partial display 1 on the LCD panel

PTDP1[8:0]: Set the physical starting position of partial display 2 on the LCD panel

The partial display 1 and partial display 2 should not overlap with each other. And make sure the PTDP0[8:0] < PTDP1[8:0].

PTSA0[8:0]: Set the start line address of display RAM of partial display 1 which will be display according to PTDP0[8:0].

PTEA0[8:0]: Set the end line address of display RAM of partial display 1 which will be display according to PTDP0[8:0].

Make sure PTSA0<=PTEA0

PTSA1[8:0]: Set the start line address of display RAM of partial display2 which will be display according to PTDP1[8:0].

PTEA1[8:0]: Set the end line address of display RAM of partial display2 which will be display according to PTDP1[8:0]

Make sure PTSA1<=PTEA1

6.2.40. Frame Cycle Control (R90h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	DIV1	DIV0	0	0	0	RTN4	RTN3	RTN2	RTN1	RTN0

RTN3-0: Set the clock cycle per line **Table 6-18** summarized the function of RTN3-0 setting.

Table 6-18

RTN4	RTN3	RTN2	RTN1	RTN0	Clock Cycles per line
0	0	0	0	0	Setting disable
Setting disable					
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks

RTN4	RTN3	RTN2	RTN1	RTN0	Clock Cycles per line
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks

DIV1-0: To specified the division ratio of internal operation clock frequency. Set the RTN and DIV bits to adjust frame frequency. Be aware of that if the number of lines for driving liquid crystal is changed, the frame frequency must also be adjusted. Moreover, In RGB interface mode, the DIV1-0 bits are disabled. **Table 6-19** summarized the function of DIV1-0 setting.

Formula to calculate frame frequency

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{Clock cycles per line} \times \text{division ratio} \times (\text{Line} + \text{BP} + \text{FP})} \quad [\text{Hz}]$$

fosc: frequency of RC oscillation

Line: number of lines for driving liquid crystal (NL bits)

Division ratio: DIV bits

Clock cycles per line: RTN bits

FP: the number of lines for the front porch period

BP: the number of lines for the back porch period

Table 6-19

DIV1	DIV0	Division Ratio	Internal Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

fosc =Frequency of RC oscillation

6.2.41. Panel Interface Control 2 (R92h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	NOWI2	NOWI1	NOWI0	0	0	0	0	0	0	0	0

NOWI [2:0]: Set the adjacent gate driver output non-overlap period. **Table 6-20** summarized the function of NO1-0 setting.

Table 6-20

NOWI2	NOW!1	NOWI0	Gate output non-overlap period Internal Operation (reference clock: internal oscillator)
0	0	0	0 clock
0	0	1	1 clocks
0	1	0	2 clocks
0	1	1	3 clocks
1	0	0	4 clocks
1	0	1	5 clocks
1	1	0	6 clocks
1	1	1	7 clocks

6.2.42. Panel Interface control 3 (R93h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	VEQW11	VEQW10						MCPI2	MCPI1	MCPI0

MCPI[2:0]: Set source driver start output timing. The source driver output position is measure from internal reference point.

MCPE2	MCPE1	MCPE0	Source driver start output position
0	0	0	0 clock
0	0	1	1 clocks
0	1	0	2 clocks
0	1	1	3 clocks
1	0	0	4 clocks
1	0	1	5 clocks
1	1	0	6 clocks
1	1	1	7 clocks

VEQW1[1:0]: Set VCOM equalize period.

VEQW1	VEQW0	VCOM Equalize Period
0	0	0 clock
0	1	1 clock
1	0	2 clocks
1	1	3 clocks

6.2.43. Frame Cycle Control (R95h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	DIVE1	DIVE0	0	0	RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0

RTNE5-0: Set the clock cycle per line **Table 6-18** summarized the function of RTN3-0 setting.

Table 6-21

RTN4	RTN3	RTN2	RTN1	RTN0	Clock Cycles per line
0	0	0	0	0	Setting disable
Setting disable					
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks

DIV1-0: To specified the division ratio of internal operation clock frequency. Set the RTN and DIV bits to adjust frame frequency. Be aware of that if the number of lines for driving liquid crystal is changed, the frame frequency must also be adjusted. Moreover, In RGB interface mode, the DIV1-0 bits are disabled. **Table 6-19** summarized the function of DIV1-0 setting.

Table 6-22

DIV1	DIV0	Division Ratio	Internal Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

fosc =Frequency of RC oscillation

6.2.44. Panel Interface Control 5 (R97h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	NOWE3	NOWE2	NOWE1	NOWE0	0	0	0	0	0	0	0	0

NOWE [3:0]: Set the adjacent gate driver output non-overlap period inRGB interface. **Table 6-20** summarized the function of NO1-0 setting.

Table 6-23

NOWE3	NOWE2	NOWE1	NOWE0	Gate output non-overlap period Internal Operation (reference clock: internal oscillator)
0	0	0	0	0 clock
0	0	0	1	1 clocks
0	0	1	0	2 clocks
0	0	1	1	3 clocks
0	1	0	0	4 clocks
0	1	0	1	5 clocks
0	1	1	0	6 clocks
0	1	1	1	7 clocks
1	0	0	0	8 clocks
1	0	0	1	9 clocks
1	0	1	0	10 clocks
1	0	1	1	11 clocks
1	1	0	0	12 clocks
1	1	0	1	13 clocks
1	1	1	0	14 clocks
1	1	1	1	15 clocks

6.2.45. Panel Interface Control (R98h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPE2	MCPE1	MCPE0

MCPE[2:0]: Set source driver start output timing in RGB interface. The source driver output position is measure from internal reference point.

MCPE2	MCPE1	MCPE0	Source driver start output position
0	0	0	0 clock
0	0	1	1 clocks
0	1	0	2 clocks
0	1	1	3 clocks
1	0	0	4 clocks
1	0	1	5 clocks
1	1	0	6 clocks
1	1	1	7 clocks

6.2.46. Calibration Control (RA4h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CALB

CALB: .the enable bit for the read function of the NVM.

When CALB=”1”: Read function from NVM is enable.

When CALB=”0”: Read function from NVMis disable.

7. GRAM

Table 7-1 GRAM address and display panel position (SS = "0")

S/G pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	....	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	DB17-0			DB17-0			DB17-0			DB17-0			....	DB17-0			DB17-0			DB17-0			DB17-0		
G1	G320	"00000"H			"00001"H			"00002"H			"00003"H			....	"000EC"H			"000ED"H			"000EE"H			"000EF"H		
G2	G319	"00100"H			"00101"H			"00102"H			"00103"H			....	"001EC"H			"001ED"H			"001EE"H			"001EF"H		
G3	G318	"00200"H			"00201"H			"00202"H			"00203"H			....	"002EC"H			"002ED"H			"002EE"H			"002EF"H		
G4	G317	"00300"H			"00301"H			"00302"H			"00303"H			....	"003EC"H			"003ED"H			"003EE"H			"003EF"H		
G5	G316	"00400"H			"00401"H			"00402"H			"00403"H			....	"004EC"H			"004ED"H			"004EE"H			"004EF"H		
G6	G315	"00500"H			"00501"H			"00502"H			"00503"H			....	"005EC"H			"005ED"H			"005EE"H			"005EF"H		
G7	G314	"00600"H			"00601"H			"00602"H			"00603"H			....	"006EC"H			"06ED"H			"06EE"H			"06EF"H		
G8	G313	"00700"H			"00701"H			"00702"H			"00703"H			....	"007EC"H			"007ED"H			"007EE"H			"007EF"H		
G9	G312	"00800"H			"00801"H			"00802"H			"00803"H			....	"008EC"H			"008ED"H			"008EE"H			"008EF"H		
G10	G311	"00900"H			"00901"H			"00902"H			"00903"H			....	"009EC"H			"009ED"H			"009EE"H			"009EF"H		
G11	G310	"00E00"H			"00E01"H			"00E02"H			"00E03"H			....	"00EEC"H			"00EED"H			"00EEE"H			"00EEF"H		
G12	G309	"00B00"H			"00B01"H			"00B02"H			"00B03"H			....	"00BEC"H			"00BED"H			"00BEE"H			"00BEF"H		
G13	G308	"00C00"H			"00C01"H			"00C02"H			"00C03"H			....	"00CEC"H			"00CED"H			"00CEE"H			"00CEF"H		
G14	G307	"00D00"H			"00D01"H			"00D02"H			"00D03"H			....	"00DEC"H			"00DED"H			"00DEE"H			"00DEF"H		
G15	G306	"00E00"H			"00E01"H			"00E02"H			"00E03"H			....	"00EEC"H			"00EED"H			"00EEE"H			"00EEF"H		
G16	G305	"00F00"H			"00F01"H			"00F02"H			"00F03"H			....	"00FEC"H			"00FED"H			"00FEE"H			"00FEF"H		
G17	G304	"01000"H			"01001"H			"01002"H			"01003"H			....	"010EC"H			"010ED"H			"010EE"H			"010EF"H		
G18	G303	"01100"H			"01101"H			"01102"H			"01103"H			....	"011EC"H			"011ED"H			"011EE"H			"011EF"H		
G19	G302	"01200"H			"01201"H			"01202"H			"01203"H			....	"012EC"H			"012ED"H			"012EE"H			"012EF"H		
G20	G301	"01300"H			"01301"H			"01302"H			"01303"H			....	"013EC"H			"013ED"H			"013EE"H			"013EF"H		
:	:	:			:			:			:				:			:			:			:		
:	:	:			:			:			:				:			:			:			:		
G313	G8	"13800"H			"13801"H			"13802"H			"13803"H			....	"138EC"H			"138ED"H			"138EE"H			"138EF"H		
G314	G7	"13900"H			"13901"H			"13902"H			"13903"H			....	"139EC"H			"139ED"H			"139EE"H			"139EF"H		
G315	G6	"13A00"H			"13A01"H			"13A02"H			"13A03"H			....	"13AEC"H			"13AED"H			"13AEE"H			"13AEF"H		
G316	G5	"13B00"H			"13B01"H			"13B02"H			"13B03"H			....	"13BEC"H			"13BED"H			"13BEE"H			"13BEF"H		
G317	G4	"13C00"H			"13C01"H			"13C02"H			"13C03"H			....	"13CEC"H			"13CED"H			"13CEE"H			"13CEF"H		
G318	G3	"13D00"H			"13D01"H			"13D02"H			"13D03"H			....	"13DEC"H			"13DED"H			"13DEE"H			"13DEF"H		
G319	G2	"13E00"H			"13E01"H			"13E02"H			"13E03"H			....	"13EEC"H			"13EED"H			"13EEE"H			"13EEF"H		
G320	G1	"13F00"H			"13F01"H			"13F02"H			"13F03"H			....	"13FEC"H			"13FED"H			"13FEE"H			"13FEF"H		

Table 7-2 GRAM address and display panel position (SS = "1")

S/G pin		S1	S2	S3	S4	S5	…	S7	S8	S9	S10	S11	S12	….	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	DB17-0			DB17-0			DB17-0			DB17-0			….	DB17-0			DB17-0			DB17-0			DB17-0		
G1	G320	"000EF"H			"000EE"H			"000ED"H			"000EC"H			….	"00003"H			"00002"H			"00001"H			"00000"H		
G2	G319	"001EF"H			"001EE"H			"001ED"H			"001EC"H			….	"00103"H			"00102"H			"00101"H			"00100"H		
G3	G318	"002EF"H			"002AE"H			"002ED"H			"002EC"H			….	"00203"H			"00202"H			"00201"H			"00200"H		
G4	G317	"003EF"H			"003EE"H			"003ED"H			"003EC"H			….	"00303"H			"00302"H			"00301"H			"00300"H		
G5	G316	"004EF"H			"004EE"H			"004ED"H			"004EC"H			….	"00403"H			"00402"H			"00401"H			"00400"H		
G6	G315	"005EF"H			"005EE"H			"005ED"H			"005EC"H			….	"00503"H			"00502"H			"00501"H			"00500"H		
G7	G314	"006EF"H			"006EE"H			"006ED"H			"006EC"H			….	"00603"H			"00602"H			"00601"H			"00600"H		
G8	G313	"007EF"H			"007EE"H			"007ED"H			"007EC"H			….	"00703"H			"00702"H			"00701"H			"00700"H		
G9	G312	"008EF"H			"008EE"H			"008ED"H			"008EC"H			….	"00803"H			"00802"H			"00801"H			"00800"H		
G10	G311	"009EF"H			"009EE"H			"009ED"H			"009EC"H			….	"00903"H			"00902"H			"00901"H			"00900"H		
G11	G310	"00AEF"H			"00AEE"H			"00AED"H			"00AEC"H			….	"00E03"H			"00A02"H			"00A01"H			"00A00"H		
G12	G309	"00BEF"H			"00BEE"H			"00BED"H			"00BEC"H			….	"00B03"H			"00B02"H			"00B01"H			"00B00"H		
G13	G308	"00CEF"H			"00CEE"H			"00CED"H			"00CEC"H			….	"00C03"H			"00C02"H			"00C01"H			"00C00"H		
G14	G307	"00DEF"H			"00DEE"H			"00DED"H			"00DEC"H			….	"00D03"H			"00D02"H			"00D01"H			"00D00"H		
G15	G306	"00EEF"H			"00EEE"H			"00EED"H			"00EEC"H			….	"00E03"H			"00E02"H			"00E01"H			"00E00"H		
G16	G305	"00FEF"H			"00FEE"H			"00FED"H			"00FEC"H			….	"00F03"H			"00F02"H			"00F01"H			"00F00"H		
G17	G304	"010EF"H			"010EE"H			"010ED"H			"010EC"H			….	"01003"H			"01002"H			"01001"H			"01000"H		
G18	G303	"011EF"H			"011EE"H			"011ED"H			"011EC"H			….	"01103"H			"01102"H			"01101"H			"01100"H		
G19	G302	"012EF"H			"012EE"H			"012ED"H			"012EC"H			….	"01203"H			"01202"H			"01201"H			"01200"H		
G20	G301	"013EF"H			"013EE"H			"013ED"H			"013EC"H			….	"01303"H			"01302"H			"01301"H			"01300"H		
:	:	:			:			:			:				:			:			:			:		
:	:	:			:			:			:				:			:			:			:		
G233	G8	"E8EF"H			"138EE"H			"138ED"H			"138EC"H			….	"13803"H			"13802"H			"13801"H			"13800"H		
G234	G7	"139EF"H			"139EE"H			"139ED"H			"139EC"H			….	"13903"H			"13902"H			"13901"H			"13900"H		
G235	G6	"13AEF"H			"13AEE"H			"13AED"H			"13AEC"H			….	"13A03"H			"13A02"H			"13A01"H			"13A00"H		
G236	G5	"13BEF"H			"13BEE"H			"13BED"H			"13BEC"H			….	"13B03"H			"13B02"H			"13B01"H			"13B00"H		
G237	G4	"13CEF"H			"13CEE"H			"13CED"H			"13CEC"H			….	"13C03"H			"13C02"H			"13C01"H			"13C00"H		
G238	G3	"13DEF"H			"13DEE"H			"13DED"H			"13DEC"H			….	"13D03"H			"13D02"H			"13D01"H			"13D00"H		
G239	G2	"13EEF"H			"13EEE"H			"13EED"H			"13EEC"H			….	"13E03"H			"13E02"H			"13E01"H			"13E00"H		
G240	G1	"13FEF"H			"13FEE"H			"13FED"H			"13FEC"H			….	"13F03"H			"13F02"H			"13F01"H			"13F00"H		

8. INTERFACES

The SPFD5408A provides different interfaces to meet the diverse need of small/medium size LCD. Based on the application requirement, there are three different display modes which are most used in end product.

1. Still picture display
2. Moving picture display.
3. Re-writing still pictures while moving picture are display.

For above three different display requirements, SPFD5408A provides different interfaces to meet the requirement.

1. System interface
2. External interface (RGB interface)
3. VSYNC interface

System interface is suitable for still picture display while RGB interface and VSYNC interface are suitable for moving picture display. Be aware that RGB or VSYNC interface still can used to display still picture and system interface can also display moving picture. **Table 8-1** summarized different interfaces for different display requirement.

Table 8-1

Operation Mode	Display Mode	RAM Access Setting (RM)	Display Operation Mode (DM1-0)
System	Still picture	System interface (RM = 0)	Internal operating clock (DM1-0 = 00)
RGB interface (1)	Moving picture	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
RGB interface (2)	Rewriting still pictures while displaying moving pictures	System interface (RM = 0)	RGB interface (DM1-0 = 01)
VSYNC interface	Moving pictures	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)

8.1. System Interface

The system interfaces of SPFD5408A can support 8-bit, 9-bit, 16-bit, 18-bit 80-system Interface and Serial Peripheral Interface (SPI), which can be set by the IM3/2/1/0 pins. The system interface can set instructions and access RAM. **Table 8-2** summarized the interface corresponding to IM3-0 setting.

Table 8-2

IM3	IM2	IM1	IM0	MPU-Interface Mode	DB Pin in use
0	0	0	0	Setting disabled	-
0	0	0	1	Setting disabled	-
0	0	1	0	80-system 16-bit interface	DB17 to 10 and 8-to-1
0	0	1	1	80-system 8-bit interface	DB17 to 10
0	1	0	*	Serial peripheral interface (SPI)	DB1-0
0	1	1	*	Setting disabled	-
1	0	0	0	Setting disabled	-
1	0	0	1	Setting disabled	-
1	0	1	0	80-system 18-bit interface	DB17 to 0
1	0	1	1	80-system 9-bit interface	DB17 to 9
1	1	*	*	Setting disabled -	-

8.1.1. 80-system 18-bit interface

The instruction and GRAM accessing format of 80-system 18-bit interface are shown in **Figure 8-1** and **Figure 8-2**, respectively.

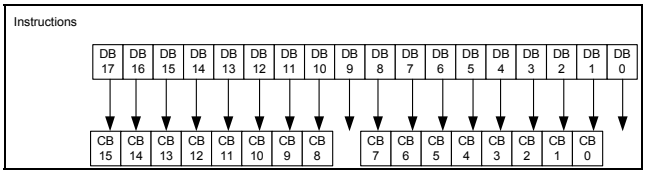


Figure 8-1

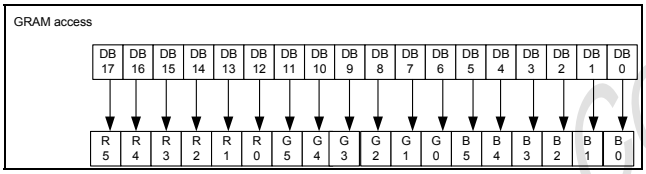


Figure 8-2

8.1.2. 80-system 16-bit interface

The instruction and GRAM accessing format of 80-system 16-bit interface are shown in **Figure 8-3** and **Figure 8-4**, respectively.

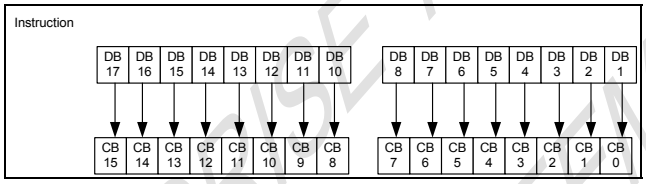


Figure 8-3

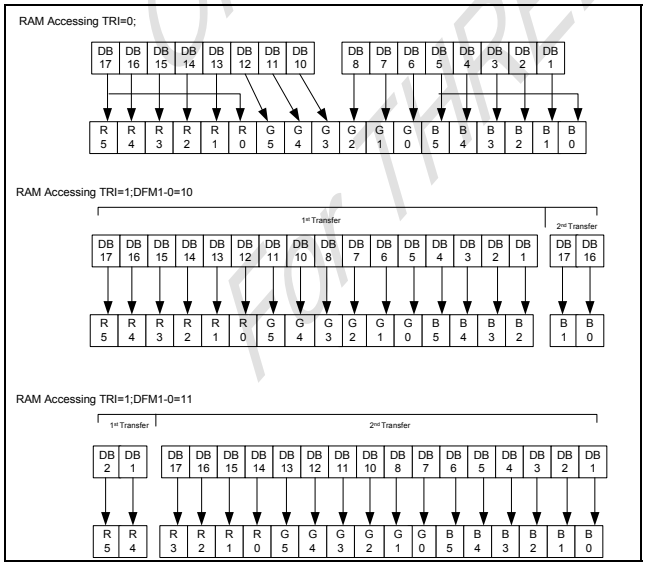


Figure 8-4

8.1.3. 80-system 9-bit interface

The instruction and GRAM accessing format of 80-system 9-bit interface are shown in **Figure 8-5** and **Figure 8-6**, respectively.

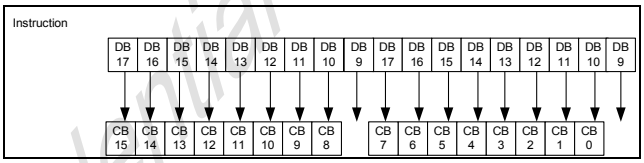


Figure 8-5

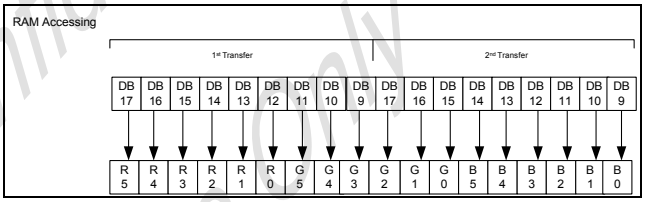


Figure 8-6

8.1.4. 80-system 8-bit interface

The instruction and GRAM accessing format of 80-system 8-bit interface are shown in **Figure 8-7** and **Figure 8-8**, respectively.

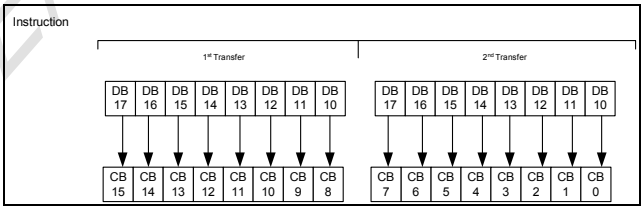


Figure 8-7

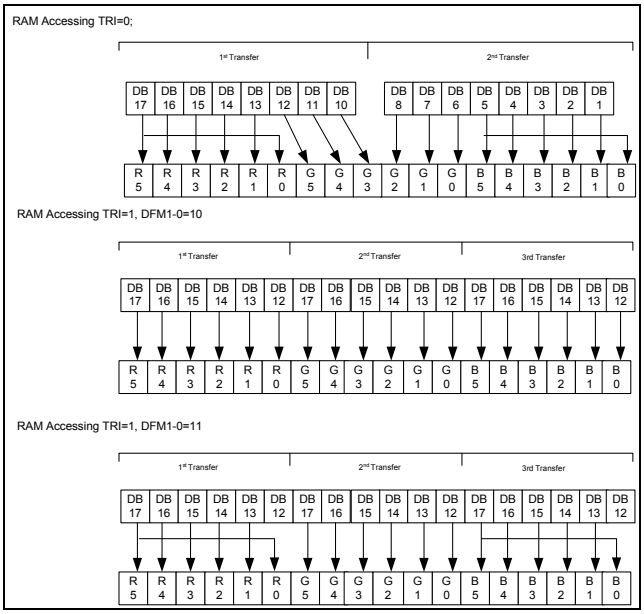


Figure 8-8

8.1.5. Serial Peripheral interface (SPI)

The system interface of SPFD5408A also includes the Serial Peripheral Interface (SPI). In SPI mode, /CS, SCL, SDI and SDO are used to transfer data between MCU and SPDFD5406A. IM0/ID pin served as the ID pin. **Figure 8-9** illustrates the detail timing while using SPI. Be aware that the unused pins such as DB17-0 pins must be fixed at either IOVcc or GND level.

The instruction and GRAM accessing format of SPI interface are shown in **Figure 8-10** and Figure 8-11, respectively.

When read operation is desired In SPI mode, valid data are read out as the SPFD5408A reads out the 6th byte data from the internal GRAM. The RAM data transfer in SPI mode, in SPI mode with TRI=1/ DFM1-0=10 and status read are illustrated in Figure 8-12, **Figure 8-13** and **Figure 8-14**, respectively.

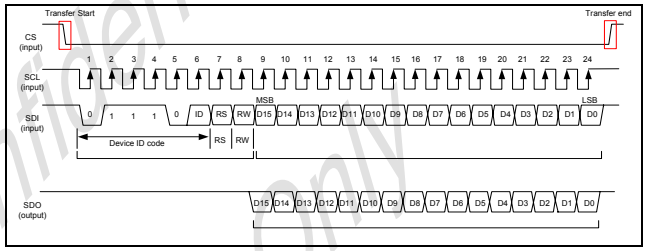


Figure 8-9

Start Byte Format

Transferred bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note 1) ID bit is selected by setting the IM0/ID pin.

RS	R/W	Function
0	0	Set an index register
0	1	Read a status
1	0	Write an instruction or RAM data
1	1	Read an instruction or RAM data

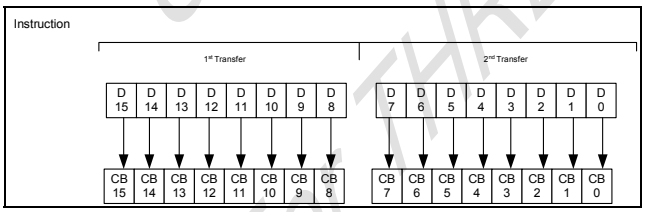


Figure 8-10

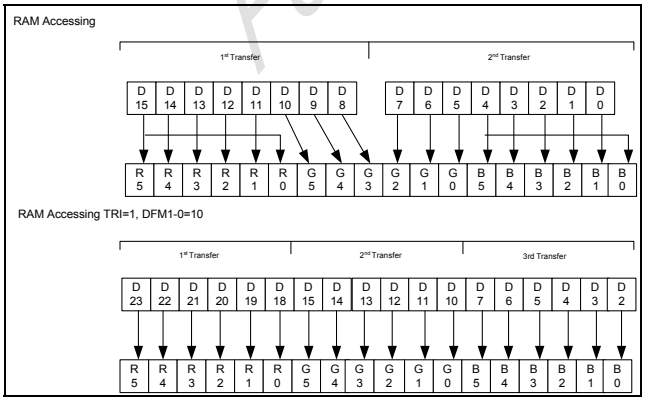


Figure 8-11

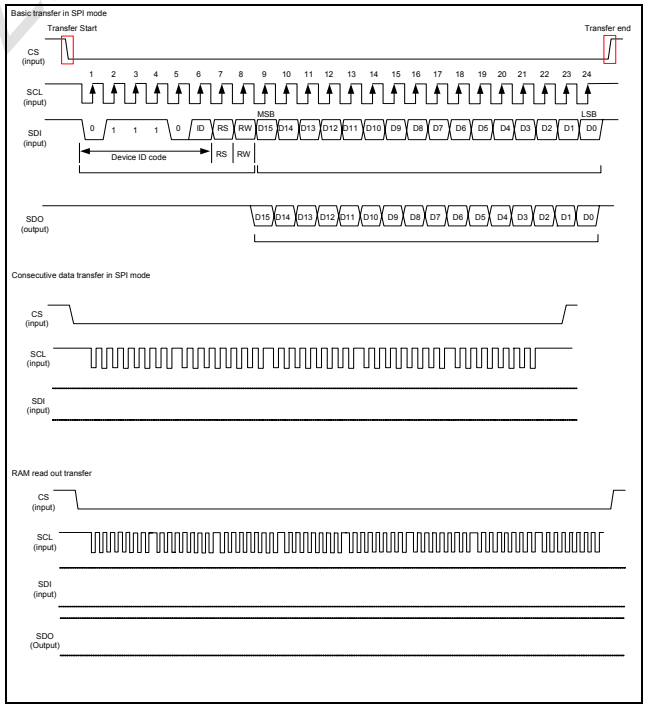


Figure 8-12

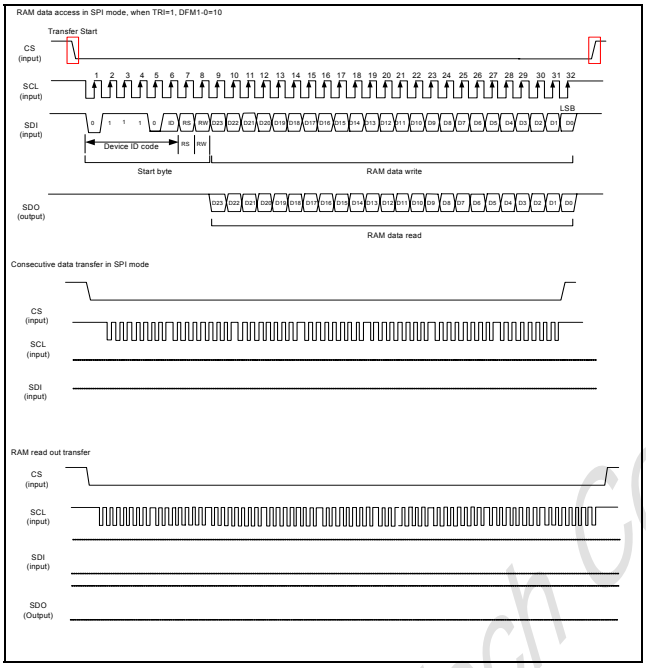


Figure 8-13

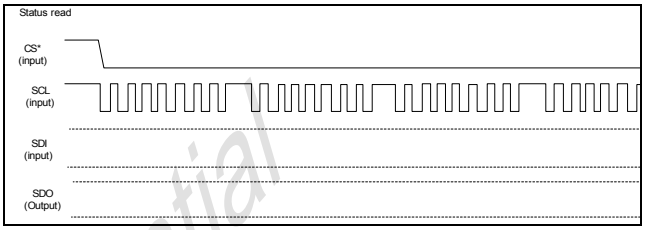


Figure 8-14

8.2. VSYNC Interface

The SPFD5408A also supports VSYNC interface for moving picture display, which is the system interface in synchronization with the frame-synchronizing signal (VSYNC). The VSYNC interface can display a moving picture without tremendous modification.

DM1-0 = “10” and RM = “0” can initialized VSYNC interface. In VSYNC interface mode, the internal display operation is synchronized with the VSYNC signal. In VSYNC interface mode, the graphic data are stored in GRAM to minimize the data transfer to overwrite on the moving picture GRAM area. **Figure 8-15** illustrates moving picture data transfer through VSYNC interface.

In VSYNC mode, Internal operation is executed in synchronization with the internal clock generated from internal oscillators and VSYNC input. Therefore the frame rate is determined by the frequency of VSYNC. SPFD5408A can access the internal RAM in high speed with less power consumption in VSYNC interface mode while using high-speed write mode

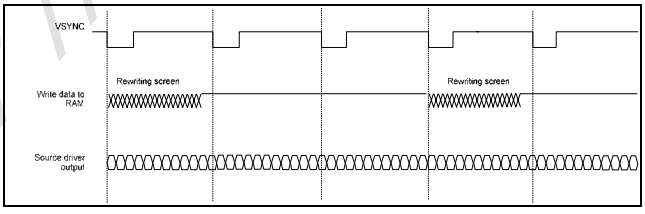


Figure 8-15

In VSYNC interface mode, the formula for Internal clock frequency and frame rate is shown below:

Input clock frequency = FrameRate x (DisplayLines) + FrontPorch + BackPorch x 16 x variance

Due to the possible cause of variances while set the internal clock frequency; be sure to complete the display operation in one VSYNC cycle.

8.3. External Display Interface

SPFD5408A also includes external (RGB) interface for displaying moving picture. External interface can be set by RIM1-0 bit. **Table 8-3** summarized the corresponding types of RGB interface with RIM1-0 setting.

Table 8-3

RIM1	RIM0	RGB Interface	DB Pin
0	0	18-bit RGB interface	DB17-0
0	1	16-bit RGB interface	DB17-10, 8-1
1	0	6-bit RGB interface	DB17-12
1	1	Setting disabled	

RGB interface cab access SPFD5408A by VSYNC, HSYNC, ENABLE, DOTCLK and DB17-0 signals, where VSYNC is used for frame synchronization; HSYNC is used for line synchronization and ENABLE is served as the valid data synchronized signals. The RGB interface can be rewriting minimum necessary data to the GRAM area which need to be overwritten with use of window address function and high-speed write mode. It is necessary for RGB interface to set front and back porch periods after and before a display period, respectively. **Figure 8-16** illustrates the general timing for RGB interface. There are some constrain while using RGB interface. The following summarized the conditions

(a) Partial display/ scroll function / interlace and graphics operation function are not available for RGB interface

(b) In RGB interface VSYNC, HSYNC, and DOTCLK signals must be input through a display operation period.

(c) The setting of the NO1-0 bits, STD1-0 bits and EQ1-0 bits are based on DOTCLK in RGB interface mode. In 6-bit RGB interface mode, it takes 3 DOTCLK inputs to transfer one pixel. Be aware data transfer in units of 3 DOTCLK inputs in 6-bit RGB interface mode is necessary. Set the cycle of each signal in 6-bit interface mode (VSYNC, HSYNC ENABLE, DB17-0) to input 3x clock to complete data transfer in units of pixels.

(d) In RGB-I/F mode, while writing data to the internal RAM make sure to use the high-speed write mode (HWM = “1” or LHWM = “1”)

(e) In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.

(f) In RGB interface mode, a GRAM address (AD15-0) is set in the address counter every frame on the falling edge of VSYNC.

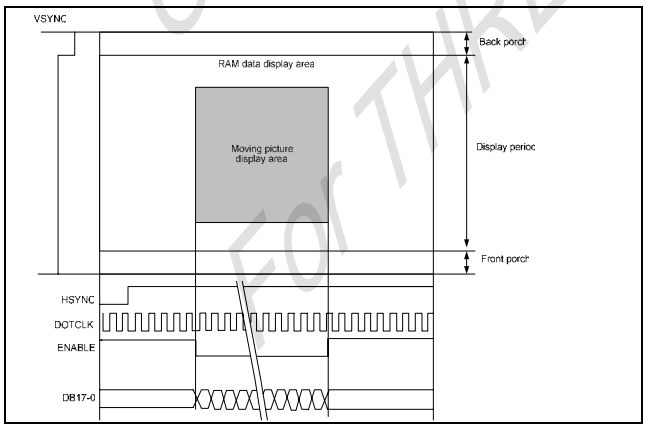


Figure 8-16

RGB interface includes ENABLE signal served as valid data synchronized signals. Moreover, the active level for ENABLE can be set by EPL. The EPL bit inverts the polarity of ENABLE signal. **Table 8-4** summarized the setting of EPL and ENABLE active level for GRAM accessing. Setting both EPL and ENABLE bits to automatically update RAM address in the AC is necessary while writing data to the GRAM.

Table 8-4

EPL	ENABLE	RAM Write	RAM Address
0	0	Enabled	Updated
0	1	Disenabled	Retained
1	0	Disenabled	Retained
1	1	Enabled	Updated

SPFD5408A can support 18-bit, 16-bit and 6-bit RGB interface. The detail timing diagram for 18-bit, 16-bit and 6-bit RGB interface are shown in **Figure 8-17** and **Figure 8-18** respectively.

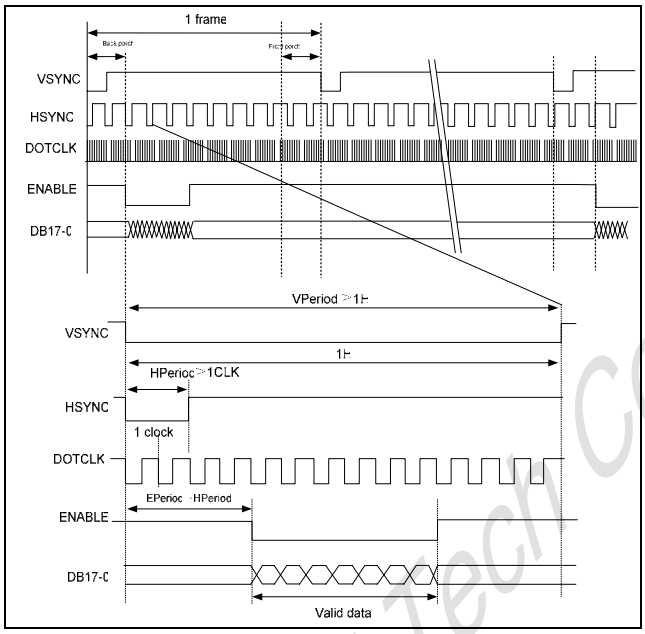


Figure 8-17

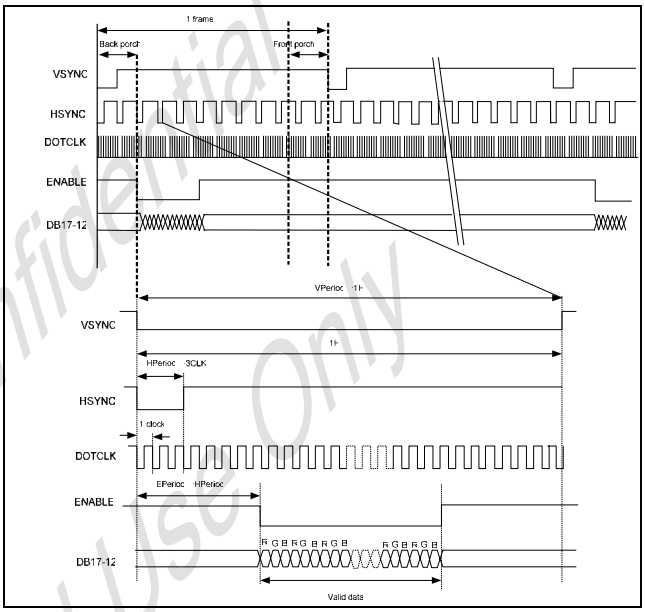


Figure 8-18

The RGB interface also has the window address function to transfer only minimum necessary data on the moving picture GRAM area, which can lower the power consumption and still can use system interface to rewrite data in still picture RAM area while displaying a moving picture. Setting RM = 0 while in RGB interface mode can make GRAM accessCBle through the system interface. When RGB interface accessing GRAM is desired, wait for one read/write bus cycle following by RM = 1 setting.

Figure 8-19 illustrates the timing diagram when displaying a moving picture through the RGB interface and rewriting data in the still picture GRAM area through the system interface.

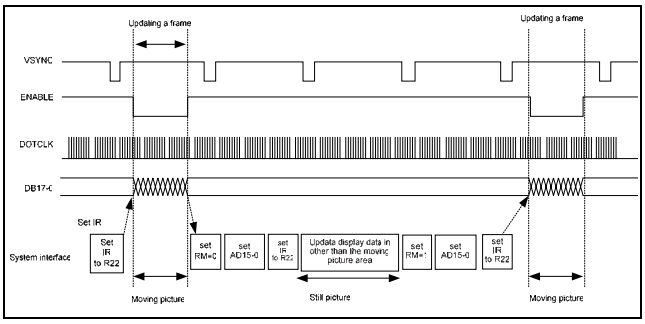


Figure 8-19

8.3.1. 6-bit RGB interface

RAM accessing format and data transmission synchronization of 6-bit RGB interface are shown in **Figure 8-20** and **Figure 8-21**, respectively.

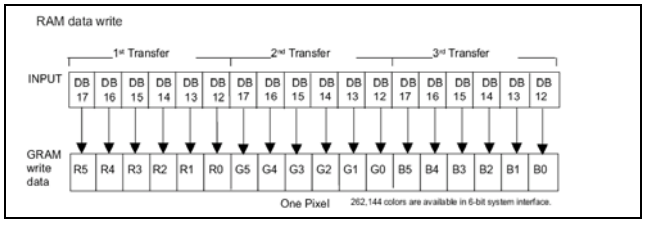


Figure 8-20

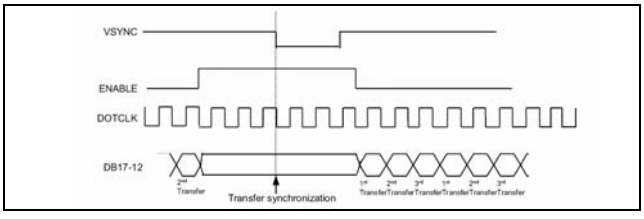


Figure 8-21

8.3.2. 16-bit RGB interface

RAM accessing format of 16-bit RGB interface are shown in **Figure 8-22**.

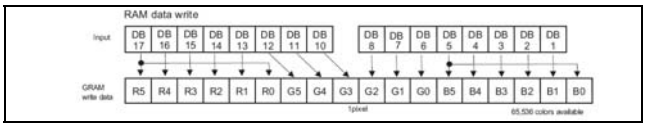


Figure 8-22

8.3.3. 18-bit RGB interface

RAM accessing format of 18-bit RGB interface are shown in **Figure 8-23**.

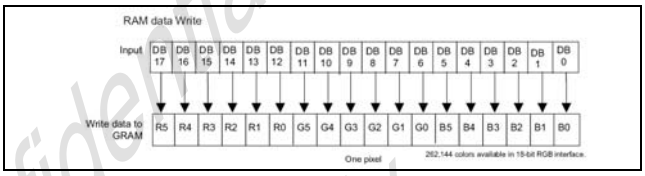


Figure 8-23

9. Display Feature Function:

9.1. FMARK function:

SPFDF5408A provided FMARK function which output signal to alert host MCU via FMARK I/O pad so that LCd display can avoid flicker effect. FMARK output position and onterval can be set by FMP[8:0] and FMI[2:0], respectively.

Figure 9.1.1 illustrated the FMARK output position when FMP[8:0]=9'h008.

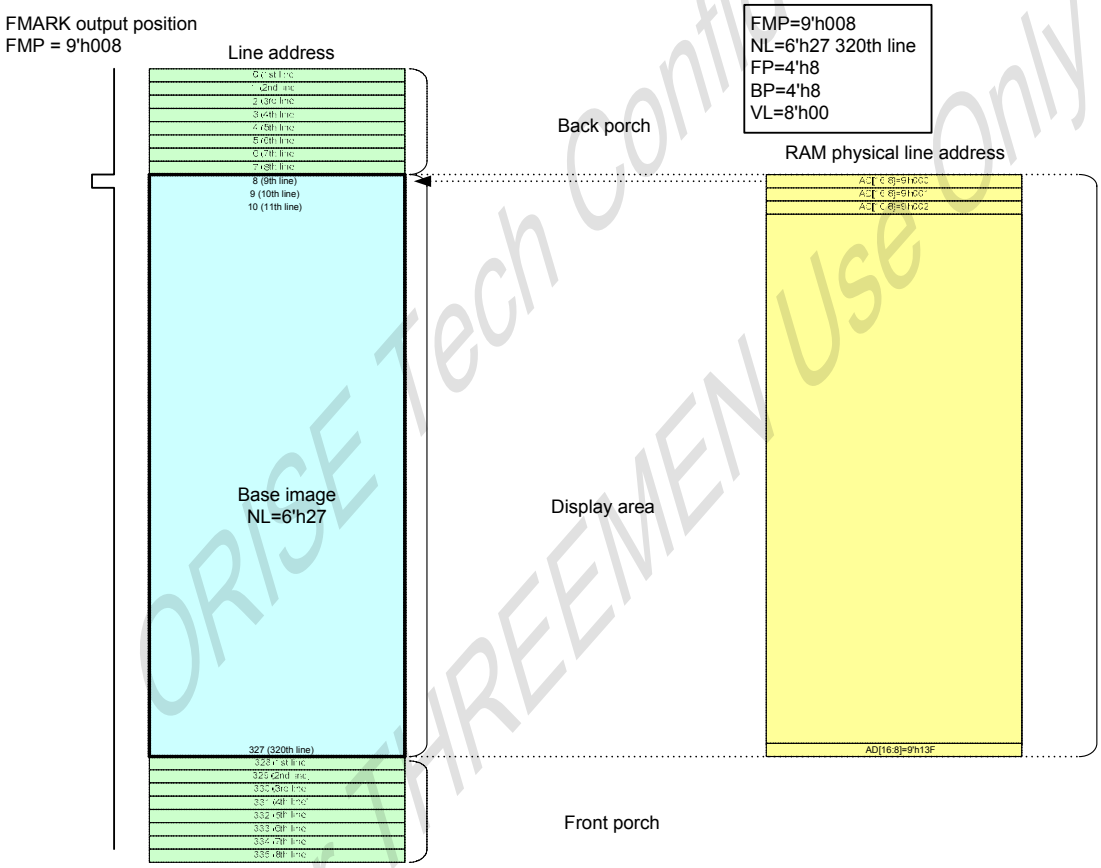
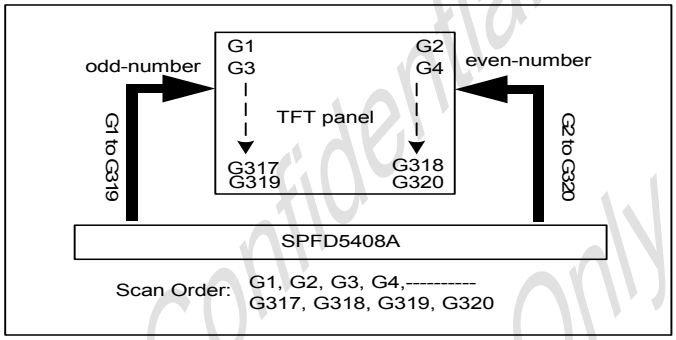
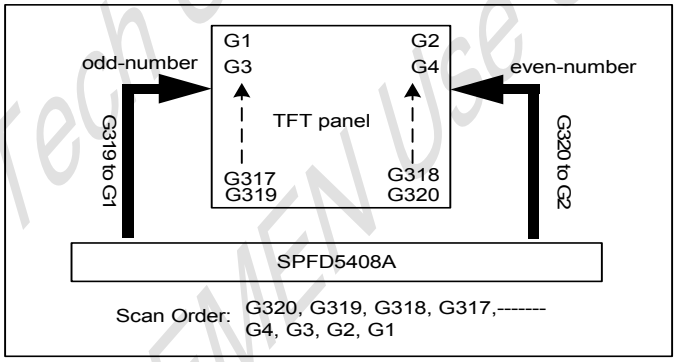
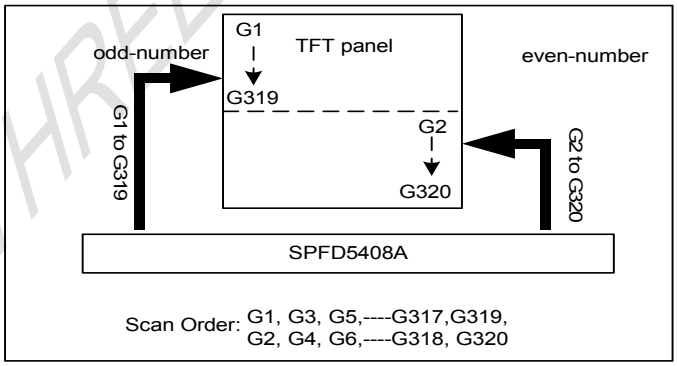
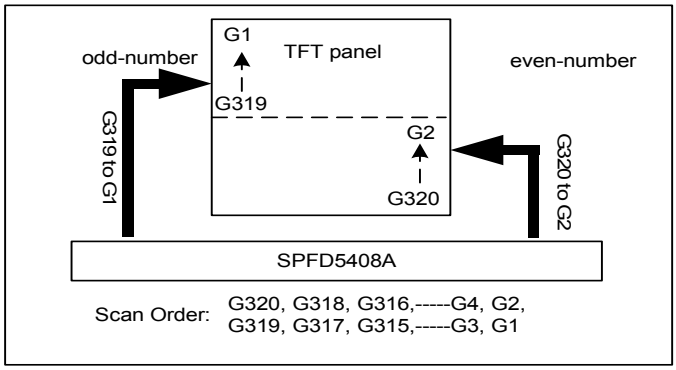


Figure 9.1.1 Example of FMARK signal.

9.2. Scan Mode function:

SM	GS	Scan Direction
0	0	
0	1	
1	0	
1	1	

9.3. Scalling function:

SPFD5408 provides scalling function to resize the disaply area. The Sccalling factor can be set via RSZ[1:0] (register R04h, CB [1:0]). Table summarized the RSZ[1:0] function. The image after scalling can be displayed at the area set by (HAS, HEA, VSA, VFA).

Table 9.3.1

RSZ[1:0]	Scalling Factor	Actual resolution (original input data 240xRGbx320)
00	No scalling	240xRGBx320
01	1/2 scalling	120xRGBx160
10	Setting Disable	-
11	1/4 scalling	60xRGBx80

Table 9.3.2 illustrated the data arrangement when scalling factor is 1/2, RSZ[1:0]=”01”

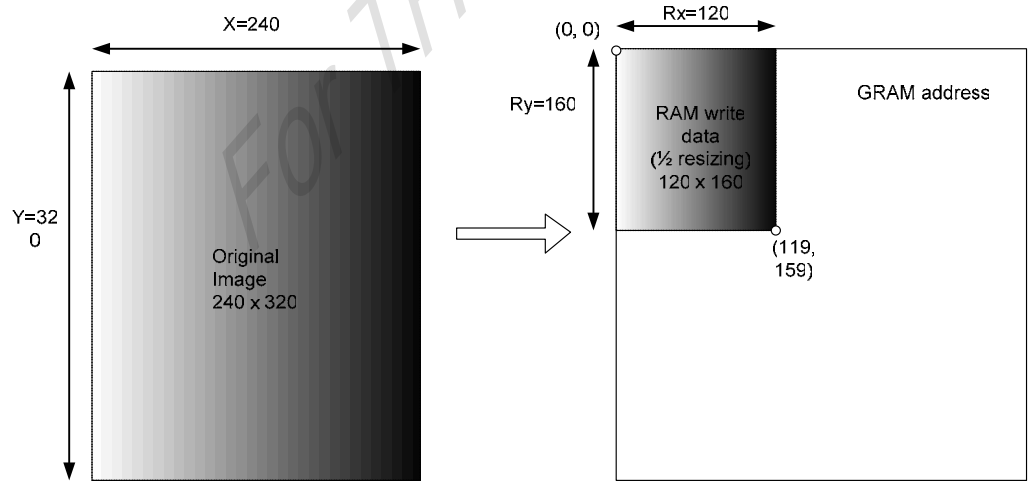
	1	2	3	4	5	6	7	8
1	A1	A2	A3	A4	A5	A6	A7	A8
2	B1	B2	B3	B4	B5	B6	B7	B8
3	C1	C2	C3	C4	C5	C6	C7	C8
4	D1	D2	D3	D4	D5	D6	D7	D8
5	E1	E2	E3	E4	E5	E6	E7	E8
6	F1	F2	F3	F4	F5	F6	F7	F8
7	G1	G2	G3	G4	G5	G6	G7	G8
8	H1	H1	H3	H4	H5	H6	H7	H8

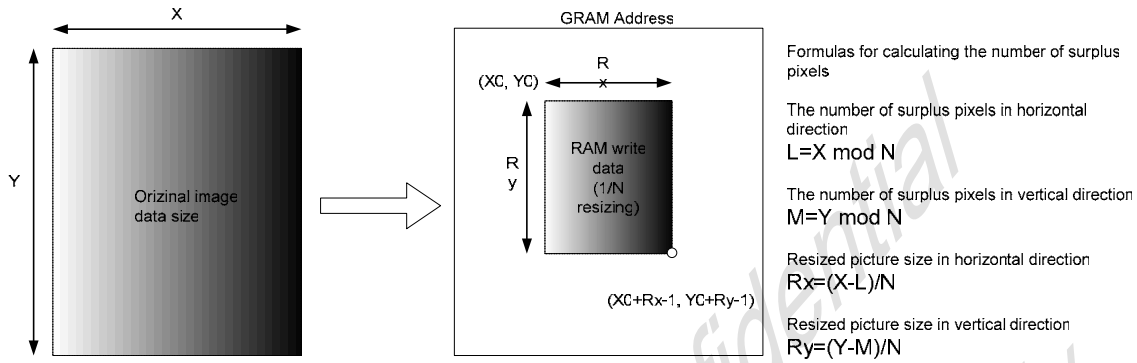
↓

	1	2	3	4
1	A1	A3	A5	A7
2	C1	C3	C5	C7
3	E1	E3	E5	E7
4	G1	G3	G5	G7

Table 9.3.2 data arrangment

Figure 9.3.1 illustrated the example when scalling factor is 1/2, RSZ[1:0]=”01”





Formulas for calculating the number of surplus pixels

The number of surplus pixels in horizontal direction

L=X mod N

The number of surplus pixels in vertical direction

M=Y mod N

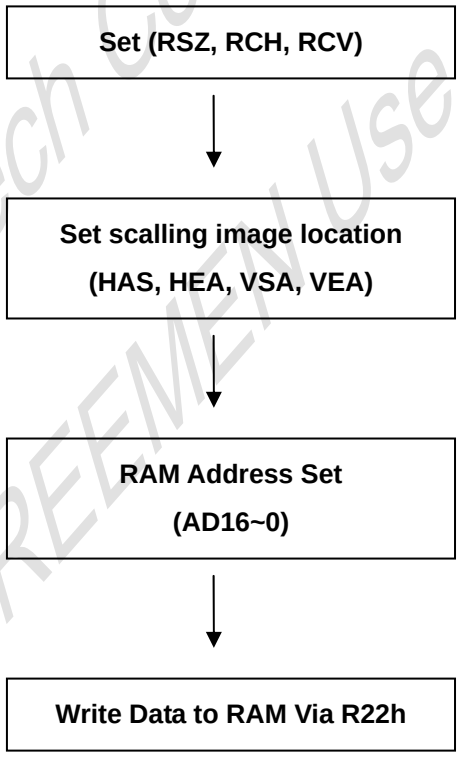
Resized picture size in horizontal direction

Rx=(X-L)/N

Resized picture size in vertical direction

Ry=(Y-M)/N

The flow chart to use scalling function:



9.4. Partial Display function:

SPFD5408 has partial display function feature which can provide only partial display for power saving purpose. Partial display function can be accessed by setting BSEE="0",. Moreover, 2 partial display area (partial image 1/ partial image 2) can be initialized by setted PTDE0="1" and PTDE1="1", respectively. The partial display area for partial image 1 and partial 2 can be set by PTSA0 / PTEA0 and PTSA1/ PTEA1, respectively. Table 9.4.1 and Figure 9.4.1 summarized the full and partial display function.

Case	Function Setting	Display area setting	Display Position
Full dsiplay	**BASEE="1" PTDE0="x" PTDE1="x"**	**(BSA,BEA)**	**-**
Partail image1:0n Partial image2:Off	**BASEE="0" PTDE0="1" PTDE1="0"**	**(PTSA0,PTEA0)**	**PTDP0**
Partail image1:Off Partial image2:On	**BASEE="0" PTDE0="0" PTDE1="1"**	**(PTSA1,PTEA1)**	**PTDP1**
Partail image1:On Partial image2:On	**BASEE="0" PTDE0="1" PTDE1="1"**	**(PTSA0,PTEA0) (PTSA1,PTEA1)**	**PTDP0 & PTDP1**

Table 9.4.1 Partial display function summary table

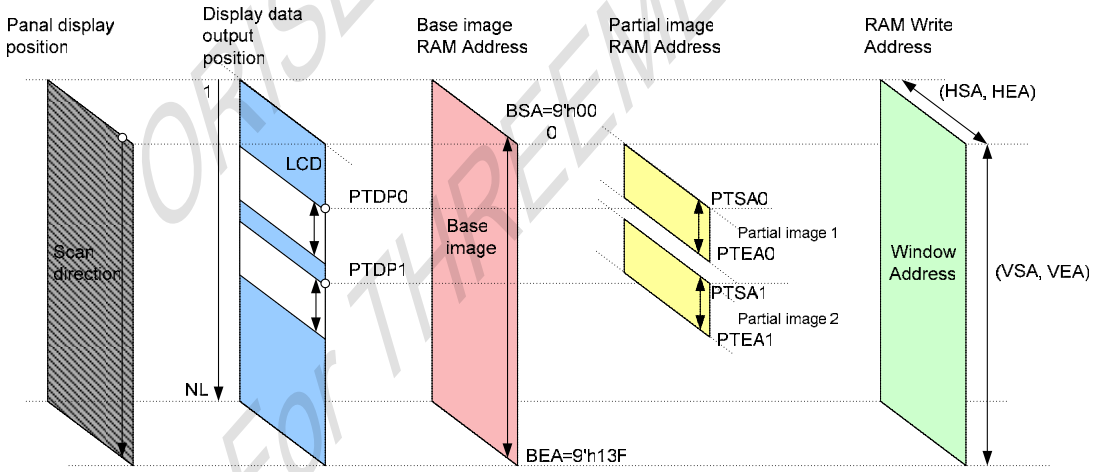


Figure 9.4.1 Partial display function diagram

Figure 9.4.2 indicated the case of NL[5:0] setting is < 6'h27 which active line is less than 320. Partial display image data can stored in not active area.

Figure 9.4.3 indicated the partial display area start position. The partial display area and start position can be set by (**PTSA0, PTEA0 , PTSA1, PTEA1) and (PTDP0, PTDP1), respectively.**

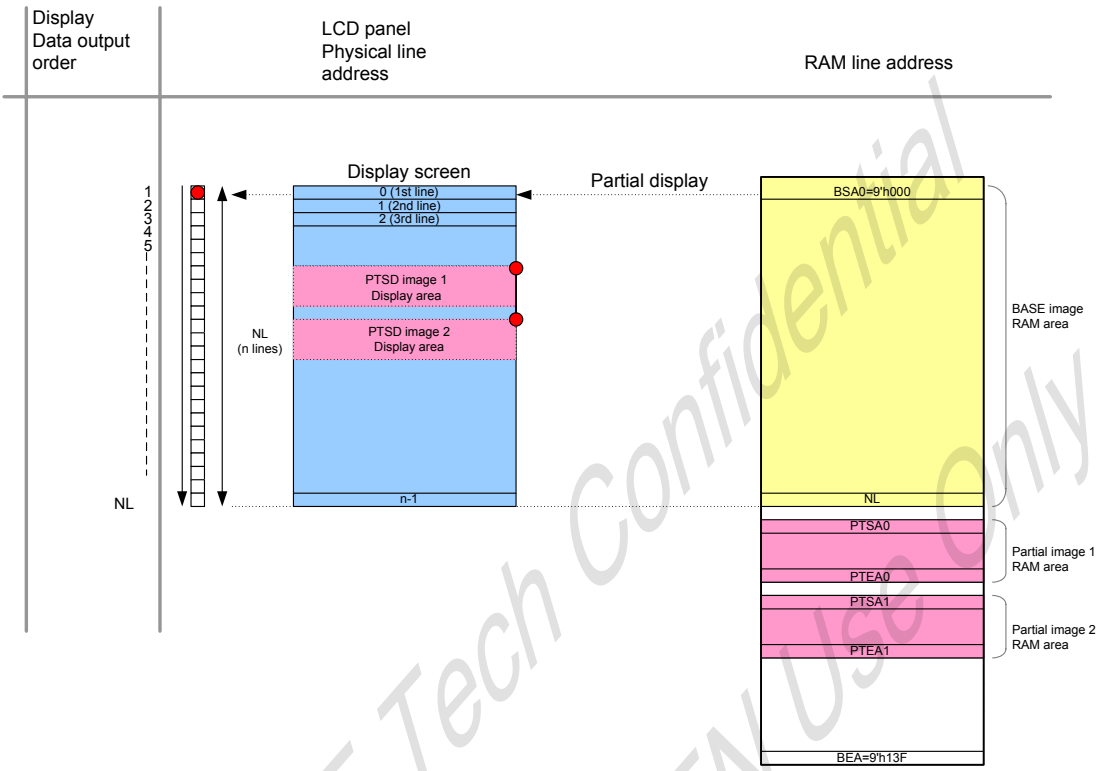


Figure 9.4.2 Example of NL[5:0] setting is < 6'h27 case

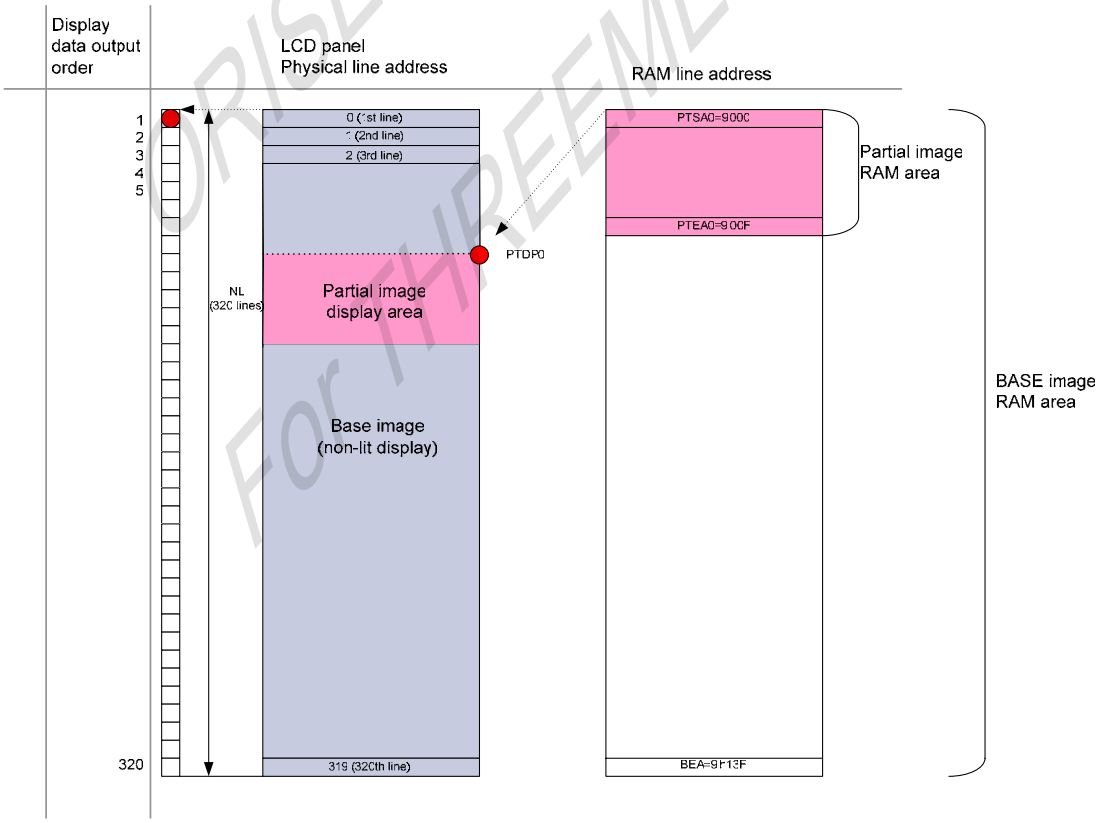


Figure 9.4.3 indicated the partial display area start position.

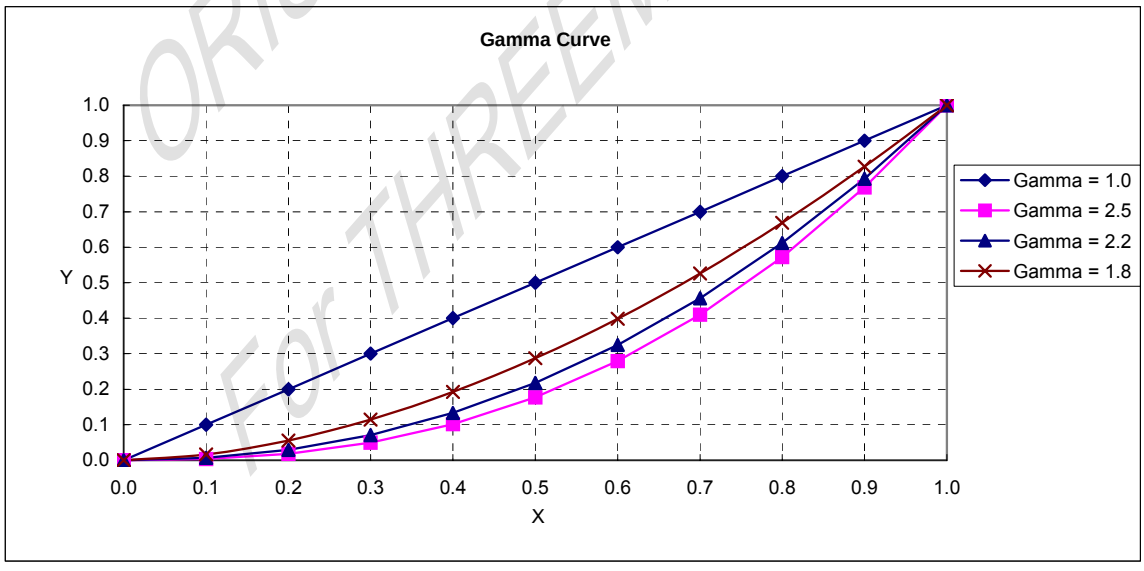
9.5. Gamma Correction function:

SPFD54508A adopt Gamma voltage generation circuit which can provide wider output voltage range to fit the difrerent kind of liquid crystal for Gamma curve from 1.0~2.5. The Gamma output voltage can be set by R30h!~R3Fh.

V1RP[4:0]: register for positive VSD0 fine tune adjustment.
V2RP[5:0]: register for positive VSD1 fine tune adjustment.
V3RP[5:0]: register for positive VSD2 fine tune adjustment.
V4RP[5:0]: register for positive VSD61 fine tune adjustment.
V5RP[5:0]: register for positive VSD62 fine tune adjustment.
V6RP[4:0]: register for positive VSD63 fine tune adjustment
V7RP[4:0]: register for positive VSD13 fine tune adjustment
V8RP[4:0]: register for positive VSD50 fine tune adjustment
V9RP[3:0]: register for positive VSD4 fine tune adjustment
V10RP[3:0]: register for positive VSD8 fine tune adjustment
V11RP[3:0]: register for positive VSD20 fine tune adjustment
V12RP[3:0]: register for positive VSD27 fine tune adjustment
V13RP[3:0]: register for positive VSD364 fine tune adjustment
V14RP[3:0]: register for positive VSD43 fine tune adjustment
V15RP[3:0]: register for positive VSD55 fine tune adjustment
V16RP[3:0]: register for positive VSD59 fine tune adjustment

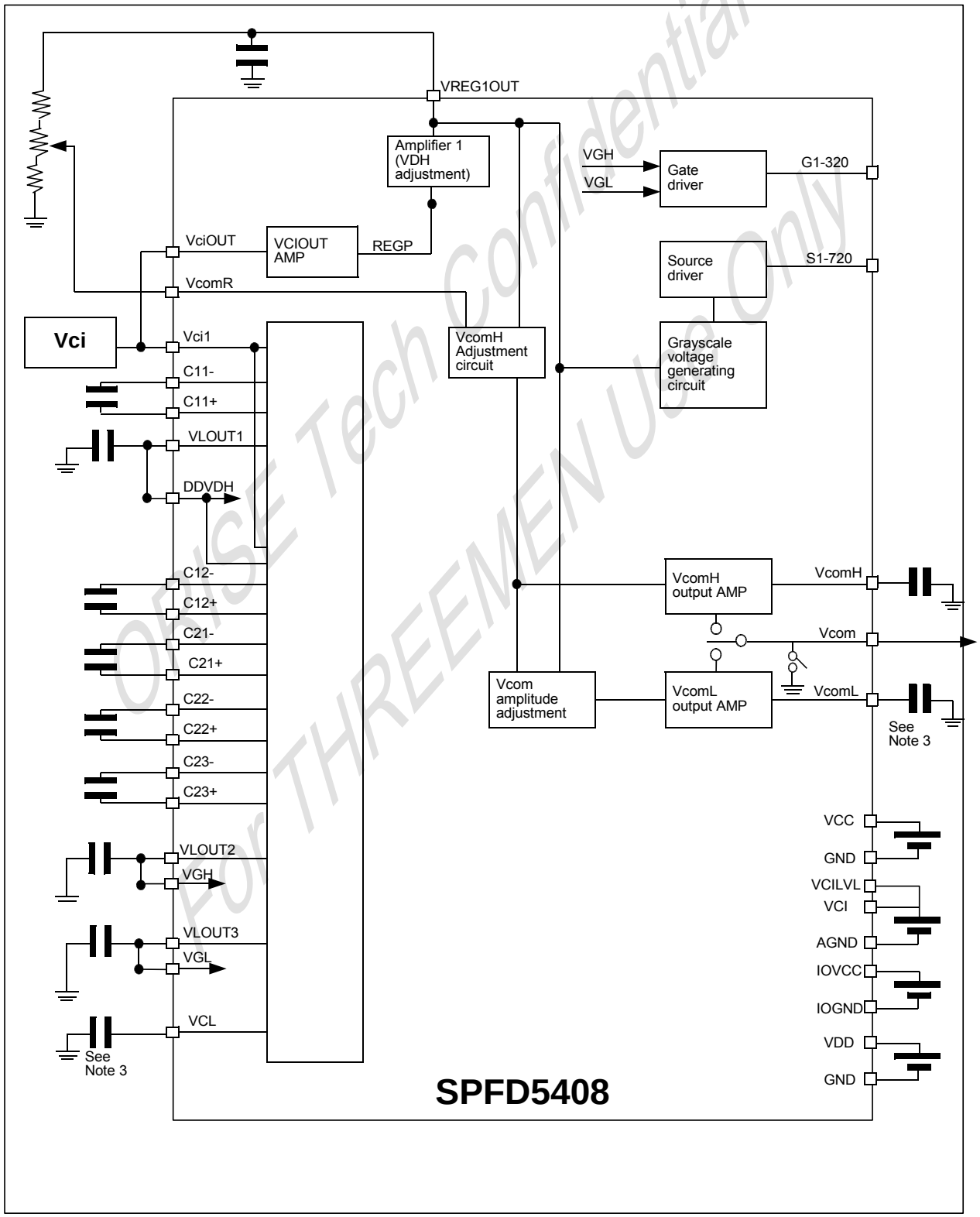
V1RN[4:0]: register for negative VSD0 fine tune adjustment.
V2RN[5:0]: register for negative VSD1 fine tune adjustment.
V3RN[5:0]: register for negative VSD2 fine tune adjustment.
V4RN[5:0]: register for negative VSD61 fine tune adjustment.
V5RN[5:0]: register for negative VSD62 fine tune adjustment.
V6RN[4:0]: register for negative VSD63 fine tune adjustment
V7RN[4:0]: register for negative VSD13 fine tune adjustment
V8RN[4:0]: register for negative VSD50 fine tune adjustment
V9RN[3:0]: register for negative VSD4 fine tune adjustment
V10RN[3:0]: register for negative VSD8 fine tune adjustment
V11RN[3:0]: register for negative VSD20 fine tune adjustment
V12RN[3:0]: register for negative VSD27 fine tune adjustment
V13RN[3:0]: register for negative VSD364 fine tune adjustment
V14RN[3:0]: register for negative VSD43 fine tune adjustment
V15RN[3:0]: register for negative VSD55 fine tune adjustment
V16RN[3:0]: register for negative VSD59 fine tune adjustment

Figure 9.5.1 illustrated 4 diffrerent Gamma Curve.

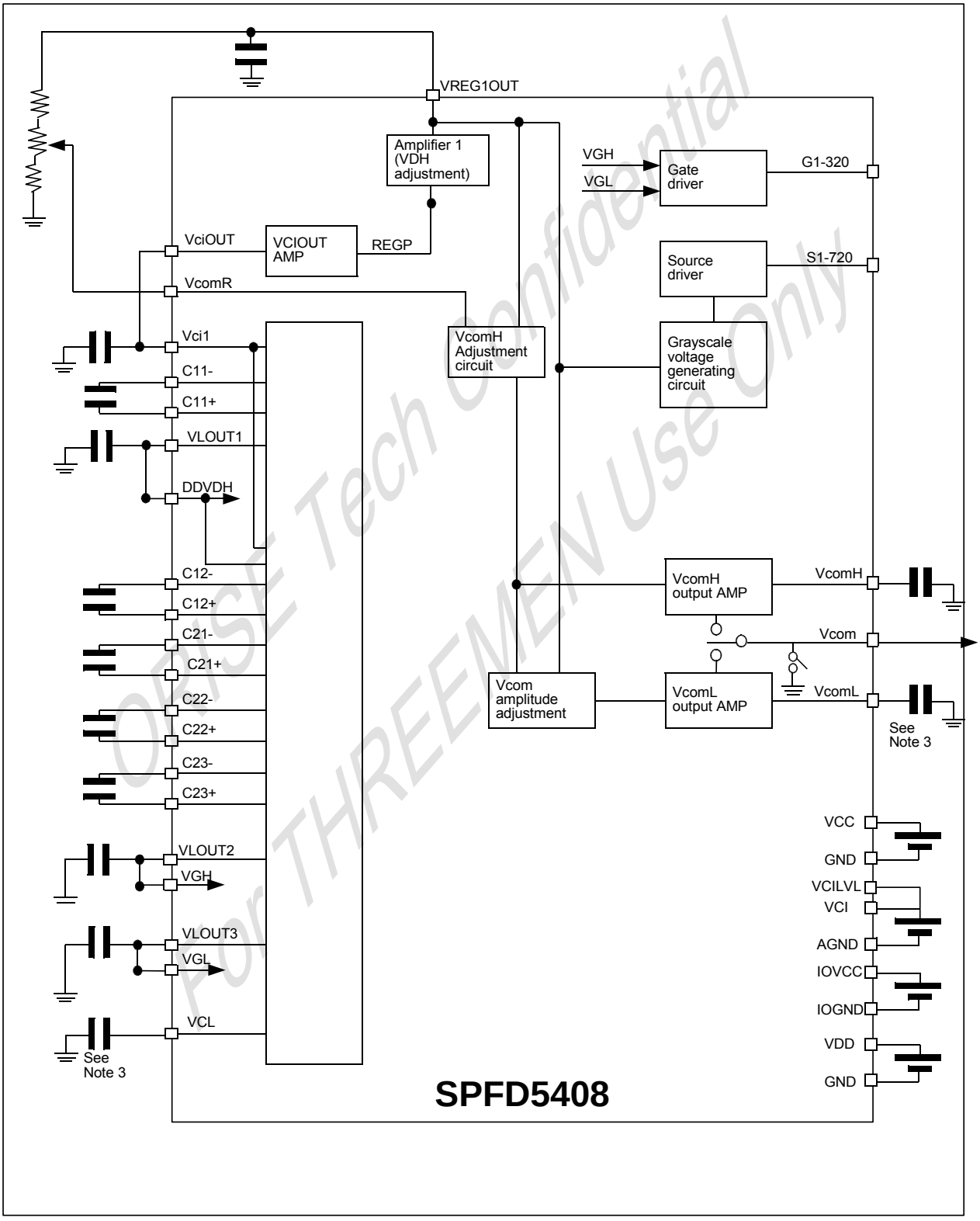


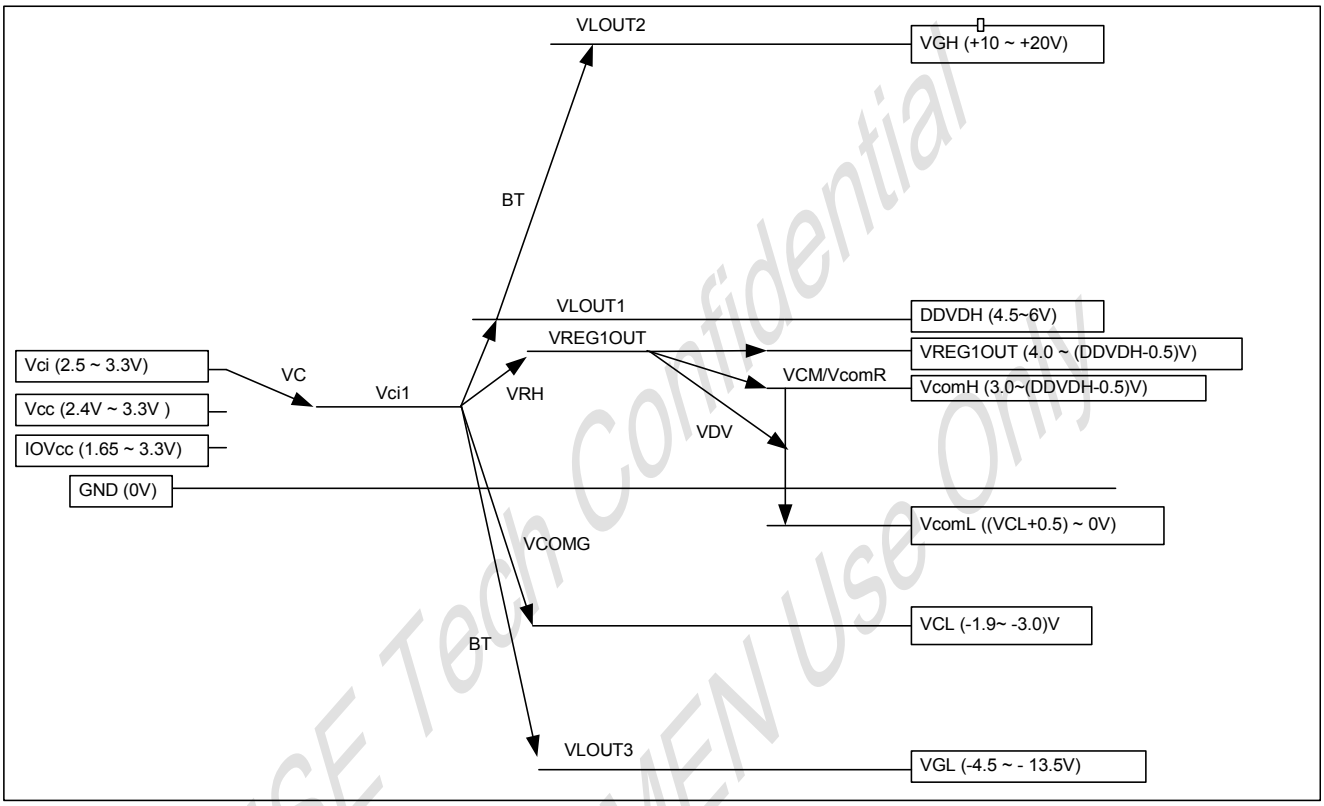
10. Power Management System:

(a) VCI1=VCI direct input:

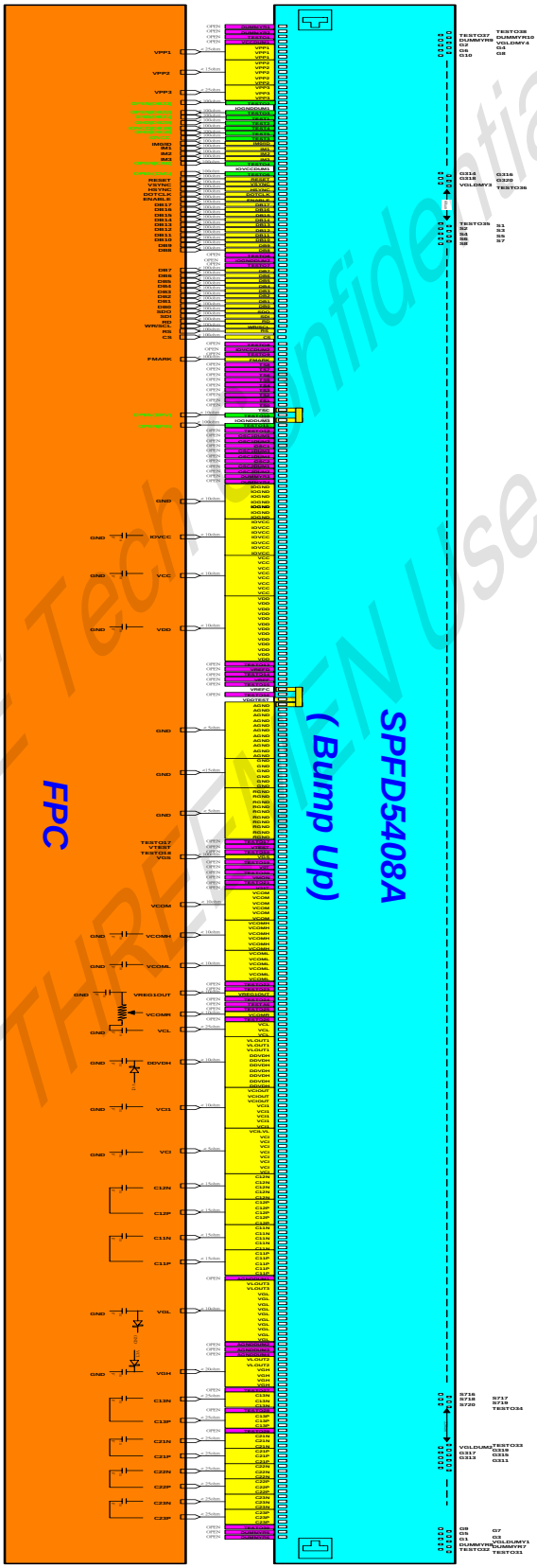


(b) VCI1=VCIOUT:





11. Application circuits:



12. Initial Code:

Step	Register Address	Register Value	Note
1	R00h	0x0001h	
2	R01h	0x0000h	
3	R02h	0x0701h	
4	R03h	0xD010h	
5	R04h	0x0000h	
6	R08h	0x0207h	
7	R09h	0x0000h	
8	R0Ah	0x0000h	
9	R0Ch	0x0000h	
10	R0Dh	0x0000h	
11	R0Fh	0x0000h	
12	R07h	0x0101h	
13	R10h	0x10B0h	
14	R11h	0x0007h	
15	R17h	0x0001h	
16	R12h	0x013Bh	
17	R13h	0x0B00h	
18	R29h	0x0012h	
19	R2Ah	0x0095h	
20	R50h	0x0000h	
21	R51h	0x00EFh	
22	R52h	0x0000h	
23	R53h	0x013Fh	
24	R60h	0x2700h	
25	R61h	0x0001h	
26	R6Ah	0x0000h	
27	R80h	0x0000h	
28	R81h	0x0021h	
29	R82h	0x0061h	
30	R83h	0x0173h	
31	R84h	0x0000h	
32	R85h	0x0000h	
33	R90h	0x0013h	
34	R92h	0x0000h	
35	R93h	0x0103h	
36	R95h	0x0110h	
37	R97h	0x0000h	
38	R98h	0x0000h	
39	RF0h	0x5408h	
40	RF3h	0x0010h	
41	RF4h	0x0011h	
42	RF0h	0x0000h	
43	R07h	0x0173	

Note: This initial code is not including Gamma setting. Please contact Orise Technology for desired Gamma setting.

13. Electrical Characteristics:

13.1. Absolute Maximum Ratings:

Table 13-1

Item	Symbol	Unit	Value	Note
Power Supply Voltage1	VCC,IOVCC	V	-0.3 ～+4.6	
Power Supply Voltage 2	VCI – AGND	V	-0.3 ～+4.6	
Power Supply Voltage 3	DDVDH – AGND	V	-0.3 ～+6.5	
Power Supply Voltage4	AGND – VCL	V	-0.3 ～+4.6	
Power Supply Voltage 5	DDVDH – VCL	V	-0.3 ～+9.0	
Power Supply Voltage7	AGND – VGL	V	-0.3 ～+14.0	
Power Supply Voltage 8	VGH– VGL	V	-0.3 ～+30.0	
Input Voltage	Vt	V	-0.3 ～IOVCC + 0.3	
Operating Temperature	Topr	℃	-40 ～+85	
Storage Temperature	Tstg	℃	-55 ～+110	

13.2. DC Characteristics

Table 13-2

VCC= 2.50V～3.30V，IOVCC=1.65V～ 3.30V，Ta=-40℃～+85℃

Item	Sym bol	Unit	Test Condition	Mi n.	Typ.	Max.	Note
Input High level voltage	VIH	V	IOVCC=1.65V～3.30V	0.8xIOVCC	-	IOVCC	
Input Low level voltage	VIL	V	IOVCC=1.65V～3.30V	-0.3	-	0.2xIOVCC	
Output ”High” level voltage 1 （DB0-17）	VOH	V	IOVCC=1.65V～3.30V, IOH=-0.1mA	0.8xIOVCC	-	-	
Output ”Low” level voltage 1 （DB0-17）	VOL	V	IOVCC=1.65V～3.30V, IOL=0.1mA	-	-	0.2xIOVCC	
I/O leak current	ILI	μA	Vin=0～IOVCC	-1	-	1	
Current Consumption (IOVCC-IOGND)+(VCC-GND) Normal operation mode (262k-colors, display operation)	IOP1	μA	fosc=376kHz (320line drive), IOVCC=VCC=3.00V fFLM=70Hz Ta=25℃ RAM data: 18’h000000	-	175	-	
Current Consumption (IOVCC-IOGND)+(VCC-GND) 8-color mode, 64-line, partial display operation	Iop2	μA	fosc=376kHz (64-line, partial display), IOVCC=VCC=3.00V , fFLM=40Hz Ta=25℃ RAM data: 18h’000000	-	140	-	

13.3. AC Characteristics

VCC= 2.50V～3.30V，IOVCC=1.65V～3.30V，Ta=-40℃～+85℃

13.3.1. Clock Characteristics

Table13-3

Item	Symbol	Unit	Timing Diagram	Min.	Typ.	Max.	Note
RC Oscillation clock	fosc	kHz	IOVCC = VCC = 3.0V, 25°C	338	376	414	9

13.3.2. 80-System Bus Interface Timing Characteristics (18-/ 16- bit interface)

Table 13-4 Normal write operation (HWM=0 or 1), IOVCC=1.65V~3.30V

Item	Symbol		Unit	Min.	Typ.	Max.
Bus cycle time	Write	tCYCW	ns	125	-	-
	Read	tCYCR	ns	450	-	-
Write low-level pulse width		PWLW	ns	45	-	-
Read low-level pulse width		PWLR	ns	170	-	-
Write high-level pulse width		PWHW	ns	70	-	-
Read high-level pulse width		PWHR	ns	250	-	-
Write/Read rise/ fall time		tWRr, WRf	ns	-	-	25
Setup time	Write (RS to CS*,WR*)	tAS	ns	0	-	-
	Read (RS to CS*, RD*)		ns	10	-	-
Address Hold Time		tAH	ns	2	-	-
Write data setup time		tDSW	ns	25	-	-
Write data hold time		tH	ns	10	-	-
Read data delay time		tDDR	ns	-	-	150
Read data hold time		tDHR	ns	5	-	-

13.3.3. Clock-synchronized Serial Interface Timing Characteristics

Normal Write Function (HWM=0), High-speed Write Function (HWM=1), IOVCC=1.65~3.30V)

Table 13-5

Item	Symbol		Unit	Min.	Typ.	Max.
SerialTime Clock Cycle	Write (received)	tSCYC	ns	100	-	20.000
	Read (transmitted)	tSCYC	ns	350	-	20.000
Serial Clock high-level width	Write (received)	tSCH	ns	40	-	-
	Read (transmitted)	tSCH	ns	150	-	-
Serial Clock low-level width	Write (received)	tSCL	ns	40	-	-
	Read (transmitted)	tSCL	ns	150	-	-
Serial clock rise/fall time		tSCr, tSCf	ns	-	-	20
Chip select setup time		tCSU	ns	20	-	-
Chip select hold time		tCH	ns	60	-	-
Serial input data setup time		tSISU	ns	30	-	-
Serial input data hold time		tSIH	ns	30	-	-
Serial output data delay time		tSOD	ns	-	-	130
Serial output data hold time		tSOH	ns	5	-	-

13.3.4. Reset Timing Characteristics (IOVCC=1.65~3.30V)

Table 13-6

Item	Symbol	Unit	Min.	Typ.	Max.
Reset low-level width	tRES	ms	1	—	—
Reset rise time	trRES	μs	—	—	10

13.3.5. RGB Interface Timing Characterics

18-/ 16- bit RGB interface (HWM=0 or 1), IOVCC=1.65~3.30V

Table 14-7

Item	Symbol	Unit	Min.	Typ.	Max.
VSYNC/HSYNC Setup time	TSYNCS	clock	0	-	1
ENABLE Setup time	TENS	ns	10	-	-
ENABLE Hold time	TENH	ns	20	-	-
DOTCLK low-level pulse width	PWDL	ns	40	-	-
DOTCLK high-level pulse width	PWDH	ns	40	-	-
DOTCLK cycle time	TCYCD	ns	100	-	-
Data setup time	TPDS	ns	10	-	-
Data hold time	TPDH	ns	40	-	-
DOTCLK, VSYNC and HSYNC rise/fall time	Trgbr Trgbf	ns	-	-	25

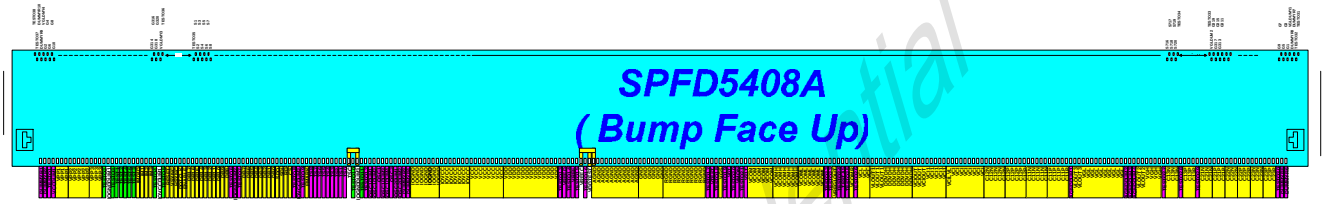
6-bit RGB interface (HWM=0 or 1), IOVCC=1.65~3.30V

Table 14-8

Item	Symbol	Unit	Min.	Typ.	Max.
VSYNC/HSYNC setup time	TSYNCS	clock	0	-	1
ENABLE setup time	TENS	ns	10	-	-
ENABLE hold time	TENH	ns	25	-	-
DOTCLK low-level pulse width	PWDL	ns	25	-	-
DOTCLK high-level pulse width	PWDH	ns	25	-	-
DOTCLK cycle time	TCYCD	ns	60	-	-
Data setup-time	TPDS	ns	10	-	-
Data hold time	TPDH	ns	25	-	-
DOTCLK, VSYNC, and HSYNC rise/fall time	Trgb Ttrgbf	ns	-	-	25

14. CHIP INFORMATION

14.1. PAD Assignment



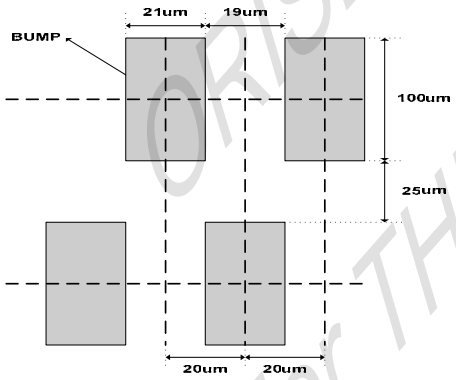
14.2. PAD Dimension

Item	PAD No.	Size		Unit
		X	Y	
Chip Size	-	21560	830	μm
Chip thickness	-	400		
Pad pitch	1~298	70	-	
	299~1354	20	125	
Bumped pad size	1~298	50	80	
	299~1354	21	100	

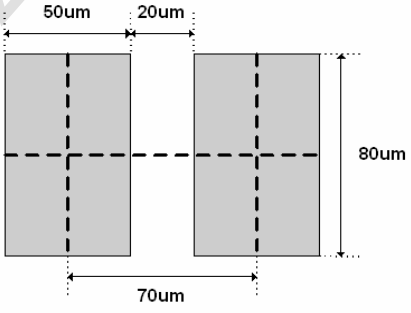
Note1: Chip size included scribe line.

14.3. Bump Dimension

14.3.1. Output Pads



14.3.2. Input Pads



14.4. PAD Locations

NO.	PAD Name	X	Y
1	DUMMYR1	345	65.5
2	DUMMYR2	415	65.5
3	TESTO1	485	65.5
4	VCCDUM1	555	65.5
5	VPP1	625	65.5
6	VPP1	695	65.5
7	VPP1	765	65.5
8	VPP2	835	65.5
9	VPP2	905	65.5
10	VPP2	975	65.5
11	VPP2	1045	65.5
12	VPP2	1115	65.5
13	VPP3	1185	65.5
14	VPP3	1255	65.5
15	VPP3	1325	65.5
16	TESTO2	1395	65.5
17	IOGNDDUM1	1465	65.5
18	TESTO3	1535	65.5
19	TEST1	1605	65.5
20	TEST2	1675	65.5
21	TEST4	1745	65.5
22	TEST5	1815	65.5
23	TEST3	1885	65.5
24	IM0_ID	1955	65.5
25	IM1	2025	65.5
26	IM2	2095	65.5
27	IM3	2165	65.5
28	TESTO4	2235	65.5
29	IOVCCDUM1	2305	65.5
30	TESTO5	2375	65.5
31	RESET	2445	65.5
32	VSYNC	2515	65.5
33	HSYNC	2585	65.5
34	DOTCLK	2655	65.5
35	ENABLE	2725	65.5
36	DB17	2795	65.5
37	DB16	2865	65.5
38	DB15	2935	65.5
39	DB14	3005	65.5
40	DB13	3075	65.5
41	DB12	3145	65.5
42	DB11	3215	65.5
43	DB10	3285	65.5
44	DB9	3355	65.5
45	DB8	3425	65.5
46	TESTO6	3495	65.5
47	IOGNDDUM2	3565	65.5
48	TESTO7	3635	65.5
49	DB7	3705	65.5
50	DB6	3775	65.5
51	DB5	3845	65.5
52	DB4	3915	65.5
53	DB3	3985	65.5
54	DB2	4055	65.5
55	DB1	4125	65.5
56	DB0	4195	65.5
57	SDO	4265	65.5
58	SDI	4335	65.5
59	RD	4405	65.5
60	WR_SCL	4475	65.5
61	RS	4545	65.5
62	CS	4615	65.5
63	TESTO8	4685	65.5
64	IOVCCDUM2	4755	65.5
65	TESTO9	4825	65.5
66	FMARK	4895	65.5
67	TS8	4965	65.5
68	TS7	5035	65.5
69	TS6	5105	65.5
70	TS5	5175	65.5
71	TS4	5245	65.5
72	TS3	5315	65.5
73	TS2	5385	65.5
74	TS1	5455	65.5
75	TS0	5525	65.5
76	TSC	5595	65.5
77	TESTO10	5665	65.5
78	IOGNDDUM3	5735	65.5
79	TESTO11	5805	65.5
80	TESTO12	5875	65.5
81	OSC1DUM1	5945	65.5
82	OSC1DUM2	6015	65.5
83	OSC1	6085	65.5
84	OSC1DUM3	6155	65.5
85	OSC1DUM4	6225	65.5
86	OSC2	6295	65.5
87	OSC2DUM1	6365	65.5
88	OSC2DUM2	6435	65.5
89	DUMMYR3	6505	65.5
90	DUMMYR4	6575	65.5
91	GND	6645	65.5
92	GND	6715	65.5
93	GND	6785	65.5
94	GND	6855	65.5
95	GND	6925	65.5
96	GND	6995	65.5
97	GND	7065	65.5
98	IOVCC	7135	65.5
99	IOVCC	7205	65.5
100	IOVCC	7275	65.5
101	IOVCC	7345	65.5
102	IOVCC	7415	65.5
103	IOVCC	7485	65.5
104	IOVCC	7555	65.5
105	VCC	7625	65.5
106	VCC	7695	65.5
107	VCC	7765	65.5
108	VCC	7835	65.5
109	VCC	7905	65.5
110	VCC	7975	65.5
111	VCC	8045	65.5
112	VCC	8115	65.5
113	VDD	8185	65.5
114	VDD	8255	65.5
115	VDD	8325	65.5
116	VDD	8395	65.5
117	VDD	8465	65.5
118	VDD	8535	65.5
119	VDD	8605	65.5
120	VDD	8675	65.5
121	VDD	8745	65.5
122	VDD	8815	65.5
123	VDD	8885	65.5
124	VDD	8955	65.5
125	VDD	9025	65.5
126	TESTO13	9095	65.5
127	VREFD	9165	65.5
128	TESTO14	9235	65.5
129	VREF	9305	65.5
130	TESTO15	9375	65.5
131	VREFC	9445	65.5
132	TESTO16	9515	65.5
133	VDDTEST	9585	65.5
134	AGND	9655	65.5
135	AGND	9725	65.5
136	AGND	9795	65.5
137	AGND	9865	65.5
138	AGND	9935	65.5
139	AGND	10005	65.5
140	AGND	10075	65.5
141	AGND	10145	65.5
142	AGND	10215	65.5
143	AGND	10285	65.5
144	AGND	10355	65.5
145	GND	10425	65.5
146	GND	10495	65.5
147	GND	10565	65.5
148	GND	10635	65.5
149	GND	10705	65.5
150	GND	10775	65.5
151	RGND	10845	65.5
152	RGND	10915	65.5
153	RGND	10985	65.5
154	RGND	11055	65.5
155	RGND	11125	65.5
156	RGND	11195	65.5
157	RGND	11265	65.5
158	RGND	11335	65.5
159	RGND	11405	65.5

NO.	PAD Name	X	Y
160	RGND	11475	65.5
161	TESTO17	11545	65.5
162	VTEST	11615	65.5
163	TESTO18	11685	65.5
164	VGS	11755	65.5
165	TESTO19	11825	65.5
166	V0T	11895	65.5
167	TESTO20	11965	65.5
168	VMON	12035	65.5
169	TESTO21	12105	65.5
170	V31T	12175	65.5
171	VCOM	12245	65.5
172	VCOM	12315	65.5
173	VCOM	12385	65.5
174	VCOM	12455	65.5
175	VCOM	12525	65.5
176	VCOM	12595	65.5
177	VCOMH	12665	65.5
178	VCOMH	12735	65.5
179	VCOMH	12805	65.5
180	VCOMH	12875	65.5
181	VCOMH	12945	65.5
182	VCOMH	13015	65.5
183	VCOML	13085	65.5
184	VCOML	13155	65.5
185	VCOML	13225	65.5
186	VCOML	13295	65.5
187	VCOML	13365	65.5
188	VCOML	13435	65.5
189	TESTO22	13505	65.5
190	TESTO23	13575	65.5
191	VREG1OUT	13645	65.5
192	TESTO24	13715	65.5
193	TESTA5	13785	65.5
194	TESTO25	13855	65.5
195	VCOMR	13925	65.5
196	TESTO26	13995	65.5
197	VCL	14065	65.5
198	VCL	14135	65.5
199	VCL	14205	65.5
200	VLOUT1	14275	65.5
201	VLOUT1	14345	65.5
202	VLOUT1	14415	65.5
203	DDVDH	14485	65.5
204	DDVDH	14555	65.5
205	DDVDH	14625	65.5
206	DDVDH	14695	65.5
207	DDVDH	14765	65.5
208	DDVDH	14835	65.5
209	DDVDH	14905	65.5
210	VCIOUT	14975	65.5
211	VCIOUT	15045	65.5
212	VCIOUT	15115	65.5
213	VCI1	15185	65.5
214	VCI1	15255	65.5

NO.	PAD Name	X	Y
215	VCI1	15325	65.5
216	VCI1	15395	65.5
217	VCI1	15465	65.5
218	VCILVL	15535	65.5
219	VCI	15605	65.5
220	VCI	15675	65.5
221	VCI	15745	65.5
222	VCI	15815	65.5
223	VCI	15885	65.5
224	VCI	15955	65.5
225	VCI	16025	65.5
226	VCI	16095	65.5
227	C12N	16165	65.5
228	C12N	16235	65.5
229	C12N	16305	65.5
230	C12N	16375	65.5
231	C12N	16445	65.5
232	C12P	16515	65.5
233	C12P	16585	65.5
234	C12P	16655	65.5
235	C12P	16725	65.5
236	C12P	16795	65.5
237	C11N	16865	65.5
238	C11N	16935	65.5
239	C11N	17005	65.5
240	C11N	17075	65.5
241	C11N	17145	65.5
242	C11P	17215	65.5
243	C11P	17285	65.5
244	C11P	17355	65.5
245	C11P	17425	65.5
246	C11P	17495	65.5
247	AGNDDUM1	17565	65.5
248	VLOUT3	17635	65.5
249	VLOUT3	17705	65.5
250	VGL	17775	65.5
251	VGL	17845	65.5
252	VGL	17915	65.5
253	VGL	17985	65.5
254	VGL	18055	65.5
255	VGL	18125	65.5
256	VGL	18195	65.5
257	VGL	18265	65.5
258	VGL	18335	65.5
259	VGL	18405	65.5
260	AGNDDUM2	18475	65.5
261	AGNDDUM3	18545	65.5
262	AGNDDUM4	18615	65.5
263	VLOUT2	18685	65.5
264	VLOUT2	18755	65.5
265	VGH	18825	65.5
266	VGH	18895	65.5
267	VGH	18965	65.5
268	VGH	19035	65.5
269	TESTO27	19105	65.5

NO.	PAD Name	X	Y
270	C13N	19175	65.5
271	C13N	19245	65.5
272	C13N	19315	65.5
273	TESTO28	19385	65.5
274	C13P	19455	65.5
275	C13P	19525	65.5
276	C13P	19595	65.5
277	TESTO29	19665	65.5
278	C21N	19735	65.5
279	C21N	19805	65.5
280	C21N	19875	65.5
281	C21P	19945	65.5
282	C21P	20015	65.5
283	C21P	20085	65.5
284	C22N	20155	65.5
285	C22N	20225	65.5
286	C22N	20295	65.5
287	C22P	20365	65.5
288	C22P	20435	65.5
289	C22P	20505	65.5
290	C23N	20575	65.5
291	C23N	20645	65.5
292	C23N	20715	65.5
293	C23P	20785	65.5
294	C23P	20855	65.5
295	C23P	20925	65.5
296	TESTO30	20995	65.5
297	DUMMYR5	21065	65.5
298	DUMMYR6	21135	65.5
299	TESTO31	21410	664.5
300	TESTO32	21390	539.5
301	DUMMYR7	21370	664.5
302	DUMMYR8	21350	539.5
303	VGLDMY1	21330	664.5
304	G1	21310	539.5
305	G3	21290	664.5
306	G5	21270	539.5
307	G7	21250	664.5
308	G9	21230	539.5
309	G11	21210	664.5
310	G13	21190	539.5
311	G15	21170	664.5
312	G17	21150	539.5
313	G19	21130	664.5
314	G21	21110	539.5
315	G23	21090	664.5
316	G25	21070	539.5
317	G27	21050	664.5
318	G29	21030	539.5
319	G31	21010	664.5
320	G33	20990	539.5
321	G35	20970	664.5
322	G37	20950	539.5
323	G39	20930	664.5
324	G41	20910	539.5

NO.	PAD Name	X	Y
325	G43	20890	664.5
326	G45	20870	539.5
327	G47	20850	664.5
328	G49	20830	539.5
329	G51	20810	664.5
330	G53	20790	539.5
331	G55	20770	664.5
332	G57	20750	539.5
333	G59	20730	664.5
334	G61	20710	539.5
335	G63	20690	664.5
336	G65	20670	539.5
337	G67	20650	664.5
338	G69	20630	539.5
339	G71	20610	664.5
340	G73	20590	539.5
341	G75	20570	664.5
342	G77	20550	539.5
343	G79	20530	664.5
344	G81	20510	539.5
345	G83	20490	664.5
346	G85	20470	539.5
347	G87	20450	664.5
348	G89	20430	539.5
349	G91	20410	664.5
350	G93	20390	539.5
351	G95	20370	664.5
352	G97	20350	539.5
353	G99	20330	664.5
354	G101	20310	539.5
355	G103	20290	664.5
356	G105	20270	539.5
357	G107	20250	664.5
358	G109	20230	539.5
359	G111	20210	664.5
360	G113	20190	539.5
361	G115	20170	664.5
362	G117	20150	539.5
363	G119	20130	664.5
364	G121	20110	539.5
365	G123	20090	664.5
366	G125	20070	539.5
367	G127	20050	664.5
368	G129	20030	539.5
369	G131	20010	664.5
370	G133	19990	539.5
371	G135	19970	664.5
372	G137	19950	539.5
373	G139	19930	664.5
374	G141	19910	539.5
375	G143	19890	664.5
376	G145	19870	539.5
377	G147	19850	664.5
378	G149	19830	539.5
379	G151	19810	664.5
380	G153	19790	539.5
381	G155	19770	664.5
382	G157	19750	539.5
383	G159	19730	664.5
384	G161	19710	539.5
385	G163	19690	664.5
386	G165	19670	539.5
387	G167	19650	664.5
388	G169	19630	539.5
389	G171	19610	664.5
390	G173	19590	539.5
391	G175	19570	664.5
392	G177	19550	539.5
393	G179	19530	664.5
394	G181	19510	539.5
395	G183	19490	664.5
396	G185	19470	539.5
397	G187	19450	664.5
398	G189	19430	539.5
399	G191	19410	664.5
400	G193	19390	539.5
401	G195	19370	664.5
402	G197	19350	539.5
403	G199	19330	664.5
404	G201	19310	539.5
405	G203	19290	664.5
406	G205	19270	539.5
407	G207	19250	664.5
408	G209	19230	539.5
409	G211	19210	664.5
410	G213	19190	539.5
411	G215	19170	664.5
412	G217	19150	539.5
413	G219	19130	664.5
414	G221	19110	539.5
415	G223	19090	664.5
416	G225	19070	539.5
417	G227	19050	664.5
418	G229	19030	539.5
419	G231	19010	664.5
420	G233	18990	539.5
421	G235	18970	664.5
422	G237	18950	539.5
423	G239	18930	664.5
424	G241	18910	539.5
425	G243	18890	664.5
426	G245	18870	539.5
427	G247	18850	664.5
428	G249	18830	539.5
429	G251	18810	664.5
430	G253	18790	539.5
431	G255	18770	664.5
432	G257	18750	539.5
433	G259	18730	664.5
434	G261	18710	539.5
435	G263	18690	664.5
436	G265	18670	539.5
437	G267	18650	664.5
438	G269	18630	539.5
439	G271	18610	664.5
440	G273	18590	539.5
441	G275	18570	664.5
442	G277	18550	539.5
443	G279	18530	664.5
444	G281	18510	539.5
445	G283	18490	664.5
446	G285	18470	539.5
447	G287	18450	664.5
448	G289	18430	539.5
449	G291	18410	664.5
450	G293	18390	539.5
451	G295	18370	664.5
452	G297	18350	539.5
453	G299	18330	664.5
454	G301	18310	539.5
455	G303	18290	664.5
456	G305	18270	539.5
457	G307	18250	664.5
458	G309	18230	539.5
459	G311	18210	664.5
460	G313	18190	539.5
461	G315	18170	664.5
462	G317	18150	539.5
463	G319	18130	664.5
464	VGLDMY2	18110	539.5
465	TESTO33	18090	664.5
466	TESTO34	17870	664.5
467	S720	17850	539.5
468	S719	17830	664.5
469	S718	17810	539.5
470	S717	17790	664.5
471	S716	17770	539.5
472	S715	17750	664.5
473	S714	17730	539.5
474	S713	17710	664.5
475	S712	17690	539.5
476	S711	17670	664.5
477	S710	17650	539.5
478	S709	17630	664.5
479	S708	17610	539.5
480	S707	17590	664.5
481	S706	17570	539.5
482	S705	17550	664.5
483	S704	17530	539.5
484	S703	17510	664.5
485	S702	17490	539.5
486	S701	17470	664.5
487	S700	17450	539.5
488	S699	17430	664.5
489	S698	17410	539.5

NO.	PAD Name	X	Y
490	S697	17390	664.5
491	S696	17370	539.5
492	S695	17350	664.5
493	S694	17330	539.5
494	S693	17310	664.5
495	S692	17290	539.5
496	S691	17270	664.5
497	S690	17250	539.5
498	S689	17230	664.5
499	S688	17210	539.5
500	S687	17190	664.5
501	S686	17170	539.5
502	S685	17150	664.5
503	S684	17130	539.5
504	S683	17110	664.5
505	S682	17090	539.5
506	S681	17070	664.5
507	S680	17050	539.5
508	S679	17030	664.5
509	S678	17010	539.5
510	S677	16990	664.5
511	S676	16970	539.5
512	S675	16950	664.5
513	S674	16930	539.5
514	S673	16910	664.5
515	S672	16890	539.5
516	S671	16870	664.5
517	S670	16850	539.5
518	S669	16830	664.5
519	S668	16810	539.5
520	S667	16790	664.5
521	S666	16770	539.5
522	S665	16750	664.5
523	S664	16730	539.5
524	S663	16710	664.5
525	S662	16690	539.5
526	S661	16670	664.5
527	S660	16650	539.5
528	S659	16630	664.5
529	S658	16610	539.5
530	S657	16590	664.5
531	S656	16570	539.5
532	S655	16550	664.5
533	S654	16530	539.5
534	S653	16510	664.5
535	S652	16490	539.5
536	S651	16470	664.5
537	S650	16450	539.5
538	S649	16430	664.5
539	S648	16410	539.5
540	S647	16390	664.5
541	S646	16370	539.5
542	S645	16350	664.5
543	S644	16330	539.5
544	S643	16310	664.5

NO.	PAD Name	X	Y
545	S642	16290	539.5
546	S641	16270	664.5
547	S640	16250	539.5
548	S639	16230	664.5
549	S638	16210	539.5
550	S637	16190	664.5
551	S636	16170	539.5
552	S635	16150	664.5
553	S634	16130	539.5
554	S633	16110	664.5
555	S632	16090	539.5
556	S631	16070	664.5
557	S630	16050	539.5
558	S629	16030	664.5
559	S628	16010	539.5
560	S627	15990	664.5
561	S626	15970	539.5
562	S625	15950	664.5
563	S624	15930	539.5
564	S623	15910	664.5
565	S622	15890	539.5
566	S621	15870	664.5
567	S620	15850	539.5
568	S619	15830	664.5
569	S618	15810	539.5
570	S617	15790	664.5
571	S616	15770	539.5
572	S615	15750	664.5
573	S614	15730	539.5
574	S613	15710	664.5
575	S612	15690	539.5
576	S611	15670	664.5
577	S610	15650	539.5
578	S609	15630	664.5
579	S608	15610	539.5
580	S607	15590	664.5
581	S606	15570	539.5
582	S605	15550	664.5
583	S604	15530	539.5
584	S603	15510	664.5
585	S602	15490	539.5
586	S601	15470	664.5
587	S600	15450	539.5
588	S599	15430	664.5
589	S598	15410	539.5
590	S597	15390	664.5
591	S596	15370	539.5
592	S595	15350	664.5
593	S594	15330	539.5
594	S593	15310	664.5
595	S592	15290	539.5
596	S591	15270	664.5
597	S590	15250	539.5
598	S589	15230	664.5
599	S588	15210	539.5

NO.	PAD Name	X	Y
600	S587	15190	664.5
601	S586	15170	539.5
602	S585	15150	664.5
603	S584	15130	539.5
604	S583	15110	664.5
605	S582	15090	539.5
606	S581	15070	664.5
607	S580	15050	539.5
608	S579	15030	664.5
609	S578	15010	539.5
610	S577	14990	664.5
611	S576	14970	539.5
612	S575	14950	664.5
613	S574	14930	539.5
614	S573	14910	664.5
615	S572	14890	539.5
616	S571	14870	664.5
617	S570	14850	539.5
618	S569	14830	664.5
619	S568	14810	539.5
620	S567	14790	664.5
621	S566	14770	539.5
622	S565	14750	664.5
623	S564	14730	539.5
624	S563	14710	664.5
625	S562	14690	539.5
626	S561	14670	664.5
627	S560	14650	539.5
628	S559	14630	664.5
629	S558	14610	539.5
630	S557	14590	664.5
631	S556	14570	539.5
632	S555	14550	664.5
633	S554	14530	539.5
634	S553	14510	664.5
635	S552	14490	539.5
636	S551	14470	664.5
637	S550	14450	539.5
638	S549	14430	664.5
639	S548	14410	539.5
640	S547	14390	664.5
641	S546	14370	539.5
642	S545	14350	664.5
643	S544	14330	539.5
644	S543	14310	664.5
645	S542	14290	539.5
646	S541	14270	664.5
647	S540	14250	539.5
648	S539	14230	664.5
649	S538	14210	539.5
650	S537	14190	664.5
651	S536	14170	539.5
652	S535	14150	664.5
653	S534	14130	539.5
654	S533	14110	664.5

NO.	PAD Name	X	Y
655	S532	14090	539.5
656	S531	14070	664.5
657	S530	14050	539.5
658	S529	14030	664.5
659	S528	14010	539.5
660	S527	13990	664.5
661	S526	13970	539.5
662	S525	13950	664.5
663	S524	13930	539.5
664	S523	13910	664.5
665	S522	13890	539.5
666	S521	13870	664.5
667	S520	13850	539.5
668	S519	13830	664.5
669	S518	13810	539.5
670	S517	13790	664.5
671	S516	13770	539.5
672	S515	13750	664.5
673	S514	13730	539.5
674	S513	13710	664.5
675	S512	13690	539.5
676	S511	13670	664.5
677	S510	13650	539.5
678	S509	13630	664.5
679	S508	13610	539.5
680	S507	13590	664.5
681	S506	13570	539.5
682	S505	13550	664.5
683	S504	13530	539.5
684	S503	13510	664.5
685	S502	13490	539.5
686	S501	13470	664.5
687	S500	13450	539.5
688	S499	13430	664.5
689	S498	13410	539.5
690	S497	13390	664.5
691	S496	13370	539.5
692	S495	13350	664.5
693	S494	13330	539.5
694	S493	13310	664.5
695	S492	13290	539.5
696	S491	13270	664.5
697	S490	13250	539.5
698	S489	13230	664.5
699	S488	13210	539.5
700	S487	13190	664.5
701	S486	13170	539.5
702	S485	13150	664.5
703	S484	13130	539.5
704	S483	13110	664.5
705	S482	13090	539.5
706	S481	13070	664.5
707	S480	13050	539.5
708	S479	13030	664.5
709	S478	13010	539.5

NO.	PAD Name	X	Y
710	S477	12990	664.5
711	S476	12970	539.5
712	S475	12950	664.5
713	S474	12930	539.5
714	S473	12910	664.5
715	S472	12890	539.5
716	S471	12870	664.5
717	S470	12850	539.5
718	S469	12830	664.5
719	S468	12810	539.5
720	S467	12790	664.5
721	S466	12770	539.5
722	S465	12750	664.5
723	S464	12730	539.5
724	S463	12710	664.5
725	S462	12690	539.5
726	S461	12670	664.5
727	S460	12650	539.5
728	S459	12630	664.5
729	S458	12610	539.5
730	S457	12590	664.5
731	S456	12570	539.5
732	S455	12550	664.5
733	S454	12530	539.5
734	S453	12510	664.5
735	S452	12490	539.5
736	S451	12470	664.5
737	S450	12450	539.5
738	S449	12430	664.5
739	S448	12410	539.5
740	S447	12390	664.5
741	S446	12370	539.5
742	S445	12350	664.5
743	S444	12330	539.5
744	S443	12310	664.5
745	S442	12290	539.5
746	S441	12270	664.5
747	S440	12250	539.5
748	S439	12230	664.5
749	S438	12210	539.5
750	S437	12190	664.5
751	S436	12170	539.5
752	S435	12150	664.5
753	S434	12130	539.5
754	S433	12110	664.5
755	S432	12090	539.5
756	S431	12070	664.5
757	S430	12050	539.5
758	S429	12030	664.5
759	S428	12010	539.5
760	S427	11990	664.5
761	S426	11970	539.5
762	S425	11950	664.5
763	S424	11930	539.5
764	S423	11910	664.5

NO.	PAD Name	X	Y
765	S422	11890	539.5
766	S421	11870	664.5
767	S420	11850	539.5
768	S419	11830	664.5
769	S418	11810	539.5
770	S417	11790	664.5
771	S416	11770	539.5
772	S415	11750	664.5
773	S414	11730	539.5
774	S413	11710	664.5
775	S412	11690	539.5
776	S411	11670	664.5
777	S410	11650	539.5
778	S409	11630	664.5
779	S408	11610	539.5
780	S407	11590	664.5
781	S406	11570	539.5
782	S405	11550	664.5
783	S404	11530	539.5
784	S403	11510	664.5
785	S402	11490	539.5
786	S401	11470	664.5
787	S400	11450	539.5
788	S399	11430	664.5
789	S398	11410	539.5
790	S397	11390	664.5
791	S396	11370	539.5
792	S395	11350	664.5
793	S394	11330	539.5
794	S393	11310	664.5
795	S392	11290	539.5
796	S391	11270	664.5
797	S390	11250	539.5
798	S389	11230	664.5
799	S388	11210	539.5
800	S387	11190	664.5
801	S386	11170	539.5
802	S385	11150	664.5
803	S384	11130	539.5
804	S383	11110	664.5
805	S382	11090	539.5
806	S381	11070	664.5
807	S380	11050	539.5
808	S379	11030	664.5
809	S378	11010	539.5
810	S377	10990	664.5
811	S376	10970	539.5
812	S375	10950	664.5
813	S374	10930	539.5
814	S373	10910	664.5
815	S372	10890	539.5
816	S371	10870	664.5
817	S370	10850	539.5
818	S369	10830	664.5
819	S368	10810	539.5

NO.	PAD Name	X	Y
820	S367	10790	664.5
821	S366	10770	539.5
822	S365	10750	664.5
823	S364	10730	539.5
824	S363	10710	664.5
825	S362	10690	539.5
826	S361	10670	664.5
827	S360	10650	539.5
828	S359	10630	664.5
829	S358	10610	539.5
830	S357	10590	664.5
831	S356	10570	539.5
832	S355	10550	664.5
833	S354	10530	539.5
834	S353	10510	664.5
835	S352	10490	539.5
836	S351	10470	664.5
837	S350	10450	539.5
838	S349	10430	664.5
839	S348	10410	539.5
840	S347	10390	664.5
841	S346	10370	539.5
842	S345	10350	664.5
843	S344	10330	539.5
844	S343	10310	664.5
845	S342	10290	539.5
846	S341	10270	664.5
847	S340	10250	539.5
848	S339	10230	664.5
849	S338	10210	539.5
850	S337	10190	664.5
851	S336	10170	539.5
852	S335	10150	664.5
853	S334	10130	539.5
854	S333	10110	664.5
855	S332	10090	539.5
856	S331	10070	664.5
857	S330	10050	539.5
858	S329	10030	664.5
859	S328	10010	539.5
860	S327	9990	664.5
861	S326	9970	539.5
862	S325	9950	664.5
863	S324	9930	539.5
864	S323	9910	664.5
865	S322	9890	539.5
866	S321	9870	664.5
867	S320	9850	539.5
868	S319	9830	664.5
869	S318	9810	539.5
870	S317	9790	664.5
871	S316	9770	539.5
872	S315	9750	664.5
873	S314	9730	539.5
874	S313	9710	664.5

NO.	PAD Name	X	Y
875	S312	9690	539.5
876	S311	9670	664.5
877	S310	9650	539.5
878	S309	9630	664.5
879	S308	9610	539.5
880	S307	9590	664.5
881	S306	9570	539.5
882	S305	9550	664.5
883	S304	9530	539.5
884	S303	9510	664.5
885	S302	9490	539.5
886	S301	9470	664.5
887	S300	9450	539.5
888	S299	9430	664.5
889	S298	9410	539.5
890	S297	9390	664.5
891	S296	9370	539.5
892	S295	9350	664.5
893	S294	9330	539.5
894	S293	9310	664.5
895	S292	9290	539.5
896	S291	9270	664.5
897	S290	9250	539.5
898	S289	9230	664.5
899	S288	9210	539.5
900	S287	9190	664.5
901	S286	9170	539.5
902	S285	9150	664.5
903	S284	9130	539.5
904	S283	9110	664.5
905	S282	9090	539.5
906	S281	9070	664.5
907	S280	9050	539.5
908	S279	9030	664.5
909	S278	9010	539.5
910	S277	8990	664.5
911	S276	8970	539.5
912	S275	8950	664.5
913	S274	8930	539.5
914	S273	8910	664.5
915	S272	8890	539.5
916	S271	8870	664.5
917	S270	8850	539.5
918	S269	8830	664.5
919	S268	8810	539.5
920	S267	8790	664.5
921	S266	8770	539.5
922	S265	8750	664.5
923	S264	8730	539.5
924	S263	8710	664.5
925	S262	8690	539.5
926	S261	8670	664.5
927	S260	8650	539.5
928	S259	8630	664.5
929	S258	8610	539.5

NO.	PAD Name	X	Y
930	S257	8590	664.5
931	S256	8570	539.5
932	S255	8550	664.5
933	S254	8530	539.5
934	S253	8510	664.5
935	S252	8490	539.5
936	S251	8470	664.5
937	S250	8450	539.5
938	S249	8430	664.5
939	S248	8410	539.5
940	S247	8390	664.5
941	S246	8370	539.5
942	S245	8350	664.5
943	S244	8330	539.5
944	S243	8310	664.5
945	S242	8290	539.5
946	S241	8270	664.5
947	S240	8250	539.5
948	S239	8230	664.5
949	S238	8210	539.5
950	S237	8190	664.5
951	S236	8170	539.5
952	S235	8150	664.5
953	S234	8130	539.5
954	S233	8110	664.5
955	S232	8090	539.5
956	S231	8070	664.5
957	S230	8050	539.5
958	S229	8030	664.5
959	S228	8010	539.5
960	S227	7990	664.5
961	S226	7970	539.5
962	S225	7950	664.5
963	S224	7930	539.5
964	S223	7910	664.5
965	S222	7890	539.5
966	S221	7870	664.5
967	S220	7850	539.5
968	S219	7830	664.5
969	S218	7810	539.5
970	S217	7790	664.5
971	S216	7770	539.5
972	S215	7750	664.5
973	S214	7730	539.5
974	S213	7710	664.5
975	S212	7690	539.5
976	S211	7670	664.5
977	S210	7650	539.5
978	S209	7630	664.5
979	S208	7610	539.5
980	S207	7590	664.5
981	S206	7570	539.5
982	S205	7550	664.5
983	S204	7530	539.5
984	S203	7510	664.5

NO.	PAD Name	X	Y
985	S202	7490	539.5
986	S201	7470	664.5
987	S200	7450	539.5
988	S199	7430	664.5
989	S198	7410	539.5
990	S197	7390	664.5
991	S196	7370	539.5
992	S195	7350	664.5
993	S194	7330	539.5
994	S193	7310	664.5
995	S192	7290	539.5
996	S191	7270	664.5
997	S190	7250	539.5
998	S189	7230	664.5
999	S188	7210	539.5
1000	S187	7190	664.5
1001	S186	7170	539.5
1002	S185	7150	664.5
1003	S184	7130	539.5
1004	S183	7110	664.5
1005	S182	7090	539.5
1006	S181	7070	664.5
1007	S180	7050	539.5
1008	S179	7030	664.5
1009	S178	7010	539.5
1010	S177	6990	664.5
1011	S176	6970	539.5
1012	S175	6950	664.5
1013	S174	6930	539.5
1014	S173	6910	664.5
1015	S172	6890	539.5
1016	S171	6870	664.5
1017	S170	6850	539.5
1018	S169	6830	664.5
1019	S168	6810	539.5
1020	S167	6790	664.5
1021	S166	6770	539.5
1022	S165	6750	664.5
1023	S164	6730	539.5
1024	S163	6710	664.5
1025	S162	6690	539.5
1026	S161	6670	664.5
1027	S160	6650	539.5
1028	S159	6630	664.5
1029	S158	6610	539.5
1030	S157	6590	664.5
1031	S156	6570	539.5
1032	S155	6550	664.5
1033	S154	6530	539.5
1034	S153	6510	664.5
1035	S152	6490	539.5
1036	S151	6470	664.5
1037	S150	6450	539.5
1038	S149	6430	664.5
1039	S148	6410	539.5

NO.	PAD Name	X	Y
1040	S147	6390	664.5
1041	S146	6370	539.5
1042	S145	6350	664.5
1043	S144	6330	539.5
1044	S143	6310	664.5
1045	S142	6290	539.5
1046	S141	6270	664.5
1047	S140	6250	539.5
1048	S139	6230	664.5
1049	S138	6210	539.5
1050	S137	6190	664.5
1051	S136	6170	539.5
1052	S135	6150	664.5
1053	S134	6130	539.5
1054	S133	6110	664.5
1055	S132	6090	539.5
1056	S131	6070	664.5
1057	S130	6050	539.5
1058	S129	6030	664.5
1059	S128	6010	539.5
1060	S127	5990	664.5
1061	S126	5970	539.5
1062	S125	5950	664.5
1063	S124	5930	539.5
1064	S123	5910	664.5
1065	S122	5890	539.5
1066	S121	5870	664.5
1067	S120	5850	539.5
1068	S119	5830	664.5
1069	S118	5810	539.5
1070	S117	5790	664.5
1071	S116	5770	539.5
1072	S115	5750	664.5
1073	S114	5730	539.5
1074	S113	5710	664.5
1075	S112	5690	539.5
1076	S111	5670	664.5
1077	S110	5650	539.5
1078	S109	5630	664.5
1079	S108	5610	539.5
1080	S107	5590	664.5
1081	S106	5570	539.5
1082	S105	5550	664.5
1083	S104	5530	539.5
1084	S103	5510	664.5
1085	S102	5490	539.5
1086	S101	5470	664.5
1087	S100	5450	539.5
1088	S99	5430	664.5
1089	S98	5410	539.5
1090	S97	5390	664.5
1091	S96	5370	539.5
1092	S95	5350	664.5
1093	S94	5330	539.5
1094	S93	5310	664.5

NO.	PAD Name	X	Y
1095	S92	5290	539.5
1096	S91	5270	664.5
1097	S90	5250	539.5
1098	S89	5230	664.5
1099	S88	5210	539.5
1100	S87	5190	664.5
1101	S86	5170	539.5
1102	S85	5150	664.5
1103	S84	5130	539.5
1104	S83	5110	664.5
1105	S82	5090	539.5
1106	S81	5070	664.5
1107	S80	5050	539.5
1108	S79	5030	664.5
1109	S78	5010	539.5
1110	S77	4990	664.5
1111	S76	4970	539.5
1112	S75	4950	664.5
1113	S74	4930	539.5
1114	S73	4910	664.5
1115	S72	4890	539.5
1116	S71	4870	664.5
1117	S70	4850	539.5
1118	S69	4830	664.5
1119	S68	4810	539.5
1120	S67	4790	664.5
1121	S66	4770	539.5
1122	S65	4750	664.5
1123	S64	4730	539.5
1124	S63	4710	664.5
1125	S62	4690	539.5
1126	S61	4670	664.5
1127	S60	4650	539.5
1128	S59	4630	664.5
1129	S58	4610	539.5
1130	S57	4590	664.5
1131	S56	4570	539.5
1132	S55	4550	664.5
1133	S54	4530	539.5
1134	S53	4510	664.5
1135	S52	4490	539.5
1136	S51	4470	664.5
1137	S50	4450	539.5
1138	S49	4430	664.5
1139	S48	4410	539.5
1140	S47	4390	664.5
1141	S46	4370	539.5
1142	S45	4350	664.5
1143	S44	4330	539.5
1144	S43	4310	664.5
1145	S42	4290	539.5
1146	S41	4270	664.5
1147	S40	4250	539.5
1148	S39	4230	664.5
1149	S38	4210	539.5

NO.	PAD Name	X	Y
1150	S37	4190	664.5
1151	S36	4170	539.5
1152	S35	4150	664.5
1153	S34	4130	539.5
1154	S33	4110	664.5
1155	S32	4090	539.5
1156	S31	4070	664.5
1157	S30	4050	539.5
1158	S29	4030	664.5
1159	S28	4010	539.5
1160	S27	3990	664.5
1161	S26	3970	539.5
1162	S25	3950	664.5
1163	S24	3930	539.5
1164	S23	3910	664.5
1165	S22	3890	539.5
1166	S21	3870	664.5
1167	S20	3850	539.5
1168	S19	3830	664.5
1169	S18	3810	539.5
1170	S17	3790	664.5
1171	S16	3770	539.5
1172	S15	3750	664.5
1173	S14	3730	539.5
1174	S13	3710	664.5
1175	S12	3690	539.5
1176	S11	3670	664.5
1177	S10	3650	539.5
1178	S9	3630	664.5
1179	S8	3610	539.5
1180	S7	3590	664.5
1181	S6	3570	539.5
1182	S5	3550	664.5
1183	S4	3530	539.5
1184	S3	3510	664.5
1185	S2	3490	539.5
1186	S1	3470	664.5
1187	TESTO35	3450	539.5
1188	TESTO36	3390	664.5
1189	VGLDMY3	3370	539.5
1190	G320	3350	664.5
1191	G318	3330	539.5
1192	G316	3310	664.5
1193	G314	3290	539.5
1194	G312	3270	664.5
1195	G310	3250	539.5
1196	G308	3230	664.5
1197	G306	3210	539.5
1198	G304	3190	664.5
1199	G302	3170	539.5
1200	G300	3150	664.5
1201	G298	3130	539.5
1202	G296	3110	664.5
1203	G294	3090	539.5
1204	G292	3070	664.5

NO.	PAD Name	X	Y
1205	G290	3050	539.5
1206	G288	3030	664.5
1207	G286	3010	539.5
1208	G284	2990	664.5
1209	G282	2970	539.5
1210	G280	2950	664.5
1211	G278	2930	539.5
1212	G276	2910	664.5
1213	G274	2890	539.5
1214	G272	2870	664.5
1215	G270	2850	539.5
1216	G268	2830	664.5
1217	G266	2810	539.5
1218	G264	2790	664.5
1219	G262	2770	539.5
1220	G260	2750	664.5
1221	G258	2730	539.5
1222	G256	2710	664.5
1223	G254	2690	539.5
1224	G252	2670	664.5
1225	G250	2650	539.5
1226	G248	2630	664.5
1227	G246	2610	539.5
1228	G244	2590	664.5
1229	G242	2570	539.5
1230	G240	2550	664.5
1231	G238	2530	539.5
1232	G236	2510	664.5
1233	G234	2490	539.5
1234	G232	2470	664.5
1235	G230	2450	539.5
1236	G228	2430	664.5
1237	G226	2410	539.5
1238	G224	2390	664.5
1239	G222	2370	539.5
1240	G220	2350	664.5
1241	G218	2330	539.5
1242	G216	2310	664.5
1243	G214	2290	539.5
1244	G212	2270	664.5
1245	G210	2250	539.5
1246	G208	2230	664.5
1247	G206	2210	539.5
1248	G204	2190	664.5
1249	G202	2170	539.5
1250	G200	2150	664.5
1251	G198	2130	539.5
1252	G196	2110	664.5
1253	G194	2090	539.5
1254	G192	2070	664.5
1255	G190	2050	539.5
1256	G188	2030	664.5
1257	G186	2010	539.5
1258	G184	1990	664.5
1259	G182	1970	539.5

NO.	PAD Name	X	Y
1260	G180	1950	664.5
1261	G178	1930	539.5
1262	G176	1910	664.5
1263	G174	1890	539.5
1264	G172	1870	664.5
1265	G170	1850	539.5
1266	G168	1830	664.5
1267	G166	1810	539.5
1268	G164	1790	664.5
1269	G162	1770	539.5
1270	G160	1750	664.5
1271	G158	1730	539.5
1272	G156	1710	664.5
1273	G154	1690	539.5
1274	G152	1670	664.5
1275	G150	1650	539.5
1276	G148	1630	664.5
1277	G146	1610	539.5
1278	G144	1590	664.5
1279	G142	1570	539.5
1280	G140	1550	664.5
1281	G138	1530	539.5
1282	G136	1510	664.5
1283	G134	1490	539.5
1284	G132	1470	664.5
1285	G130	1450	539.5
1286	G128	1430	664.5
1287	G126	1410	539.5
1288	G124	1390	664.5
1289	G122	1370	539.5
1290	G120	1350	664.5
1291	G118	1330	539.5
1292	G116	1310	664.5
1293	G114	1290	539.5
1294	G112	1270	664.5
1295	G110	1250	539.5
1296	G108	1230	664.5
1297	G106	1210	539.5
1298	G104	1190	664.5
1299	G102	1170	539.5
1300	G100	1150	664.5
1301	G98	1130	539.5
1302	G96	1110	664.5
1303	G94	1090	539.5
1304	G92	1070	664.5
1305	G90	1050	539.5
1306	G88	1030	664.5
1307	G86	1010	539.5
1308	G84	990	664.5
1309	G82	970	539.5
1310	G80	950	664.5
1311	G78	930	539.5
1312	G76	910	664.5
1313	G74	890	539.5
1314	G72	870	664.5

NO.	PAD Name	X	Y
1315	G70	850	539.5
1316	G68	830	664.5
1317	G66	810	539.5
1318	G64	790	664.5
1319	G62	770	539.5
1320	G60	750	664.5
1321	G58	730	539.5
1322	G56	710	664.5
1323	G54	690	539.5
1324	G52	670	664.5
1325	G50	650	539.5
1326	G48	630	664.5
1327	G46	610	539.5
1328	G44	590	664.5

NO.	PAD Name	X	Y
1329	G42	570	539.5
1330	G40	550	664.5
1331	G38	530	539.5
1332	G36	510	664.5
1333	G34	490	539.5
1334	G32	470	664.5
1335	G30	450	539.5
1336	G28	430	664.5
1337	G26	410	539.5
1338	G24	390	664.5
1339	G22	370	539.5
1340	G20	350	664.5
1341	G18	330	539.5
1342	G16	310	664.5

NO.	PAD Name	X	Y
1343	G14	290	539.5
1344	G12	270	664.5
1345	G10	250	539.5
1346	G8	230	664.5
1347	G6	210	539.5
1348	G4	190	664.5
1349	G2	170	539.5
1350	VGLDMY4	150	664.5
1351	DUMMYR9	130	539.5
1352	DUMMYR10	110	664.5
1353	TESTO37	90	539.5
1354	TESTO38	70	664.5

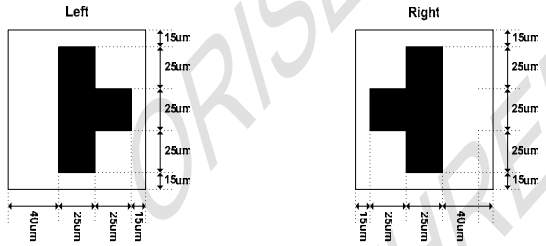
14.5. Alignment Mark

--Alignment Mark coordinate

Left (107, 230)

Right (21373, 230)

--Alignment Mark size



15. DISCLAIMER

The information appearing in this publication is believed to be accurate.

Integrated circuits sold by ORISE Technology are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only. ORISE Technology makes no warranty, express, statutory implied or by description regarding the information in this publication or regarding the freedom of the described chip(s) from patent infringement. FURTHERMORE, ORISE Technology MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. ORISE Technology reserves the right to halt production or alter the specifications and prices at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders. Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by ORISE Technology for such applications. Please note that application circuits illustrated in this document are for reference purposes only.

16. REVISION HISTORY

Date	Revision #	Description	Page
MAR. 06, 2007	0.3	Modify “15.4. PAD Locations”	67-75
FEB. 16, 2007	0.2	Modify “15.4. PAD Locations”	67-75
DEC. 20, 2006	0.1	Original	77