DATA SHEET

旭曜科技
ORISE TECH

SPFD5420A

720-channel 6-bit Source Driver with System-on-chip for Color Amorphous TFT-LCDs

Preliminary

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Version 0.7

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720-CHANNEL DRIVER WITH SYSTEM-ON-CHIP (SOC) FOR COLOR AMORPHOUS TFT LCD

1. GENERAL DESCRIPTION

The SPFD5420A, a 262144-color System-on-Chip (SoC) driver LSI designed for small and medium sizes of TFT LCD display, is capable of supporting up to 240xRGBx432 in resolution which can be achieved by the designated RAM for graphic data. The 720-channel source driver has true 6-bit resolution, which generates 64 Gamma-corrected values by an internal D/A converter.

The SPFD5420A is able to operate with low IO interface power supply up to 1.65V and incorporate with several charge pumps to generate various voltage levels that form an on-chip power management system for gate driver and source driver.

The built-in timing controller in SPFD5420A can support several interfaces for the diverse request of medium or small size portable display. SPFD5420A provides system interfaces, which include 8-/9-/16-/18-bit parallel interfaces and serial interface (SPI), to configure system. Not only can the system interfaces be used to configure system, they can also access RAM at high speed for still picture display. In addition, the SPFD5420A incorporates 6, 16, and 18-bit RGB interfaces for picture movement display. The SPFD5420A also supports eight-color mode and standby mode for power saving consideration.

2. FEATURES

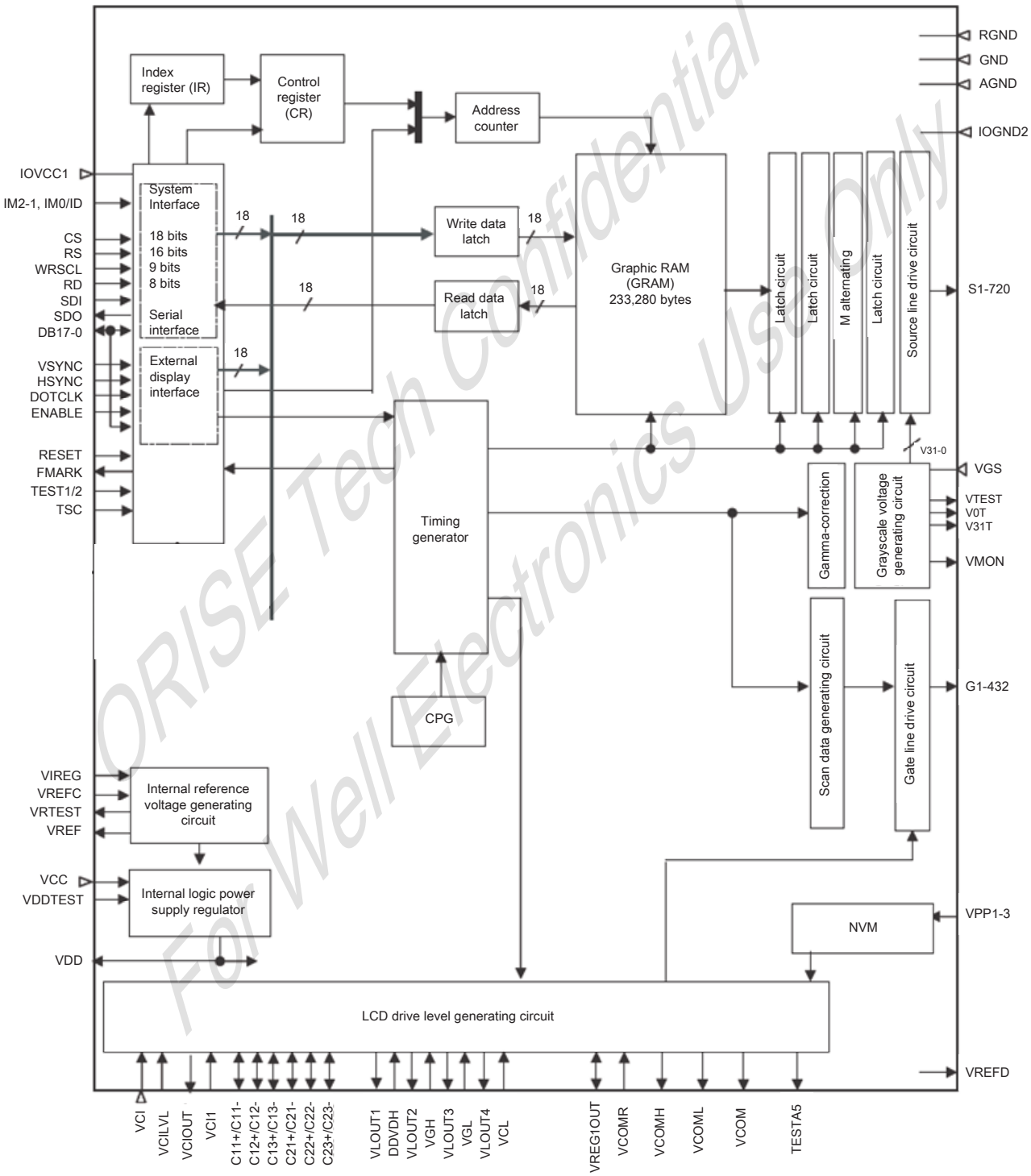
- One-chip solution for amorphous TFT-LCD.
- Supports resolution up to 240xRGBx432, incorporating a 720-channel source driver and a 432-channel gate driver
- Outputs 64 γ -corrected values using an internal true 6-bit resolution D/A converter to achieve 262K colors
- Built-in 233,280 bytes internal RAM
- Line Inversion AC drive / frame inversion AC drive
- System interfaces
  - High-speed interfaces to 8-, 9-, 16-, and 18-bit parallel ports
  - Serial Peripheral Interface (SPI)
- Interfaces for moving picture display
  - 6-, 16-, and 18-bit RGB interfaces
- Varies RAM accessing for functional display
  - Window address function to display at any area on the screen via a moving picture display interface
  - Window address function to limit the data rewriting area and reduce data transfer
  - Moving and still picture can display at the same time
  - Vertical scrolling function
  - Partial screen display
- Power supply
  - Logic power supply voltage (Vcc): 2.5 ~ 3.6 V
  - I/O interface supply voltage (IOVcc): 1.65 ~3.6 V
  - Analog power supply voltage (Vci): 2.5 ~ 3.6 V
- On-chip power management system
  - Power saving mode (standby / 8-color mode, etc)
  - Low power consumption structure for source driver.
- Built-in Charge Pump circuits
  - Source driver voltage level: DDVDH-GND=4.5V ~ 6V.
  - Gate driver voltage level (VGH, VGL)
    VGH = 10.0V ~15.0V
    VGL = -4.5V ~ -12.5V
    VGH – VGL $\leqq$ 28.0V
  - Built-in internal oscillator and hardware reset
- Built–in One-Time-Programmable (OTP) function for VCOM amplitude and VcomH voltage adjustment. User identification code,4 bits, VCOM level adjustment, 5 bits x 2 sets

3. ORDERING INFORMATION

Product Number	Package Type
SPFD5420A-C1	Chip Form with Gold Bump

4. BLOCK DIAGRAM

4.1. Block Function



4.2. System Interface

4.2.1. The SPFD5420A supports three high-speed system interfaces:

1. 80-system high-speed interfaces with 8-, 9-, 16-, 18-bit parallel ports.
2. Serial Peripheral Interface (SPI).

The SPFD5420A has a 16-bit index register (IR) and two 18-bit data registers, a write-data register (WDR) and a read-data register (RDR). The IR register is used to store index information from control registers. The WDR register is used to temporarily store data to be written for register control and internal GRAM. The RDR register is used to temporarily store data read from the GRAM. When graphic data is written to the internal GRAM from MCU/graphic engine, the data is first written to the WDR and then automatically written to the internal GRAM in internal operation. When graphic data read operation is executed, graphic data is read via the RDR from the internal GRAM. Therefore, invalid data is first read out to the data bus when the SPFD5420A executes the 1st read operation. Thus, valid data can be read out after the SPFD5420A executes the 1st read operation.

4.2.2. External Display Interface

The SPFD5420A supports external RGB interface for picture movement display.
The SPFD5420A allows switching between one of the external display interfaces and the system interface via pin configuration so that the optimum interface is selected for still / moving picture displayed on the screen.

When the RGB interface is chosen, display operations are synchronized with external supplied signals, VSYNC, HSYNC, and DOTCLK. Moreover, valid display data (DB17-0) is written to GRAM, which synchronized with signal (DE) enabling.

4.2.3. Address Counter (AC)

SPFD5420A features an Address Counter (AC) giving an address to the internal GRAM. The address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

4.2.4. Graphics RAM (GRAM)

SPFD5420A features a 233,280-byte (240RGB x 432 x 18 / 8) Graphic RAM (GRAM).

4.2.5. Grayscale Voltage Generating Circuit

SPFD5420A has true 6-bit resolution D/A converter, which generates 64 Gamma-corrected values and cooperates with OP-AMP structure to enhance display quality. The grayscale voltage can be adjusted by grayscale data set in the γ-correction register.

4.2.6. Timing Controller

SPFD5420A has a timing controller, which can generate a timing signal for internal circuit operation such as gate output timing, RAM accessing timing, etc.

4.2.7. Oscillator (OSC)

The SPFD5420A also features an internal oscillator to generate RC oscillation with an internal resistor. In standby mode, RC oscillation is halted to reduce power consumption.

4.2.8. Source Driver Circuit

SPFD5420A consists of a 720-output source driver circuit (S1 ~ S720). Data in the GRAM are latched when the 720th bit data is input. The latched data controls the source driver and generates a drive waveform.

4.2.9. Gate Driver Circuit

SPFD5420A consists of a 432-output gate driver circuit (G1~G432). The gate driver circuit outputs gate driver signals at either VGH or VGL level.

4.2.10. LCD Driving Power Supply Circuit

The LCD driving power supply circuit generates the voltage levels DDVDH, VLOUT2, VLOUT3 and VCOM for driving an LCD. All this voltages can be adjusted by register setting.

5. SIGNAL DESCRIPTIONS

<table>
<tr><th>Signal</th><th>No. of pins</th><th>I/O</th><th>Connected with</th><th>Function</th></tr>
<tr><td colspan="5">System Configuration Input Signal</td></tr>
<tr><td>IM2~1, IM0/ID</td><td>3</td><td>I</td><td>GND/ IOVCC</td><td>Select a mode to interface to an MPU. In serial interface operation, the IM0 pin is used to set the ID bit of device code.
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0/ I D</th><th>Interface Mode</th><th>DB Pin</th><th>Colors</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>80-system 18-bit interface</td><td>DB17-0</td><td>262,144</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>80-system 9-bit interface</td><td>DB17-9</td><td>262,144</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>80-system 16-bit interface</td><td>DB17-10, DB8-1</td><td>262,144 see Note 1</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>80-system 8-bit interface</td><td>DB17-10</td><td>262,144 see Note 2</td></tr>
<tr><td>1</td><td>0</td><td>*(ID)</td><td>Clock synchronous serial interface</td><td>-</td><td>65,536</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
</table>
Notes: 1. 65,536 colors in one transfer mode
2. 65,536 colors in two transfers mode</td></tr>
<tr><td>/RESET</td><td>1</td><td>I</td><td>MPU or external RC circuit</td><td>RESET pin. This is an active low signal.</td></tr>
<tr><td colspan="5">Interface input Signals</td></tr>
<tr><td>/CS</td><td>1</td><td>I</td><td>MPU</td><td>Chip select signal.
Low: the SPFD5420A is accessible
High: the SPFD5420A is not accessible
Must be connected to the GND or IOVCC level when not used.</td></tr>
<tr><td>RS</td><td>1</td><td>I</td><td>MPU</td><td>Register select signal.
Low: Index register or internal status is selected.
High: Control register is selected.
Must be connected to the GND or IOVCC level when not used.</td></tr>
<tr><td>(/WR) / (SCL)</td><td>1</td><td>I</td><td>MPU</td><td>(A) In 80-system interface mode, a write strobe signal can be input via this pin and initializes a write operation when the signal is low.
(B) In SPI mode, served as a synchronizing clock signal.</td></tr>
<tr><td>/RD</td><td>1</td><td>I</td><td>MPU</td><td>In 80-system interface mode, a read strobe signal can be input via this pin and initializes a read operation when the signal is low.
Must be connected to the GND or IOVCC level when not in use.</td></tr>
<tr><td>SDI</td><td>1</td><td>I</td><td>MPU</td><td>Serial Data is inputted on the rising edge of the SCL signal in SPI mode.
Must be connected to the GND or IOVCC level when not in use</td></tr>
<tr><td>SDO</td><td>1</td><td>O</td><td>MPU</td><td>Serial Data is outputted on the rising edge of the SCL signal in SPI mode.</td></tr>
<tr><td>DB0-DB17</td><td>1</td><td>I/O</td><td>MPU</td><td>Served as an 18-bit parallel bi-directional data bus. Data bus pin assignment corresponding to different modes are summarized in the table:
<table>
<tr><th>Mode</th><th>Pin Assignment</th></tr>
<tr><td>8-bit system interface</td><td>DB17-DB10</td></tr>
<tr><td>9-bit system interface</td><td>DB17-DB9</td></tr>
<tr><td>16-bit system interface</td><td>DB17-DB10, DB8-DB1</td></tr>
<tr><td>18-bit system interface</td><td>DB17-DB0</td></tr>
</table></td></tr>
</table>

Signal	No. of pins	I/O	Connected with	Function
				6-bit External (RGB) interface: DB17-DB12 16-bit External (RGB) interface: DB17-13, DB11-DB1 18-bit External (RGB) interface: DB17-DB0 Must be connected to the GND or IOVCC level when not in use.
VSYNC	1	I	MPU	In external interface mode, served as a vertical synchronize signal input Must be connected to the IOVCC or GND level when not in use.
HSYNC	1	I	MPU	In external interface mode, served as a horizontal synchronized signal input Must be connected to the IOVCC or GND level when not used.
ENABLE	1	I	MPU	In external interface mode, polarity of ENABLE signal is synchronized with valid graphic data input. Low: Valid data on DB17-DB0 High: Invalid data on DB17-DB0 Moreover, setting EPL bit can change the polarity of the ENABLE signal. Must be connected to the GND or IOVCC level when not in use.
DOTCLK	1	I	MPU	In external interface mode, served as a dot clock signal. When DPL = "0": Input data on the rising edge of DOTCLK When DPL = "1": Input data on the falling edge of DOTCLK It is fixed to the IOVCC level when not in use.
FMARK	1	O	MPU	Frame head pulse signal, which is used when writing data to the internal RAM. Keep this pin open when not used.
Charge Pump and Power Supply Signal				
C11P/N, C12P/N C13P/N C21P/N, C22P/N C23P/N	12	I/O	Step-up capacitor	Connect boost capacitors for the internal DC/DC converter circuit to these pins. Leave the pins open when DC/DC converter circuits are not used.
VCIOUT	1	O	Stabilizing capacitor, VCI1	Output voltage from the step-up circuit 1, generated from the reference voltage. VC bits set the output factor. Make sure to connect to stabilizing capacitor.
VCI1	1	I/O	VCIOUT	Reference voltage of step-up circuit 1. Make sure the output voltage levels from VLOUT1, VLOUT2, and VLOUT3 do not exceed the respective setting ranges.
VLOUT1	1	O	Stabilizing capacitor, DDVDH	Output voltage from the step-up circuit 1, generated from VCI1. The step-up factor is set by BT. Make sure to connect to stabilizing capacitor. VLOUT1 = 4.5V ~ 6.0V
DDVDH	1	I	VLOUT1	Power supply for the source driver liquid crystal drive unit and VCOM drive. Connect to VLOUT1. DDVDH = 4.5V ~ 6.0V
VLOUT2	1	O	Stabilizing capacitor, VGH	Output voltage from the step-up circuit 2, generated from VCI1 and DDVDH. The step-up factor is set by BT. Make sure to connect to stabilizing capacitor. VLOUT2 = max 15.0V
VGH	1	I	VLOUT2	Liquid crystal drive power supply. Connect to VLOUT2.
VLOUT3	1	O	Stabilizing capacitor, VGL	Output voltage from the step-up circuit 2, generated from VCI1 and DDVDH. The step-up factor is set by BT bits. Make sure to connect to stabilizing capacitor. VLOUT3 = min –12.5V

Signal	No. of pins	I/O	Connected with	Function
VGL	1	I	VLOUT3	Liquid crystal drive power supply. Connect to VLOUT3.
VLOUT4	1	O	Stabilizing capacitor, VCL	Output voltage from the step-up circuit 2, generated from VCI1 and DDVDH. The step-up factor is set by BT bits. Make sure to connect to stabilizing capacitor. VLOUT = -1.9V – 3.0V.
VCL	1	O	Stabilizing capacitor	VCOML drive power supply. Make sure to connect to stabilizing capacitor. VCL = -1.9V ~ -3.0V
VCILVL		I	Reference power supply	VCILVL must be at the same electrical potential as VCI. VCILVL = 2.5V ~ 3.6V. Connect to external power supply. In case of COG, connect to VCI on the FPC to prevent noise.
VPP1	1	I	Power supply or open	OTP power supply.
VPP2	1	I	Power supply or open	
VPP3A, 3B	2	I	Power supply or open	

Operation mode	VPP1	VPP2	VPP3
NVM Write	GND	8.25V	GND
NVM read	GND/Open	Open	GND/Open

Source/Gate Driver and VCOM Signals				
G1~G432	432	O	LCD	Output gate driver signals, which has the swing from VGH to VGL
S1~S720	720	O	LCD	Output source driver signals. The D/A converted 64-gray-scale analog voltages are outputted.
VREG1 OUT	1	O	Stabilizing capacitor	Output voltage generated from the reference voltage (VCILVL or VCIR). The factor is determined by instruction (VRH bits). VREG1OUT is used for (1) source driver grayscale reference voltage, (2) VCOMH level reference voltage, and (3) VCOM amplitude reference voltage. Connect to a stabilizing capacitor when in use. VREG1OUT = 4.0V ~ (DDVDH – 0.5)V
VCOM	1	O	TFT panel common electrode	Power supply to TFT panel's common electrode. VCOM alternates between VCOMH and VCOML. The alternating cycle is set by internal register. Also, the VCOM output can be started and halted by register setting.
VCOMH	1	O	Stabilizing capacitor	The High level of VCOM amplitude. The output level can be adjusted by either external resistor (VCOMR) or electronic volume. Make sure to connect to stabilizing capacitor.
VCOML	1	O	Stabilizing capacitor	The Low level of VCOM amplitude. The output level can be adjusted by instruction (VDV bits). VCOML = (VCL+0.5)V ~ 0V. Make sure to connect to stabilizing capacitor.
VCOMR	1	I	Variable resistor or open	Connect a variable resistor when adjusting the VCOMH level between VREG1OUT and GND.
VGS	1	I	GND	Reference level for the grayscale voltage generating circuit.
VCC	1	-	Power supply	Internal logic power: VCC = 2.5V ~3.6V. VCC > IOVCC.
GND	1	-	Power supply	Internal logic GND: GND = 0V.
RGND	1	-	Power supply	Internal RAM GND. RGND must be at the same electrical potential as GND. In case of COG, connect to GND on the FPC to prevent noise.
VDD	1	O	Stabilizing capacitor	Internal logic regulator output, which is used as the power supply to internal logic. Connect a stabilizing capacitor.
IOVCC	1	-	Power supply	Power supply to the interface pins: RESET*, CS*, WR, RD*, RS, DB17-0, VSYNC, HSYNC, DOTCLK, ENABLE. IOVCC = 1.65V ~ 3.3V. VCC ≥IOVCC. In case of COG, connect to VCC on the FPC if IOVCC=VCC, to prevent noise.

Signal	No. of pins	I/O	Connected with	Function
IOGND	1	-	Power supply	GND for the interface pins: RESET*, CS*, WR, RD*, RS, DB17-0, VSYNC, HSYNC, DOTCLK, ENABLE. IOGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
AGND	1	-	Power supply	Analog GND (for logic regulator and liquid crystal power supply circuit): AGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
VCI	1	I	Power supply	Power supply to the liquid crystal power supply analog circuit. Connect to an external power supply of 2.5V ~ 3.6V.
VCILVL	1	I	Reference power supply	VCILVL must be at the same electrical potential as VCI. VCILVL = 2.5V ~ 3.6V. Connect to external power supply. In case of COG, connect to VCI on the FPC to prevent noise.
Misc. Signal				
V0T, V31T	2	I/O	Open	Test pins. Leave them open. SPFD5420A use these pins to do self-test. No signal on panel can cross these pins, otherwise function fail.
VTEST	1	I/O	Open	Test pins. Leave them open. SPFD5420A use these pins to do self-test. No signal on panel can cross these pins, otherwise function fail.
VREFC	1	I/O	Open	Test pins. Fix to the AGND level.
VREF	1	I/O	Open	Test pins. Leave them open.
VDDTEST	1	I/O	Open	Test pins. Fix to the AGND level.
VREFD	1	I/O	Open	Test pins. Leave them open. SPFD5420A use these pins to do self-test. No signal on panel can cross these pins, otherwise function fail.
VMON	1	I/O	Open	Test pins. Leave them open. SPFD5420A use these pins to do self-test. No signal on panel can cross these pins, otherwise function fail.
TESTA5	1	I/O	Open	Test pins. Leave them open. SPFD5420A use these pins to do self-test. No signal on panel can cross these pins, otherwise function fail.
IOVCCDUM1~2	2	I/O	Open	Test pins. Leave them open.
VCCDUM1	1	I/O	Open	Test pins. Leave them open.
IOGNDDUM1~3	3	I/O	Open	Test pins. Leave them open.
AGNDDUM1~5	5	I/O	Open	Test pins. Fix to VREFC, VDDTEST.
DUMMYR1~10	10	I/O	Open	Test pins. Leave them open. SPFD5420A use these pins to do self-test. No any signal on panel can cross these pins, otherwise function fail.
VGLDMY1~4	4	I/O	Open	Test pins. Leave them open.
TESTO1~18	18	I/O	Open	Test pins. Leave them open.
TEST1~3	3	I	IOGND	Test pins. Connect to IOGND.

6. INSTRUCTIONS

6.1. Outline

The SPFD5420A supports 18-bit data bus interface to access command register to configure system. When the command register accessing is desired, sending the command information to specify which index register would be accessed and following the data to that control register. Moreover, register accessing operation should cooperate with RS, /WR, /RD signal for SPFD5420A to recognize the control instruction. And command instruction can be accomplished by using all system interfaces (18-bit, 16-bit, 9-bit, 8-bit 80 system and SPI). The corresponding pin assignment of different system interface are shown in **Figure 6-1** to **Figure 6-6**

The instruction can be categorized into 8 groups. And the 8 groups are:

1. Specify the index of register
2. Read a status
3. Display control
4. Power management Control
5. Graphics data processing
6. Set internal GRAM address
7. Transfer data to and from the internal GRAM
8. Internal grayscale γ-correction

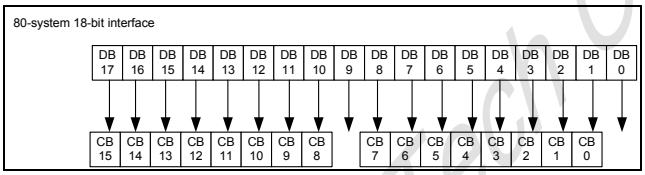


Figure 6-1

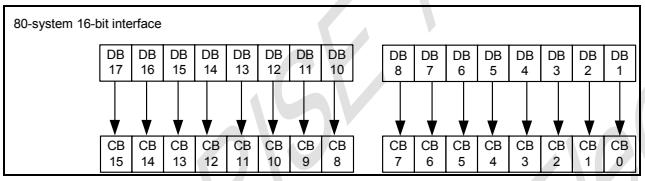


Figure 6-2

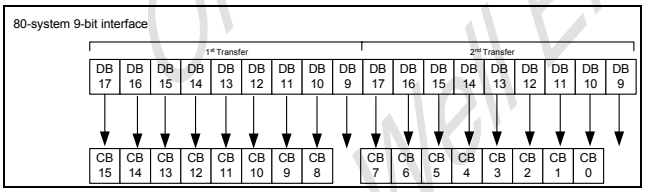


Figure 6-3

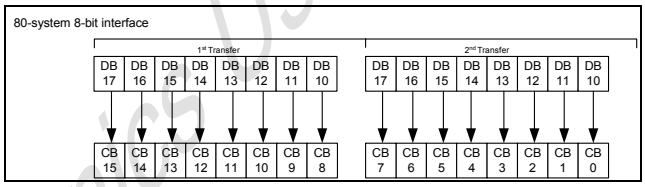


Figure 6-4

Serial interface Data Format

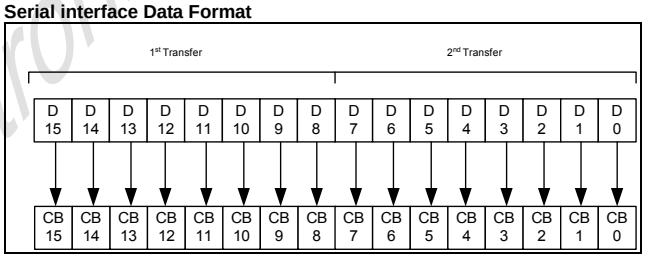


Figure 6-5

Serial interface Data Transfer Format

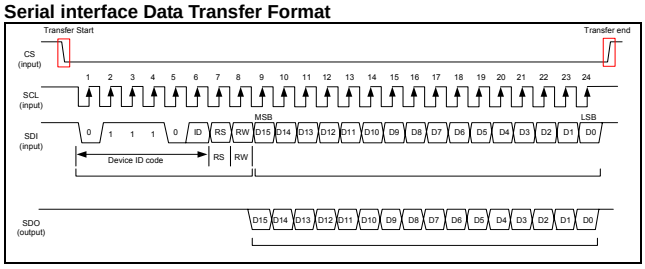


Figure 6-6

6.2. Instruction

Table 6-1 Instruction List Table

Register No	Register	Upper 8-bit								Lower 8-bit							
		CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
000h	ID Read	0	1	0	1	0	1	0	0	0	0	1	0	0	0	0	0
001h	Driver Output Control	0	0	0	0	0	SM (0)	0	SS (0)	0	0	0	0	0	0	0	0
002h	LCD Drive Waveform Control	0	0	0	0	0	0	0	B/C (0)	0	0	0	0	0	0	NW1 (0)	NW0 (0)
003h	Entry Mode	TRIREG (0)	DFM (0)	0	BGR (0)	0	0	HWM (0)	0	ORG (0)	0	I/D1 (1)	I/D0 (1)	AM (0)	0	EPF1 (0)	EPF0 (0)
004h-006h	Setting disabled																
007h	Display Control (1)	0	0	PTDE1 (0)	PTDE0 (0)	0	0	0	BASEE (0)	0	VON (0)	GON (0)	DTE (0)	0	0	D1 (0)	D0 (0)
008h	Display Control (2)	0	0	0	0	FP3 (1)	FP2 (0)	FP1 (0)	FP0 (0)	0	0	0	0	BP3 (1)	BP2 (0)	BP1 (0)	BP0 (0)
009h	Low Power Control (1)	0	0	0	0	PTV (0)	PTS2 (0)	PTS1 (0)	PTS0 (0)	0	0	PTG1 (0)	PTG0 (0)	ISC3 (0)	ISC2 (0)	ISC1 (0)	ISC0 (0)
00Ah	Setting Disabled																
00Bh	Low Power Control (2)	0	0	0	0	0	0	0	0	0	0	0	VEM0 (0)	0	0	0	COL (0)
0Ch	External Display Controll (1)	0	ENC2 (0)	ENC1 (0)	ENC0 (0)	0	0	0	RM (0)	0	0	DM1 (0)	DM0 (0)	0	0	RIM1 (0)	RIM0 (0)
00Dh-00Eh	Setting Disabled																
00Fh	External Display Controll (2)	0	0	0	0	0	0	0	0	0	0	0	VSPL (0)	HSPL (0)	0	EPL (0)	DPL (0)
010h	Panel interface Control 1	0	0	0	0	0	0	DIVI1 (0)	DIVI0 (0)	0	0	0	RTNI4 (1)	RTNI3 (0)	RTNI2 (1)	RTNI1 (1)	RTNI0 (1)
011h	Panel interface Control 2	0	0	0	0	0	NOWI2 (0)	NOWI1 (0)	NOWI0 (0)	0	0	0	0	0	SDTI2 (0)	SDTI1 (0)	SDTI0 (0)
012h	Panel interface Control 3	0	0	0	0	0	0	VEQW11 (0)	VEQW10 (0)	0	0	0	0	0	0	0	0
013-01Fh	Setting Disabled																
020h	Panel Interface Control 4	0	0	0	0	0	0	DIVE1 (0)	DIVE0 (0)	0	RTNE6 (0)	RTNE5 (0)	RTNE4 (1)	RTNE3 (1)	RTNE2 (1)	RTNE1 (1)	RTNE0 (0)
021h	Panel Interface Control 5	0	0	0	0	NOWE3 (0)	NOWE2 (0)	NOWE1 (0)	NOWE0 (0)	0	0	0	0	SDTE3 (0)	SDTE2 (0)	SDTE1 (0)	SDTE0 (0)
022h	Panel Interface Control 6	0	0	0	0	0	VEQWE2 (0)	VEQWE1 (0)	VEQWE0 (0)	0	0	0	0	0	0	0	0
023h-08Fh	Setting Disabled																
090h	Frame Marker Control	FMKM (0)	FMI2 (0)	FMI1 (0)	FMI0 (0)	0	0	0	FMP8 (0)	FMP7 (0)	FMP6 (0)	FMP5 (0)	FMP4 (0)	FMP3 (0)	FMP2 (0)	FMP1 (0)	FMP0 (0)
091h-0FFh	Setting disabled																
100h	Power Control (1)	0	0	0	SAP (0)	0	BT2 (0)	BT1 (0)	BT0 (0)	APE (0)	0	AP1 (0)	AP0 (0)	0	DSTB (0)	SLP (0)	0
101h	Power Control (2)	0	0	0	0	0	DC12 (0)	DC11 (0)	DC10 (0)	0	DC02 (0)	DC01 (0)	DC00 (0)	0	VC2 (0)	VC1 (0)	VC0 (0)
102h	Power Control (3)	0	0	0	0	0	0	0	VCMR0 (0)	VREG1R (0)	0	PSON (0)	PON (0)	VRH3 (0)	VRH2 (0)	VRH1 (0)	VRH0 (0)
103h	Power Control (4)	0	0	VCOMG (0)	VDV4 (0)	VDV3 (0)	VDV2 (0)	VDV1 (0)	VDV0 (0)	0	0	0	0	0	0	0	0
104h-106h	Setting disabled																
107h	Power Control (5)	0	0	0	0	0	0	0	0	0	0	0	DCM0 (0)	DCT3 (0)	DCT2 (0)	DCT1 (0)	DCT0 (0)
108-10Fh	Setting disabled																
110h	Power Control(6)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PSE (0)
111-1ffh	Setting disabled																
200h	GRAM address Set Horizontal Address	0	0	0	0	0	0	0	0	AD7 (0)	AD6 (0)	AD5 (0)	AD4 (0)	AD3 (0)	AD2 (0)	AD1 (0)	AD0 (0)
201h	GRAM address Set Vertical Address	0	0	0	0	0	0	0	AD16 (0)	AD15 (0)	AD14 (0)	AD13 (0)	AD12 (0)	AD11 (0)	AD10 (0)	AD9 (0)	AD8 (0)
202h	Write Data to GRAM Read Data from GRAM	Data format is varied according to “interface”.															
203-20Fh	Setting disabled																
210h	Window Horzontal RAM Address Start	0	0	0	0	0	0	0	0	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	HSA2 (0)	HSA1 (0)	HSA0 (0)
211h	Window Horzontal RAM Address End	0	0	0	0	0	0	0	0	HEA7 (1)	HEA6 (1)	HEA5 (1)	HEA4 (0)	HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (1)
212h	Window Vertical RAM Address Start	0	0	0	0	0	0	0	VSA8 (0)	VSA7 (0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)
213h	Window Vertical RAM Address End	0	0	0	0	0	0	0	VEA8 (1)	VEA7 (0)	VEA6 (0)	VEA5 (1)	VEA4 (1)	VEA3 (1)	VEA2 (1)	VEA1 (1)	VEA0 (1)
214-27Fh	Setting Disabled																
280h	NVM Write/Read	0	0	0	0	0	0	0	0	0	0	0	0	UID3 (0)	UID2 (0)	UID1 (0)	UID0 (0)
281h	VCom high voltage 1	0	0	0	0	0	0	0	0	0	0	0	VCM14 (0)	VCM13 (0)	VCM12 (0)	VCM11 (0)	VCM10 (0)
282h	VCom high voltage 2	0	0	0	0	0	0	0	0	VCMSEL (0)	0	0	VCM24 (0)	VCM23 (0)	VCM22 (0)	VCM21 (0)	VCM20 (0)
283-2FFh	Setting disabled																
300h	γ Control (1)	0	0	0	V1RP4	V1RP3	V1RP2	V1RP1	V1RP0	0	0	0	V6RN4	V6RN3	V6RN2	V6RN1	V6RN0

301h	γ Control (2)	0	0	V2RP5	V2RP4	V2RP3	V2RP2	V2RP1	V2RP0	0	0	V5RN5	V5RN4	V5RN3	V5RN2	V5RN1	V5RN0
302h	γ Control (3)	0	0	V3RP5	V3RP4	V3RP3	V3RP2	V3RP1	V3RP0	0	0	V4RN5	V4RN4	V4RN3	V4RN2	V4RN1	V4RN0
303h	γ Control (4)	0	0	V4RP5	V4RP4	V4RP3	V4RP2	V4RP1	V4RP0	0	0	V3RN5	V3RN4	V3RN3	V3RN2	V3RN1	V3RN0
304h	γ Control (5)	0	0	V5RP5	V5RP4	V5RP3	V5RP2	V5RP1	V5RP0	0	0	V2RN5	V2RN4	V2RN3	V2RN2	V2RN1	V2RN0
305h	γ Control (6)	0	0	0	V6RP4	V6RP3	V6RP2	V6RP1	V6RP0	0	0	0	V1RN4	V1RN3	V1RN2	V1RN1	V1RN0
306h	γ Control (7)	0	0	0	V7RP4	V7RP3	V7RP2	V7RP1	V7RP0	0	0	0	V8RN4	V8RN3	V8RN2	V8RN1	V8RN0
307h	γ Control (8)	0	0	0	V8RP4	V8RP3	V8RP2	V8RP1	V8RP0	0	0	0	V7RN4	V7RN3	V7RN2	V7RN1	V7RN0
308h	γ Control (9)	0	0	0	0	V9RP3	V9RP2	V9RP1	V9RP0	0	0	0	0	V16RN3	V16RN2	V16RN1	V16RN0
309h	γ Control (10)	0	0	0	0	V10RP3	V10RP2	V10RP1	V10RP0	0	0	0	0	V15RN3	V15RN2	V15RN1	V15RN0
30Ah	γ Control (11)	0	0	0	0	V11RP3	V11RP2	V11RP1	V11RP0	0	0	0	0	V14RN3	V14RN2	V14RN1	V14RN0
30Bh	γ Control (12)	0	0	0	0	V12RP3	V12RP2	V12RP1	V12RP0	0	0	0	0	V13RN3	V13RN2	V13RN1	V13RN0
30Ch	γ Control (13)	0	0	0	0	V13RP3	V13RP2	V13RP1	V13RP0	0	0	0	0	V12RN3	V12RN2	V12RN1	V12RN0
30Dh	γ Control (14)	0	0	0	0	V14RP3	V14RP2	V14RP1	V14RP0	0	0	0	0	V11RN3	V11RN2	V11RN1	V11RN0
30Eh	γ Control (15)	0	0	0	0	V15RP3	V15RP2	V15RP1	V15RP0	0	0	0	0	V10RN3	V10RN2	V10RN1	V10RN0
30Fh	γ Control (16)	0	0	0	0	V16RP3	V16RP2	V16RP1	V16RP0	0	0	0	0	V9RN3	V9RN2	V9RN1	V9RN0
310-3FFh	Setting disabled																
400h	Size of base image	GS (0)	0	NL5 (0)	NL4 (0)	NL3 (0)	NL2 (0)	NL1 (0)	NL0 (0)	0	0	SCN5 (0)	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)
401h	Base image display control	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL (0)	VLE (0)	REV (0)
402-403h	Setting disabled																
404h	Vertical Scoll Control	0	0	0	0	0	0	0	VL8 (0)	VL7 (0)	VL6 (0)	VL5 (0)	VL4 (0)	VL3 (0)	VL2 (0)	VL1 (0)	VL0 (0)
405-4FFh	Setting disabled																
500h	Display Position - Partial Display 1	0	0	0	0	0	0	0	PTDP08 (0)	PTDP07 (0)	PTDP06 (0)	PTDP05 (0)	PTDP04 (0)	PTDP03 (0)	PTDP02 (0)	PTDP01 (0)	PTDP00 (0)
501h	RAM Address Start - Partial Display 1	0	0	0	0	0	0	0	PTSA08 (0)	PTSA07 (0)	PTSA06 (0)	PTSA05 (0)	PTSA04 (0)	PTSA03 (0)	PTSA02 (0)	PTSA01 (0)	PTSA00 (0)
502h	RAM Address End - Partial Display 1	0	0	0	0	0	0	0	PTEA08 (0)	PTEA07 (0)	PTEA06 (0)	PTEA05 (0)	PTEA04 (0)	PTEA03 (0)	PTEA02 (0)	PTEA01 (0)	PTEA00 (0)
503h	Display Position - Partial Display 2	0	0	0	0	0	0	0	PTDP18 (0)	PTDP17 (0)	PTDP16 (0)	PTDP15 (0)	PTDP14 (0)	PTDP13 (0)	PTDP12 (0)	PTDP11 (0)	PTDP10 (0)
504h	RAM Address Start - Partial Display 2	0	0	0	0	0	0	0	PTSA18 (0)	PTSA17 (0)	PTSA16 (0)	PTSA15 (0)	PTSA14 (0)	PTSA13 (0)	PTSA12 (0)	PTSA11 (0)	PTSA10 (0)
505h	RAM Address End - Partial Display 2	0	0	0	0	0	0	0	PTEA18 (0)	PTEA17 (0)	PTEA16 (0)	PTEA15 (0)	PTEA14 (0)	PTEA13 (0)	PTEA12 (0)	PTEA11 (0)	PTEA10 (0)
506-605h	Setting Disabled																
606h	i80-I/F Endian Control	0	0	0	0	0	0	0	TCREV1 (0)	0	0	0	0	0	0	0	TCREV0 (0)
607-6EFh	Setting disabled																
6F0h	NVM access control	0	0	0	0	0	0	0	0	TE (0)	0	EOP1 (0)	EOP0 (0)	0	0	EAD1 (0)	EAD0 (0)
6F1-FFFh	Setting disabled																

The following are detailed explanations of instructions with illustrations of instruction bits (CB15-0) assigned to each interface.

6.2.1. Index Register (IR)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	0	0	0	0	0	0	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the index (R000h ~ RFFFh) of a control register.

6.2.2. ID Read Register (R000h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R	0	0	1	0	1	0	1	0	0	0	0	1	0	0	0	0	0

The IC code of SPFD5420A can be accessed by read operation. '5420H' can be read out when read ID operation is exectued.

6.2.3. Driver Output Control Register (R001h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	SM(0)	0	SS(0)	0	0	0	0	0	0	0	0

SS: Shift direction of the source driver output selection.

When SS = “0”, source driver shifts from S1 to S720. When SS = “1”, source driver shifts from S720 to S1. Moreover, SS can cooperate with BGR for different color filter configuration of LCD panel. The combination of SS and BGR bit are summarized at **Table 6-2.**

Table 6-2

SS=0;BGR=0;	S1	S2	S3	····▶	S718	S719	S720
SS=0;BGR=1;	S1	S2	S3	····▶	S718	S719	S720
SS=1,BGR=0;	S1	S2	S3	◀····	S718	S719	S720
SS=1,BGR=1;	S1	S2	S3	◀····	S718	S719	S720

SM: Set the scan mode of the gate driver output. Moreover, SM can cooperate with GS for different LCD panel gate line layout. The combination of GS and SM bit are summarized at **Table 6-3**.

Table 6-3

SM	GS	Shift Direction (begin,…..,end)
0	0	G1, G2, G3, G4……G429, G430, G431, G432
0	1	G432, G431, G430, G429……G4, G3, G2, G1
1	0	G1, G3, G5, …G429, G431, …G2, G4,... G430, G432
1	1	G432, G430, G428,..G4, G2, ..G429, G431,...G3, G1

6.2.4. LCD Driving Waveform Control (R002h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	B/C(0)	0	0	0	0	0	0	NW1(0)	NW0(0)

NW1-NW0: SPFD5420A provides 1-line inversion for Vcom.

B/C: This bit .is to set the Vcom toggle at frame rate format of N-line inversion format.

B/C=0: Frame inversion.

B/C=1: 1-line inversion.

6.2.5. Entry Mode (R003h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	TRI REG(0	DFM (0)	0	BGR (0)	0	0	HWM (0)	0	ORG (0)	0	I/D1 (1)	I/D0 (1)	AM (0)	0	EPF1 (0)	EPF0 (0)

Table 6-4

Operation mode	ORG	AM	I/D1	I/D0	Function
Mode 1	0	0	0	0	Replace horizontal data
Mode2	0	1	0	1	Replace vertical data
Mode3	1	0	1	0	Conditionally replace horizontal data
Mode4	1	1	1	1	Conditionally replace vertical data

AM: To set the update direction when writing data to GRAM. If AM=1, data will write in vertical direction. If AM=0, data will write in horizontal direction. Moreover, if a fixed window GRAM accessing is desired, the writing direction can be set by I/D1-0 and AM bits.

I/D1-0: To specify address counter increment / decrement automatically function while GRAM is accessing. I/D[0] indicates the increment or decrement in horizontal direction. I/D[1] indicates the increment or decrement in vertical direction.

I/D[0]=0: decrement in horizontal direction automatically

I/D[0]=1: increment in horizontal direction automatically

I/D[1]=0: decrement in vertical direction automatically

I/D[1]=1: increment in vertical direction automatically

ID[1-0] setting can cooperate with AM bit to set the data updating direction.

ORG: SPFD5420A provides the option of start address definition when window function is selected.

ORG=1: RAM address setting should set to (00000h) no matter where the window start address is. In this case, the window start postion is treated as (00000h), regardless the physical location in GRAM.

ORG=0: RAM address setting should set to the address.

HWM: SPFD5420A provides a high speed GRAM accessing mode that updated GRAM data in 1-line unit. Be aware that data can be written to GRAM only if accessing GRAM operation is halted after writing enough data for 1-line. Make sure the AM is set to “0”, when HWM function is set to “1”.

BGR: To set the order of RGB dot location in GRAM.

BGR=0: same assignment of RGB allocation of DB17-0

BGR=1: inverse assignment of RGB allocation of DB17-0

DFM: In combination with TRIREG setting to set the different data transfer mode.

TRIREG: to set 1–3 time transfer mode for system interface. TRIREG bit should cooperate with DFM to meet the specific transfer mode.

For 8-bit databus interface mode:

TRIREG=0: 2 time transfer mode for 16-bit GRAM data.

TRIREG=1: 3 time transfer mode for 18-bit GRAM data

For 16-bit databus interface mode:

TRIREG=0: 1 time transfer mode for 16-bit GRAM data.

TRIREG=1: 2 time transfer mode for 18-bit GRAM data

Note: Set TRIREG=0, when using neither 8-bit nor 16-bit.

EPF1-0: To select the algorithm of expanding 8/16 bits to 18 bits. This setting is valid only when 16-bit or 8-bit interfaces are in use.

6.2.6. Display Control 1 (R007h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	PTDE1 (0)	PTDE0 (0)	0	0	0	BASEE (0)	0	VON (0)	GON (0)	DTE (0)	0	0	D1 (0)	D0 (0)

D1-0: To set the internal operation, source driver output and VCOM output function. When D1-0=00; SPFD5420A is set to standby mode. The combination of D1-0 and BASEE bit is summarized at **Table 6-5**.

Table 6-5

D1	D0	BASEE	Source, VCOM output	Internal Operation	FLM
0	0	*	GND	Terminated	OFF
0	1	*	GND	Normal Operation	ON
1	0	*	Non-lit display	Normal Operation	ON
1	1	0	Non-lit display	Normal Operation	ON
		1	Normal display	Normal Operation	ON

DTE, GON: Specify the high/low level of gate driver output signal. The combination of DTE and GON bit is summarized at **Table 6-6**.

Table 6-6

APE	GON	DTE	Gate Output
0	*	*	VGL(=GND)
1	0	0	VGH
	0	1	VGH
	1	0	VGL
	1	1	VGH/VGL

VON: To Control VCOM output signal. The combination of APE, AP[1:0] , VON and VCOMG bit is summarized at **Table 6-7.**

Table 6-7

APE	AP [1:0]	VON	VCOMG	VCOM Output
0	*	*	*	GND
1	00	0	0	GND
	00	1	0-1	Setting Disabled
	00	0	1	Setting Disabled
	01-11	0	0	GND
	01-11	0	1	VCOML
	01-11	1	0	VCOMH/GND
	01-11	1	1	VCOMH/VCOML

BASEE: To enable Base image display

BASEE	
0	(1) Non-lit display (2) Partial image display
1	Base image is display on the LCD

PTDE1-0: To set the partial-display enables function.

PTDE [0]: "0" Partial image 1 display "Off".
"1" Partial image 1 display "On".

PTDE [1]: "0" Partial image 2 display "Off".
"1" Partial image 2 display "On".

6.2.7. Display Control 2 (R008h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	FP3 (1)	FP2 (0)	FP1 (0)	FP0 (0)	0	0	0	0	BP3 (1)	BP2 (0)	BP1 (0)	BP0 (0)

FP3-0: Set the amount of blank period of front porch

BP3-0: Set the amount of blank period of back porch

Table 6-8 summarized the function of FP3-0/BP3-0 setting. When setting this register, make sure that:

BP + FP ≤ 16 lines

FP ≥ 2 lines

BP ≥ 2 lines

In external display interface mode, a back porch (BP) period starts on the falling edge of the VSYNC signal, followed by a display operation period. After driving the number of lines set with NL bits, a front porch period starts. After the front porch period, a blank period continues until the next input of VSYNC signal. Be aware that different interface mode, has different BP/ FP setting. **Table 6-9** summarized the setting for each interface mode.

Table 6-8

FP3	FP2	FP1	FP0	Number of lines for the Front Porch
BP3	BP2	BP1	BP0	Number of lines for the Back Porch
0	0	0	0	Setting disabled
0	0	0	1	Setting disabled
0	0	1	0	2 lines
0	0	1	1	3 lines
0	1	0	0	4 lines
0	1	0	1	5 lines
0	1	1	0	6 lines
0	1	1	1	7 lines
1	0	0	0	8 lines
1	0	0	1	9 lines
1	0	1	0	10 lines
1	0	1	1	11 lines
1	1	0	0	12 lines
1	1	0	1	13 lines
1	1	1	0	14 lines
1	1	1	1	Setting disabled

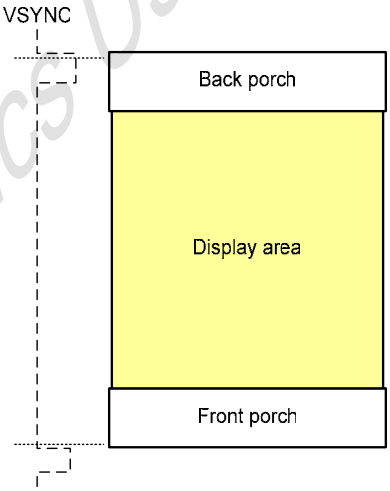


Figure 6-7 Front porch and back porch function diagram

Table 6-9

Operation of Internal clock	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP ≤ 16 lines
RGB interface	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP ≤ 16 lines
VSYNC interface	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP = 16 lines

6.2.8. Display Control 3 (R009h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	PTV (0)	PTS2 (0)	PTS1 (0)	PTS0 (0)	0	0	PTG1 (0)	PTG0 (0)	ISC3 (0)	ISC2 (0)	ISC1 (0)	ISC0 (0)

ISC3-0: To set the gate driver scan cycle in non-display area. **Table 6-10** summarized the function of ISC3-0 setting

Table 6-10

ISC3	ISC2	ISC1	ISC0	Scan cycle	fFLM=60Hz
0	0	0	0	Setting disable	
0	0	0	1	3frames	50 ms
0	0	1	0	5 frames	84 ms
0	0	1	1	7 frames	117 ms
0	1	0	0	9 frames	150 ms
0	1	0	1	11 frames	184 ms
0	1	1	0	13 frames	217 ms
0	1	1	1	15 frames	251 ms
1000-1111				Setting Disabled	

PTG1-0: To set the gate driver scan mode in non-display area. **Table 6-11** summarized the function of PTG1-0 setting

Table 6-11

PTG1	PTG0	Gate outputs in non-display area	Source outputs in non-display area	VCOM output
0	0	Normal scan	Based on the PTS2-0 bits setting	VCOMH/VCOML
0	1	Setting Disable		
1	0	Interval scan	Based on the PTS2-0 bits setting	VCOMH/VCOML
1	1	Setting Disable		

PTS2-0: To set the source driver output level in non-display area of partial display mode. **Table 6-12** summarized the function of PTS2-0 setting.

Table 6-12

PTS2	PTS1	PTS0	Source output in non-display area		Operation amplifier in non-display area
			+ve polarity	-ve polarity	
0	0	0	V31	V0	V0-V31
001-011			Setting inhibited		
1	0	0	V31	V0	V0-V31
101-111			Setting inhibited		

PTV: To set VCOM output in non-display area, Vcom operates normally when PTV = 1, and stops operation when PTV = 0.

6.2.9. Low Power Control (R00Bh)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	VEM0 (0)	0	0	0	COL (0)

COL:

COL = 0: 262,144 colors

COL = 1: 8 colors.

In 8-color mode, the source output is either connected to VREGIOUT or GND.

VEM0: VEM0 = 1, when VCOM is switched from VCOMH to VCOML, it will dropped to GND level in the intermediate stage.

VEM0 = 0, when VCOM is switched from VCOMH to VCOML, it will directly change to VCOML level.

6.2.10. External Display Interface Control 1 (R00Ch)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	ENC2 (0)	ENC1 (0)	ENC0 (0)	0	0	0	RM (0)	0	0	DM1 (0)	DM0 (0)	0	0	RIM1 (0)	RIM0 (0)

RIM1-0: To set the different transfer modes of RGB interface.

Table 6-13 summarized the function of RIM1-0 setting.

Table 6-13

RIM1	RIM0	RGB Interface Mode	Colors	Data Bus
0	0	18-bit RGB interface (one transfer/pixel)	262K	DB 17-0
0	1	16-bit RGB interface (one transfer/pixel)	65K	DB 17-13; DB 11-1
1	0	6-bit RGB interface (three transfers/pixel)	262K	DB17-12
1	1	Setting disabled	-	-

DM1-0: To specify the display interface mode.

Table 6-14summarized the function of DM1-0 setting.

Table 6-14

DM1	DM0	Display Interface
0	0	Internal clock operation
0	1	RGB interface
1	0	VSYNC interface
1	1	Setting disabled

RM: Select the interface to access the SPFD5420A's internal GRAM. The setting of RM should be consistent with DM1-0.

Table 6-15 summarized the function of RM bit setting.

Table 6-15

RM	Interface for RAM Access
0	System interface/VSYNC interface
1	RGB interface

ENC2-0: Set the RAM data write cycle in RGB interface mode.

Table 6-16 summarized the function of ENC2-0 setting.

Table 6-16

ECN2	ECN1	ECN0	RAM data write cycle
0	0	0	1 frame
0	0	1	2 frames
0	1	0	3 frames
0	1	1	4 frames
1	0	0	5 frames
1	0	1	6 frames
1	1	0	7 frames
1	1	1	8 frames

6.2.11. External Display Interface Control 2 (R00Fh)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL (0)	HSPL (0)	0	EPL (0)	DPL (0)

DPL: Select the data latch edge of the DOTCLK signal in RGB interface mode.
DPL = ”0”: rising edge of the DOTCLK.
DPL =”1”: falling edge of the DOTCLK.

HSPL: The polarity of HSYNC signal selection in RGB interface mode.
HSPL = ”0”: Low active.
HSPL = ”1”: High active.

EPL: The polarity of ENABLE signal selection in RGB interface mode.
EPL = “0”: ENABLE: Low active
EPL = ”1”: ENABLE: High active

VSPL: The polarity of VSYNC signal selection in RGB interface mode.
VSPL = ”0”: Low active.
VSPL = ”1”: High active.

6.2.12. Panel Interface Control 1 (R010h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	DIVI1 (0)	DIVI0 (0)	0	0	0	RTNI4 (1)	RTNI3 (0)	RTNI2 (1)	RTNI1 (1)	RTNI0 (1)

RTNI4-0: Set the clock cycle per line **Table 6-17** summarized the function of RTNI4-0 setting.

Table 6-17

RTNI4	RTNI3	RTNI2	RTNI1	RTNI0	Clock Cycles per line
0	0	0	0	0	Setting disable
Setting disable					
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks

DIVI1-0: To specified the division ratio of internal operation clock frequency. Set the RTN and DIVI bits to adjust frame frequency. Be aware of that if the number of lines for driving liquid crystal is changed, the frame frequency must also be adjusted. Moreover, In RGB interface mode, the DIVI1-0 bits are disabled. **Table 6-18** summarized the function of DIVI1-0 setting.

Table 6-18

DIVI1	DIVI0	Division Ratio	Internal Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

fosc =Frequency of RC oscillation

Formula to calculate frame frequency

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{Clock cycles per line} \times \text{division ratio} \times (\text{Line} + \text{BP} + \text{FP})} \quad [\text{Hz}]$$

fosc: frequency of RC oscillation
Line: number of lines for driving liquid crystal (NL bits)
Division ratio: DIVI bits
Clock cycles per line: RTNI bits
FP: the number of lines for the front porch period
BP: the number of lines for the back porch period

6.2.13. Panel Interface Control 2 (R011h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	NOWI2 (0)	NOWI1 (0)	NOWI0 (0)	0	0	0	0	0	SDTI2 (0)	SDTI1 (0)	SDTI0 (0)

NOWI [2:0]: Set the adjacent gate driver output non-overlap period. **Table 6-19** summarized the function of NOWI2-0 setting.

Table 6-19

NOWI2	NOWI1	NOWI0	Gate output non-overlap period Internal Operation (reference clock: internal oscillator)
0	0	0	0 clock
0	0	1	1 clocks
0	1	0	2 clocks
0	1	1	3 clocks
1	0	0	4 clocks
1	0	1	5 clocks
1	1	0	6 clocks
1	1	1	7 clocks

SDTI2-0: Set the delay of source output in every line.

Table 6-20

SDTI2	SDTI1	SDTI0	Source output delay period Internal Operation (reference clock: internal oscillator)
0	0	0	0 clock
0	0	1	1 clocks
0	1	0	2 clocks
0	1	1	3 clocks
1	0	0	4 clocks
1	0	1	5 clocks
1	1	0	6 clocks
1	1	1	7 clocks

6.2.14. Panel Interface control 3 (R012h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	VEQW1 (0)	VEQW0 (0)	0	0	0	0	0	0	0	0	0

VEQWI[1:0]: Set VCOM equalize period.

Table 6-21

VEQWI1	VEQWI0	VCOM Equalize Period
0	0	0 clock
0	1	1 clock
1	0	2 clocks
1	1	3 clocks

6.2.15. Panel Interface control 4 (R020h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	DIVE1 (1)	DIVE0 (0)	0	RTNE6 (0)	RTNE5 (0)	RTNE4 (1)	RTNE3 (1)	RTNE2 (1)	RTNE1 (1)	RTNE0 (0)

RTNE6-0: Set the clock cycle per line **Table 6-22** summarized the function of RTNE5-0 setting.

Table 6-22

RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0	Clock Cycles per line
0	0	0	0	0	0	Setting disable
Setting disable						
0	1	0	0	0	0	16 clocks
0	1	0	0	0	1	17 clocks
0	1	0	0	1	0	18 clocks
0	1	0	0	1	1	19 clocks
0	1	0	1	0	0	20 clocks
0	1	0	1	0	1	21 clocks
0	1	0	1	1	0	22 clocks
0	1	0	1	1	1	23 clocks
0	1	1	0	0	0	24 clocks
0	1	1	0	0	1	25 clocks
0	1	1	0	1	0	26 clocks
0	1	1	0	1	1	27 clocks
0	1	1	1	0	0	28 clocks
0	1	1	1	0	1	29 clocks
0	1	1	1	1	0	30 clocks
0	1	1	1	1	1	31 clocks
1	1	0	0	0	0	32 clocks
1	1	0	0	0	1	33 clocks
1	1	0	0	1	0	34 clocks

RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0	Clock Cycles per line
1	1	0	0	1	1	35 clocks
1	1	0	1	0	0	36 clocks
1	1	0	1	0	1	37 clocks
1	1	0	1	1	0	38 clocks
1	1	0	1	1	1	39 clocks
1	1	1	0	0	0	40 clocks
1	1	1	0	0	1	41 clocks
1	1	1	0	1	0	42 clocks
1	1	1	0	1	1	43 clocks
1	1	1	1	0	0	44 clocks
1	1	1	1	0	1	45 clocks
1	1	1	1	1	0	46 clocks
1	1	1	1	1	1	47 clocks
1	1	0	0	0	0	48 clocks
1	1	0	0	0	1	49 clocks
1	1	0	0	1	0	50 clocks
1	1	0	0	1	1	51 clocks
1	1	0	1	0	0	52 clocks
1	1	0	1	0	1	53 clocks
1	1	0	1	1	0	54 clocks
1	1	0	1	1	1	55 clocks
1	1	1	0	0	0	56 clocks
1	1	1	0	0	1	57 clocks
1	1	1	0	1	0	58 clocks
1	1	1	0	1	1	59 clocks
1	1	1	1	0	0	60 clocks
1	1	1	1	0	1	61 clocks
1	1	1	1	1	0	62 clocks
1	1	1	1	1	1	63 clocks

DIVE1-0: To specified the division ratio of internal operation clock frequency. Set the RTNE and DIVE bits to adjust frame frequency. Be aware of that if the number of lines for driving liquid crystal is changed, the frame frequency must also be adjusted. Moreover, In RGB interface mode, the DIVE1-0 bits are disabled. **Table 6-23** summarized the function of DIVE1-0 setting.

Table 6-23

DIVE1	DIVE0	Division Ratio	Internal Operation Clock Frequency (16 bit, one time transfer)	Internal Operation Clock Frequency(8 bit, three time transfer)
0	0	Setting disable		
0	1	4	fosc / 4	fosc / 12
1	0	8	fosc / 8	fosc / 24
1	1	16	fosc / 16	fosc / 48

fosc =Frequency of RC oscillation

6.2.16. Panel Interface Control 5 (021Rh)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	NOW E3(0)	NOW E2(0)	NOW E1(0)	NOW E0(0)	0	0	0	0	SDT E3(0)	SDT E2(0)	SDT E1(0)	SDT E0(0)

NOWE [3:0]: Set the adjacent gate driver output non-overlap period in RGB interface. **Table 6-24** summarized the function of NOWE3-0 setting.

Table 6-24

NOWE3	NOWE2	NOWE1	NOWE0	Gate output non-overlap period Internal Operation (reference clock: internal oscillator)
0	0	0	0	0 clock
0	0	0	1	1 clocks
0	0	1	0	2 clocks
0	0	1	1	3 clocks
0	1	0	0	4 clocks
0	1	0	1	5 clocks
0	1	1	0	6 clocks
0	1	1	1	7 clocks
1	0	0	0	8 clocks
1	0	0	1	9 clocks
1	0	1	0	10 clocks
1	0	1	1	11 clocks
1	1	0	0	12 clocks
1	1	0	1	13 clocks
1	1	1	0	14 clocks
1	1	1	1	15 clocks

SDTE: Set the source output delay in RGB interface.

Table 6-25

SDTE3	SDTE 2	SDTE 1	SDTE 0	Source output period Internal Operation (reference clock: internal oscillator)
0	0	0	0	0 clock
0	0	0	1	1 clocks
0	0	1	0	2 clocks
0	0	1	1	3 clocks
0	1	0	0	4 clocks
0	1	0	1	5 clocks
0	1	1	0	6 clocks
0	1	1	1	7 clocks
1	0	0	0	8 clocks
1	0	0	1	9 clocks
1	0	1	0	10 clocks
1	0	1	1	11 clocks
1	1	0	0	12 clocks

1	1	0	1	13 clocks
1	1	1	0	14 clocks
1	1	1	1	15 clocks

6.2.17. Panel Interface Control 6 (R022h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	VEQ WE2(0)	VEQ WE1(0)	VEQ WE0(0)	0	0	0	0	0	0	0	0

VEQWE2-0: To set the drive period of low power VCOM, which is valid when the operation is synchronized with RGB interface signals.

Table 6-26

VEQWE2	VEQWE1	VEQWE0	Source Output Delay Perios
0	0	0	0 clock
0	0	1	1 clocks
0	1	0	2 clocks
0	1	1	3 clocks
1	0	0	4 clocks
1	0	1	5 clocks
1	1	0	6 clocks
1	1	1	7 clocks

6.2.18. Frame Marker Control (R090h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	FMKM (0)	FMI2 (0)	FMI1 (0)	FMI0 (0)	0	0	0	FMP8 (0)	FMP7 (0)	FMP6 (0)	FMP5 (0)	FMP4 (0)	FMP3 (0)	FMP2 (0)	FMP1 (0)	FMP0 (0)

FMP8-0: Set the position of the frame marker. 0 ≤ FMP ≤ BP + NL + FP

Table 6-27

FMP8-0	Frame Marker Position
000000000	0
000000001	1
000000010	2
000000011	3
…	…
110111100	444
110111101	445
110111110	446
110111111	447

FMI2-0: Set the period of the Frame Marker.

Table 6-28

FMI2	FMI1	FMI0	Period of FMARK
0	0	0	1 frame
0	1	1	2 frames
1	0	1	4 frames
1	1	1	6 frames

FMKM:

0: Disable FMARK

1. Enable FMARK

6.2.19. Power Control 1 (R100h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	SAP (0)	0	BT2 (0)	BT1 (0)	BT0 (0)	APE (0)	0	AP1 (0)	AP0 (0)	0	DSTB (0)	SLP (0)	0

SLP: Sleep mode selection. When SLP =1, SPFD5420A set to sleep mode. In sleep mode, all internal operations are terminated except internal RC oscillation. Be sure that a display off sequence should be executed before set SLP to "1". In sleep mode, no instruction can be accepted. Set STB=0 can exit sleep mode. Moreover, when exit from sleep mode, data in GRAM and in instruction registers are remained unchanged.

DSTB: Deep Standby mode selection. When DSTB =1, SPFD5420A set to deep standby mode. In this mode, all internal operations are terminated including internal RC oscillation. Be sure that a display off sequence should be executed before set DSTB to "1". Set DSTB=0 can exit standby mode. Be sure that start oscillation following by 10ms delay should be executed before set DSTB to "0". Moreover, when exit from deep standby mode, data in GRAM and register would be lost, reset and re-sending command and data into GRAM are necessary.

AP1-0: Operational amplifier DC bias current adjustment. Set AP1-0 = "00" to stop operational amplifier and DC/DC charge pump circuits to reduce current consumption during non display period. **Table 6-29** summarized the function of AP1-0 setting. Please note that the values listed in the table are the ratios of the currents of the corresponding settings to the current at the max rank.

Table 6-29

AP1	AP0	Constant current in power supply circuit	Constant current in Gamma circuit
0	0	Halt	Halt
0	1	0.5	0.62
1	0	0.75	0.71
1	1	1	1

APE: Enable bit for both liquid crystal power supply and gamma voltage generation circuit.

APE="0", Halt liquid crystal power supply and gamma voltage generation circuit

APE="1", Enable liquid crystal power supply and gamma voltage generation circuit.

BT3-0: Set the voltage level of DDVDH, VGH, VGL and VCL.

Table 6-30 summarized the function of BT2-0 setting

BT2	BT1	BT0	DDVDH	VGH	VGL	VCL	Capacitor connection pins
0	0	0	VCI1 x 2 [VCI1x2]	DDVDH x 3 [VCI1 x 6]	-(VCI1+DDVDHx 2) [VCI1x -5]	-VCI1 [VCI1x-1]	C23 can be eliminated
0	0	1	Setting Disabled	Setting Disabled	Setting Disabled	Setting Disabled	Setting Disabled
0	1	0	Setting Disabled	Setting Disabled	Setting Disabled	Setting Disabled	Setting Disabled
0	1	1	VCI1 x 2 [x2]	DDVDH x 3 + VCI1 [VCI1 x 7]	-(VCI1+DDVDHx 2) [VCI1x -5]	-VCI1	
1	0	0	VCI1 x 2 [x2]	DDVDH x 3 + VCI1 [VCI1 x 7]	-(DDVDHx 2) [VCI1x -4]	-VCI1	
1	0	1	VCI1 x 2 [x2]	DDVDH x 3 + VCI1 [VCI1 x 7]	-(VCI1+DDVDH) [VCI1x -3]	-VCI1	
1	1	0	VCI1 x 2 [x2]	DDVDH x 3 [VCI1 x 6]	-(DDVDHx 2) [VCI1x -4]	-VCI1	C23 can be eliminated
1	1	1	VCI1 x 2 [x2]	DDVDH x 3 [VCI1 x 6]	-(VCI1+DDVDH) [VCI1x -3]	-VCI1	C23 can be eliminated

SAP: Enable bit for gamma voltage generation circuit.

SAP="0", Halt gamma voltage generation circuit.

SAP="1", Enable gamma voltage generation circuit.

6.2.20. Power Control 2 (R101h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	DC12 (1)	DC11 (1)	DC10 (0)	0	DC02 (1)	DC01 (1)	DC00 (0)	0	VC2 (0)	VC1 (0)	VC0 (0)

VC2-0: Set the voltage of VCIOUT. VCIOUT is generated by VCILVL. **Table 6-31** summarized the function of VC2-0 setting

Table 6-31

VC2	VC1	VC0	VCIOUT
0	0	0	0.94 x VCILVL
0	0	1	0.89 x VCILVL
0	1	0	Setting Disable
0	1	1	Setting Disable
1	0	0	0.76 x VCILVL
1	0	1	Setting Disable
1	1	0	Setting Disable
1	1	1	1.00 x VCILVL

DC02-00: Set DC/DC charge pump circuit 1 operating frequency. **Table 6-32** summarized the function of DC02-00 setting

Table 6-32

DC02	DC01	DC00	DC/DC charge pump circuit 1 frequency (fDCDC1)
0	0	0	Oscillation clock
0	0	1	Oscillation clock / 2
0	1	0	Oscillation clock / 4
0	1	1	Oscillation clock / 8
1	0	0	Oscillation clock / 16
1	0	1	Invalid Setting
1	1	0	Halt Step-up Circuit 1
1	1	1	Invalid Setting

DC12-10: Set DC/DC charge pump circuit 2 operating frequency. **Table 6-33** summarized the function of DC02-00 setting

Table 6-33

DC12	DC11	DC10	Step-up circuit 2 step-up frequency (fDCDC2)
0	0	0	Oscillation clock / 16
0	0	1	Oscillation clock / 32
0	1	0	Oscillation clock / 64
0	1	1	Oscillation clock / 128
1	0	0	Oscillation clock / 256
1	0	1	Setting disabled
1	1	0	Halt Step-up Circuit 2
1	1	1	Setting disabled

6.2.21. Power Control 3 (R102h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	VCM R0(0)	VRE G1R(0	0	PSON ()	PON (0)	VRH3 (0)	VRH2 (0)	VRH1 (0)	VRH0 (0)

VRH3-0: Set the voltage level of VREG1OUT, which generated from VCILVL. **Table 6-34** summarized the function of VRH3-0 setting

Table 6-34

VRH3	VRH2	VRH1	VRH0	VREG1OUT voltage		VRH3	VRH2	VRH1	VRH0	VREG1OUT voltage	
				VCILVL	VCIR					VCILVL	VCIR
0	0	0	0	Halt	Halt	1	0	0	0	VCILVLx1.6	2.5Vx1.6
0	0	0	1	Halt	Halt	1	0	0	1	VCILVLx1.65	2.5Vx1.65
0	0	1	0	Halt	Halt	1	0	1	0	VCILVLx1.7	2.5Vx1.7
0	0	1	1	Halt	Halt	1	0	1	1	VCILVLx1.75	2.5Vx1.75
0	1	0	0	Setting disable	Setting disable	1	1	0	0	VCILVLx1.8	2.5Vx1.8
0	1	0	1	Setting disable	Setting disable	1	1	0	1	VCILVLx1.85	2.5Vx1.85
0	1	1	0	Setting disable	Setting disable	1	1	1	0	VCILVLx1.9	2.5Vx1.9
0	1	1	1	Setting disable	Setting disable	1	1	1	1	Setting disable	Setting disable

PON: VLOUT3 ON/OFF control. Set PON = “0” to stop VLOUT3. Set PON = “1” to start VLOUT3.

PSON: Power Supply control bit for ON/OFF. When turning on power supply, Set PSE = “1” and then set PSON = “1” to start internal power supply operation..

VREG1R: Select reference voltage for VREG1OUT

VREG1R = “0” (default): VCILVL (External) as reference voltage for VREG1OUT.

VREG1R = ”1”: VCIR (internal) as reference voltage for VREG1OUT.

VCMR[0]: Select VCOMH external resistance or internal setting for VCOMH voltage level.

VCMR[0] = “0” use VCOMR (External) setting as VCOMH voltage.

VCMR[0] = ”1”: use register (Internal) setting as VCOMH voltage.

6.2.22. Power Control 4 (R103h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	VCOMG(0)	VDV4 (0)	VDV3 (0)	VDV2 (0)	VDV1 (0)	VDV0 (0)	0	0	0	0	0	0	0	0

VDV4-0: Set the Vcom amplitude. Vcom amplitude is generated from VREG1OUT, the coefficient is valid from 0.7 to 1.24.

Table 6-35

VDV4	VDV3	VDV2	VDV1	VDV0	Vcom amplitude
0	0	0	0	0	VREG1OUT x 0.70
0	0	0	0	1	VREG1OUT x 0.72
0	0	0	1	0	VREG1OUT x 0.74
0	0	0	1	1	VREG1OUT x 0.76
0	0	1	0	0	VREG1OUT x 0.78
0	0	1	0	1	VREG1OUT x 0.80
0	0	1	1	0	VREG1OUT x 0.82
0	0	1	1	1	VREG1OUT x 0.84
0	1	0	0	0	VREG1OUT x 0.86
0	1	0	0	1	VREG1OUT x 0.88
0	1	0	1	0	VREG1OUT x 0.90
0	1	0	1	1	VREG1OUT x 0.92
0	1	1	0	0	VREG1OUT x 0.94
0	1	1	0	1	VREG1OUT x 0.96
0	1	1	1	0	VREG1OUT x 0.98
0	1	1	1	1	VREG1OUT x 1.00
1	0	0	0	0	VREG1OUT x 1.02
1	0	0	0	1	VREG1OUT x 1.04
1	0	0	1	0	VREG1OUT x 1.06
1	0	0	1	1	VREG1OUT x 1.08
1	0	1	0	0	VREG1OUT x 1.10
1	0	1	0	1	VREG1OUT x 1.12
1	0	1	1	0	VREG1OUT x 1.14
1	0	1	1	1	VREG1OUT x 1.16
1	1	0	0	0	VREG1OUT x 1.18
1	1	0	0	1	VREG1OUT x 1.20
1	1	0	1	0	VREG1OUT x 1.22
1	1	0	1	1	VREG1OUT x 1.24
1	1	1	0	0	Setting Disabled
1	1	1	0	1	
1	1	1	1	0	
1	1	1	1	1	

VCOMG: Set the value of VcomL.
When VCOMG = 0, VcomL equals to GND.
When VCOMG = 1, VcomL is set by VDV4-0.

6.2.23. Power Control 5 (R107h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	DCM0 (0)	0	0	0	0

6.2.24. Power Control 6(R110h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PSE

PSE: Power supply enable bit

PSE = “1”, and set PSON can start SPFD5420A power supply system.

PSE = ”0”, power supply system reset. .

6.2.25. GRAM Address Set (Horizontal Address) (R200h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

See R201h.

6.2.26. GRAM Address Set (Vertical Address) (R201h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8

AD16–0: To set the initial address counter for GRAM address. Based on AM and I/D[1:0] setting, the address counter is automatically increment or decrement while data are written to the internal GRAM There is no need to updated AD16-0 every data transfer if AD16-0 was set in the beginning of one frame graphic data. Be aware that address counter is not automatically updated if reading data from the internal GRAM instruction is executed. Moreover, the address counter cannot be accessed when the SPFD5420A is in standby mode.

Table 6-36 summarized the function of AD15-0 setting

Note1: The address AD16-0 should be set in the address counter every frame on the falling edge of VSYNC if RGB interface mode is selected.

Note2: The address AD16-0 should be set when executing an instruction if system or VSYNC interface mode is selected.

Table 6-36

AD16–AD0	GRAM Setting
“00000”H – “000EF”H	Bitmap data for G1
“00100”H – “001EF”H	Bitmap data for G2
“00200”H – “002EF”H	Bitmap data for G3
“00300”H – “003EF”H	Bitmap data for G4
:	:
“1AC00”H – “1ACEF”H	Bitmap data for G399
“1AD00”H – “1ADEF”H	Bitmap data for G430
“1AE00”H – “1AEEF”H	Bitmap data for G431
“1AF00”H – “1AFEF”H	Bitmap data for G432

6.2.27. Write Data to GRAM (R202h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	RAM write data (WD17-0) The DB17-0 pin assignment is different in different transferring modes.															

WD17-0: SPFD5420A supports 18 bits data format. However, if only 16-bit (565format) is input to GRAM, SPFD5420A will expand the 16 bit data into 18-bit format. Same case when RGB interface is selected. Based on the graphic data in GRAM, the grayscale voltage of source driver is selected. **Table 6-37** summarized the source driver grayscale voltage output versus graphic data in GRAM. **Figure 6-8 ~ Figure 6-18** illustrates the pin assignment among data bus (DB17-0), (WD17-0) and GRAM.

Table 6-37

Data in GRAM	Source Driver Grayscale Output – REV=1 (REV=0)	
RGB	**Negative(Postive)**	**Positive(Negative)**
000000	V31	V0
000001	(V30+V31)/2	(V1+V0)/2
000010	V30	V1
000011	(V29+V30)/2	(V2+V1)/2
000100	V29	V2
000101	(V29+V28)/2	(V3+V2)/2
000110	V28	V3
000111	(V28+V27)/2	(V4+V3)/2
001000	V27	V4
001001	(V27+V26)/2	(V5+V4)/2
001010	V26	V5
001011	(V26+V25)/2	(V6+V5)/2
001100	V25	V6
001101	(V25+V24)/2	(V7+V6)/2
001110	V24	V7
001111	(V24+V23)/2	(V8+V7)/2
010000	V23	V8
010001	(V23+V22)/2	(V9+V8)/2
010010	V22	V9
010011	(V22+V21)/2	(V10+V9)/2
010100	V21	V10
010101	(V21+V20)/2	(V11+V10)/2
010110	V20	V11
010111	(V20+V19)/2	(V12+V11)/2
011000	V19	V12
011001	(V19+V18)/2	(V12+V11)/2
011010	V18	V13
011011	(V18+V17)/2	(V13+V12)/2
011100	V17	V14
011101	(V17+V16)/2	(V14+V13)/2
011110	V16	V15
011111	(V16+V15)/2	(V16+V15)/2
100000	V15	V16
100001	(V15+V14)/2	(V17+V16)/2
100010	V14	V17
100011	(V14+V13)/2	(V18+V17)/2
100100	V13	V18
100101	(V13+V12)/2	(V19+V18)/2
100110	V12	V19
100111	(V12+V11)/2	(V20+V19)/2
101000	V11	V20
101001	(V11+V10)/2	(V21+V20)/2
101010	V10	V21
101011	(V10+V9)/2	(V22+V21)/2
101100	V9	V22
101101	(V9+V8)/2	(V23+V22)/2
101110	V8	V23
101111	(V8+V7)/2	(V24+V23)/2
110000	V7	V24
110001	(V7+V6)/2	(V25+V24)/2
110010	V6	V25
110011	(V6+V5)/2	(V26+V25)/2
110100	V5	V26
110101	(V5+V4)/2	(V27+V26)/2
110110	V4	V27
110111	(V4+V3)/2	(V28+V27)/2
111000	V3	V28
111001	(V3+V2)/2	(V29+V28)/2
111010	V2	V29
111011	(V2+V1)/2	(V29+V30)/2
111100	V1	V30
111101	(V1+V0)/2	(V30+V31)/2
111110	(V1+2V0)/2	(V30+2V31)/2
111111	V0	V31

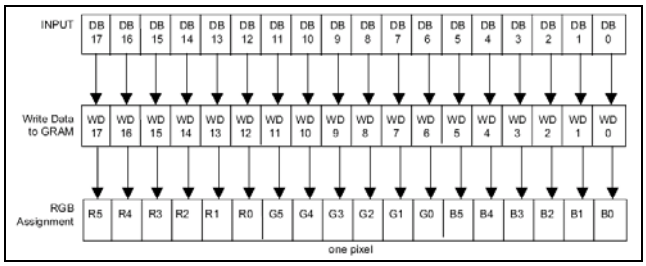


Figure 6-8 18-bit interface (262,144 colors)

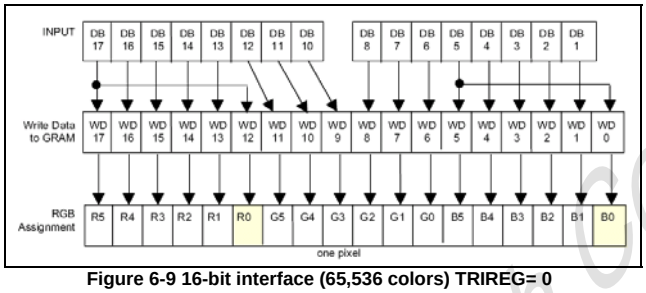


Figure 6-9 16-bit interface (65,536 colors) TRIREG= 0

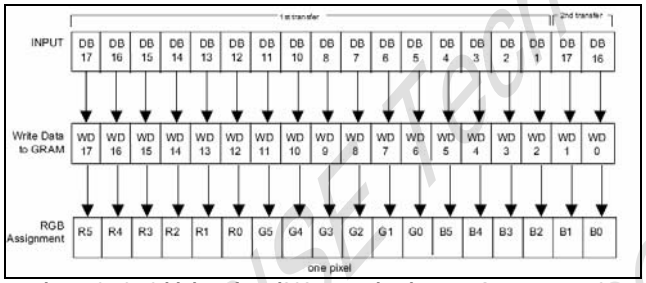


Figure 6-10 16-bit interface (262,144 colors) TRIREG = 1, DFM = 0

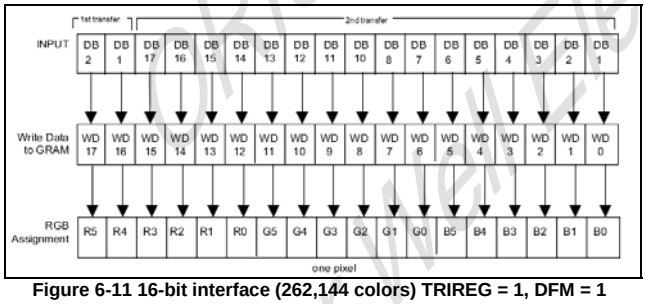


Figure 6-11 16-bit interface (262,144 colors) TRIREG = 1, DFM = 1

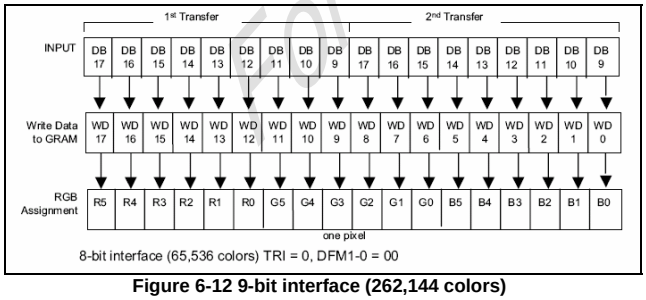


Figure 6-12 9-bit interface (262,144 colors)

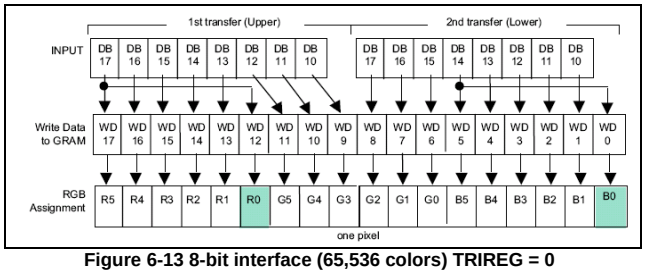


Figure 6-13 8-bit interface (65,536 colors) TRIREG = 0

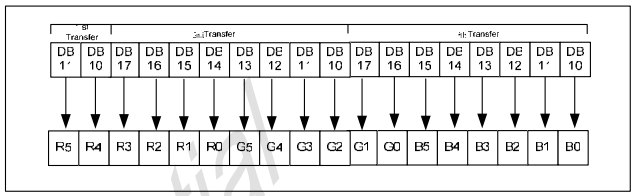


Figure 6-14 8-bit interface 262 colors) TRIREG = 1, DFM=0.

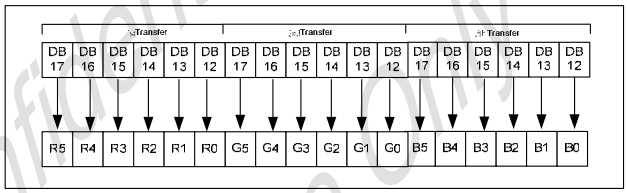


Figure 6-15 8-bit interface (262K colors) TRIREG = 1, DFM=1

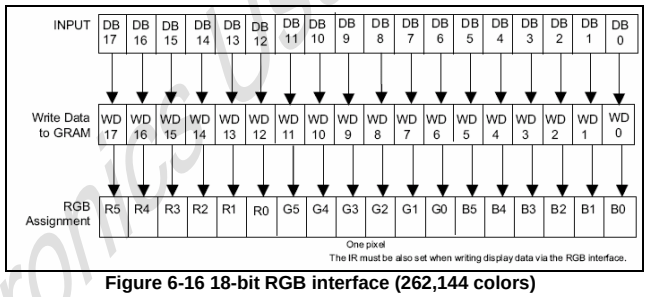


Figure 6-16 18-bit RGB interface (262,144 colors)

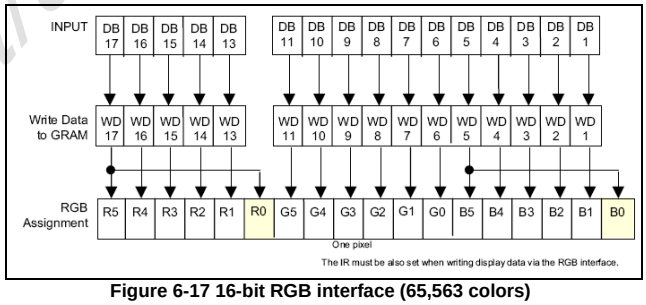


Figure 6-17 16-bit RGB interface (65,563 colors)

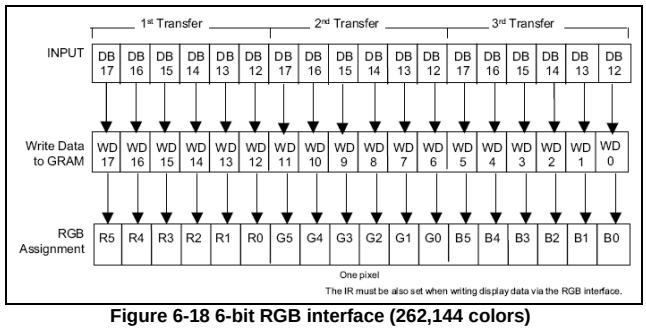


Figure 6-18 6-bit RGB interface (262,144 colors)

SPFD5420A supports external (RGB) interface. In RGB interface mode, all graphic data are stored in GRAM. To meet the diverse requirement of small size LCD panel, SPFD5420A also supports in a fix window using RGB interface and outside the window still use system interface.

In RGB interface mode, data writing to the internal RAM is synchronized with DOTCLK during ENABLE = "Low". Set ENABLE "High" to terminate writing data to RAM. Wait for a write/read bus cycle time. If accessing internal RAM using the RGB interface is desired after accessing the RAM via the system interface. **Figure 6-19** illustrates the timing diagram while RGB and system interface are both use in the same time.

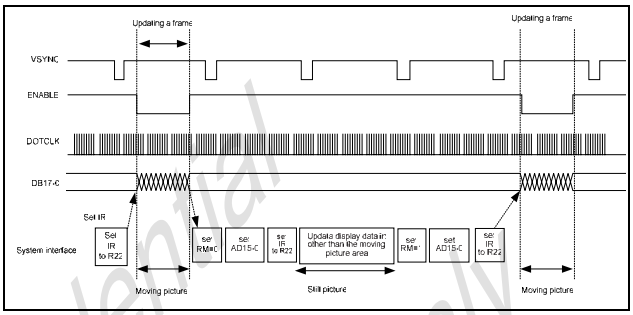


Figure 6-19

6.2.28. Read Data Read from GRAM (R202h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	RAM Read data (RD17-0) The DB17-0 pin assignment is different in different transferring modes.															

R202 also served as a register, which store the data read out from GRAM. When data are read out from the GRAM is desired, first sets the RAM address and executes first word read, and issues second word read. When first word read instruction is issued, Invalid data are sent to the data bus DB17-0. Valid data are sent to the data bus as second word data is executed.

The LSBs of R and B dots cannot read out, when the 8 or 16-bit interface is selected,

Note: This register is not available with the RGB interface. **Figure 6-20** and
Figure 6-23 **Figure 6-23** illustrates the pin assignment among data bus (DB17-0), R22 (RD17-0) and GRAM in read data instruction.

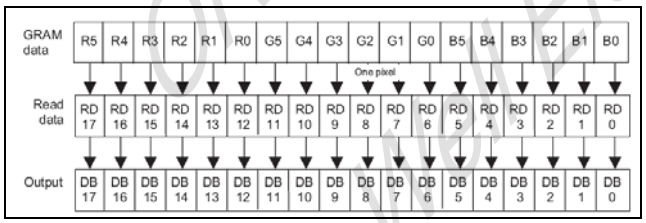


Figure 6-20 18-bit interface

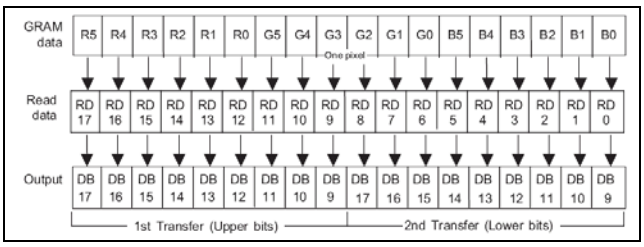


Figure 6-22 9-bit interface

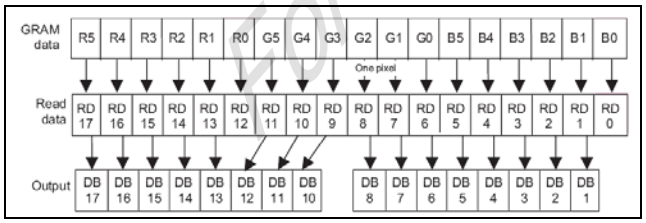


Figure 6-21 16-bit interface

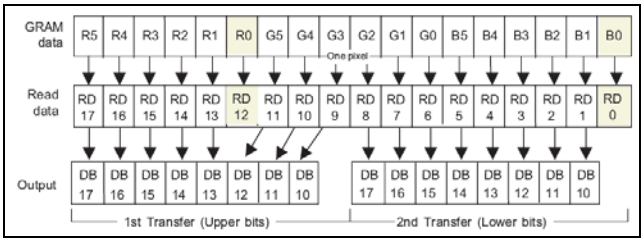


Figure 6-23 8-bit interface / SPI

6.2.29. NVM read data 1 (R280h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	UID3 (0)	UID2 (0)	UID1 (0)	UID0 (0)

See R282h

6.2.30. NVM read data 2 (R281h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	VCM 14(0)	VCM 13(0)	VCM 12(0)	VCM 11(0)	VCM 10(0)

See R282h

6.2.31. NVM read data 3 (R282h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	VCM SEL	0	0	VCM 24(0)	VCM 23(0)	VCM 22(0)	VCM 21(0)	VCM 20(0)

UID[3:0]: SPFD5420A provides a 4-bit identification code UID[3:0] for user to use. UID[3:0] can be write / read from NVM. UID can be read out via R280h.

VCM1 [4:0]: These pins are to set the factor for generating VCOMH when VCMSEL="0". **Table 6-38** summarized the the factor of VERG1OUT

Table 6-38

VCM1[4:0]	VCOMH voltage
5'h00	VREG1OUT x 0.69
5'h01	VREG1OUT x 0.70
5'h02	VREG1OUT x 0.71
5'h03	VREG1OUT x 0.72
5'h04	VREG1OUT x 0.73
5'h05	VREG1OUT x 0.74
5'h06	VREG1OUT x 0.75
5'h07	VREG1OUT x 0.76
5'h08	VREG1OUT x 0.77
5'h09	VREG1OUT x 0.78
5'h0A	VREG1OUT x 0.79
5'h0B	VREG1OUT x 0.80
5'h0C	VREG1OUT x 0.81
5'h0D	VREG1OUT x 0.82
5'h0E	VREG1OUT x 0.83
5'h0F	VREG1OUT x 0.84
5'h10	VREG1OUT x 0.85
5'h11	VREG1OUT x 0.86
5'h12	VREG1OUT x 0.87
5'h13	VREG1OUT x 0.88
5'h14	VREG1OUT x 0.89
5'h15	VREG1OUT x 0.90
5'h16	VREG1OUT x 0.91
5'h17	VREG1OUT x 0.92
5'h18	VREG1OUT x 0.93
5'h19	VREG1OUT x 0.94
5'h1A	VREG1OUT x 0.95
5'h1B	VREG1OUT x 0.96
5'h1C	VREG1OUT x 0.97
5'h1D	VREG1OUT x 0.98
5'h1E	VREG1OUT x 0.99
5'h1F	VREG1OUT x 1.00

VCM2 [4:0]: These pins are to set the factor for generating VCOMH when VCMSEL="1". **Table 6-39** summarized the the factor of VERG1OUT

Table 6-39

VCM2[4:0]	VCOMH voltage
5'h00	VREG1OUT x 0.69
5'h01	VREG1OUT x 0.70
5'h02	VREG1OUT x 0.71
5'h03	VREG1OUT x 0.72
5'h04	VREG1OUT x 0.73
5'h05	VREG1OUT x 0.74
5'h06	VREG1OUT x 0.75
5'h07	VREG1OUT x 0.76
5'h08	VREG1OUT x 0.77
5'h09	VREG1OUT x 0.78
5'h0A	VREG1OUT x 0.79
5'h0B	VREG1OUT x 0.80
5'h0C	VREG1OUT x 0.81
5'h0D	VREG1OUT x 0.82
5'h0E	VREG1OUT x 0.83
5'h0F	VREG1OUT x 0.84
5'h10	VREG1OUT x 0.85
5'h11	VREG1OUT x 0.86
5'h12	VREG1OUT x 0.87
5'h13	VREG1OUT x 0.88
5'h14	VREG1OUT x 0.89
5'h15	VREG1OUT x 0.90
5'h16	VREG1OUT x 0.91
5'h17	VREG1OUT x 0.92
5'h18	VREG1OUT x 0.93
5'h19	VREG1OUT x 0.94
5'h1A	VREG1OUT x 0.95
5'h1B	VREG1OUT x 0.96
5'h1C	VREG1OUT x 0.97
5'h1D	VREG1OUT x 0.98
5'h1E	VREG1OUT x 0.99
5'h1F	VREG1OUT x 1.00

VCMSEL: VCMSEL is to select VCM1 or VCM2; When VCMSEL="0", VCM1 is selected while VCMSEL="1", VCM2 is selected.

6.2.32. Window Horizontal RAM Address Start (R210h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	HAS (0)2	HSA1 (0)	HSA0 (0)

See R213h.

6.2.33. Window Horziontal RAM Address End (R211h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	HEA7 (1)	HEA6 (1)	HEA5 (1)	HEA4 (1)	HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (1)

See R213h.

6.2.34. Window Vertical RAM Address Start (R212h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	VSA8 (0)	VSA7 (0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)

See R213h.

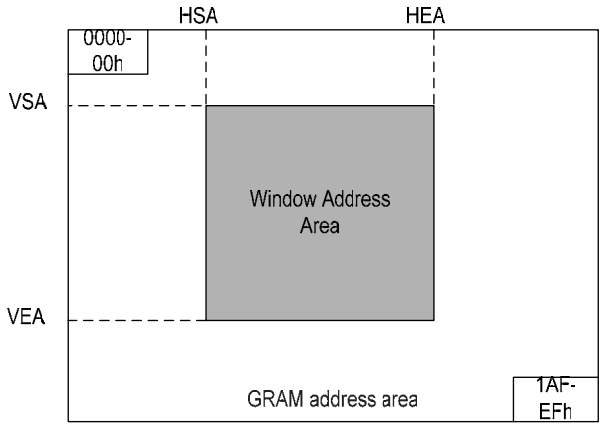
6.2.35. Window Vertical RAM Address End (R213h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	VEA8 (1)	VEA7 (1)	VEA6 (1)	VEA5 (1)	VEA4 (1)	VEA3 (1)	VEA2 (1)	VEA1 (1)	VEA0 (1)

HSA7-0/HEA7-0: SPFD5420A provides window access function. Set HSA7-0 and HEA7-0 represent the start address and end address of the window function in horizontal direction. To use window-accessing function, HSA and HEA bits must be set before starting RAM write operation. Be aware that "00"h ≤ HSA7-0< HEA7-0 ≤ "EF"h and HEA-HAS>="04h".

VSA8-0/VEA8-0: SPFD5420A provides window access function. Set VSA8-0 and VEA8-0 represent the start address and end address of the window in vertical direction. To use window-accessing function, VSA and VEA bits must be set before starting RAM write operation. Be aware that "00"h ≤ VSA8-0< VEA8-0 ≤ 9'h1AF.

Figure 6-24 illustrates the window-accessing function.



6.2.36. γ Control (R300h to R30Fh)

	R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R300	W	1	0	0	0	V1RP4	V1RP3	V1RP2	V1RP1	V1RP0	0	0	0	V6RN4	V6RN3	V6RN2	V6RN1	V6RN0
R301	W	1	0	0	V2RP5	V2RP4	V2RP3	V2RP2	V2RP1	V2RP0	0	0	V5RN5	V5RN4	V5RN3	V5RN2	V5RN1	V5RN0
R302	W	1	0	0	V3RP5	V3RP4	V3RP3	V3RP2	V3RP1	V3RP0	0	0	V4RN5	V4RN4	V4RN3	V4RN2	V4RN1	V4RN0
R303	W	1	0	0	V4RP5	V4RP4	V4RP3	V4RP2	V4RP1	V4RP0	0	0	V3RN5	V3RN4	V3RN3	V3RN2	V3RN1	V3RN0

R304	W	1	0	0	V5RP5	V5RP4	V5RP3	V5RP2	V5RP1	V5RP0	0	0	V2RN5	V2RN4	V2RN3	V2RN2	V2RN1	V2RN0
R305	W	1	0	0	0	V6RP4	V6RP3	V6RP2	V6RP1	V6RP0	0	0	0	V1RN4	V1RN3	V1RN2	V1RN1	V1RN0
R306	W	1	0	0	0	V7RP4	V7RP3	V7RP2	V7RP1	V7RP0	0	0	0	V8RN4	V8RN3	V8RN2	V8RN1	V8RN0
R307	W	1	0	0	0	V8RP4	V8RP3	V8RP2	V8RP1	V8RP0	0	0	0	V7RN4	V7RN3	V7RN2	V7RN1	V7RN0
R308	W	1	0	0	0	0	V9RP3	V9RP2	V9RP1	V9RP0	0	0	0	0	V16RN3	V16RN2	V16RN1	V16RN0
R309	W	1	0	0	0	0	V10RP3	V10RP2	V10RP1	V10RP0	0	0	0	0	V15RN3	V15RN2	V15RN1	V15RN0
R30A	W	1	0	0	0	0	V11RP3	V11RP2	V11RP1	V11RP0	0	0	0	0	V14RN3	V14RN2	V14RN1	V14RN0
R30B	W	1	0	0	0	0	V12RP3	V12RP2	V12RP1	V12RP0	0	0	0	0	V13RN3	V13RN2	V13RN1	V13RN0
R30C	W	1	0	0	0	0	V13RP3	V13RP2	V13RP1	V13RP0	0	0	0	0	V12RN3	V12RN2	V12RN1	V12RN0
R30D	W	1	0	0	0	0	V14RP3	V14RP2	V14RP1	V14RP0	0	0	0	0	V11RN3	V11RN2	V11RN1	V11RN0
R30E	W	1	0	0	0	0	V15RP3	V15RP2	V15RP1	V15RP0	0	0	0	0	V10RN3	V10RN2	V10RN1	V10RN0
R30F	W	1	0	0	0	0	V16RP3	V16RP2	V16RP1	V16RP0	0	0	0	0	V9RN3	V9RN2	V9RN1	V9RN0

- **Control (R300h to R30Fh):** SPFD5420A provides 16 gamma registers to fine tune gamma output voltage.

V1RP[4:0]: register for positive VSD0 fine tune adjustment.
V2RP[5:0]: register for positive VSD1 fine tune adjustment.
V3RP[5:0]: register for positive VSD2 fine tune adjustment.
V4RP[5:0]: register for positive VSD61 fine tune adjustment.
V5RP[5:0]: register for positive VSD62 fine tune adjustment.
V6RP[4:0]: register for positive VSD63 fine tune adjustment.
V7RP[4:0]: register for positive VSD13 fine tune adjustment.
V8RP[4:0]: register for positive VSD50 fine tune adjustment.
V9RP[3:0]: register for positive VSD4 fine tune adjustment.
V10RP[3:0]: register for positive VSD8 fine tune adjustment.
V11RP[3:0]: register for positive VSD20 fine tune adjustment.
V12RP[3:0]: register for positive VSD27 fine tune adjustment.
V13RP[3:0]: register for positive VSD36 fine tune adjustment.
V14RP[3:0]: register for positive VSD43 fine tune adjustment.
V15RP[3:0]: register for positive VSD55 fine tune adjustment.
V16RP[3:0]: register for positive VSD59 fine tune adjustment.

V1RN[4:0]: register for negative VSD0 fine tune adjustment.
V2RN[5:0]: register for negative VSD1 fine tune adjustment.
V3RN[5:0]: register for negative VSD2 fine tune adjustment.
V4RN[5:0]: register for negative VSD61 fine tune adjustment.
V5RN[5:0]: register for negative VSD62 fine tune adjustment.
V6RN[4:0]: register for negative VSD63 fine tune adjustment.
V7RN[4:0]: register for negative VSD13 fine tune adjustment.
V8RN[4:0]: register for negative VSD50 fine tune adjustment.
V9RN[3:0]: register for negative VSD4 fine tune adjustment.
V10RN[3:0]: register for negative VSD8 fine tune adjustment.
V11RN[3:0]: register for negative VSD20 fine tune adjustment.
V12RN[3:0]: register for negative VSD27 fine tune adjustment.
V13RN[3:0]: register for negative VSD36 fine tune adjustment.
V14RN[3:0]: register for negative VSD43 fine tune adjustment.
V15RN[3:0]: register for negative VSD55 fine tune adjustment.
V16RN[3:0]: register for negative VSD59 fine tune adjustment.

6.2.37. Base Image Number of Line (R400h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	GS (0)	0	NL5 (0)	NL4 (0)	NL3 (0)	NL2 (0)	NL1 (0)	NL0 (0)	0	0	SCN5 (0)	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)

SCN5-0: Set the SCN5-0 bits can specify the starting position of the gate driver. The start position of gate driver is determined by the combination of the setting of GS and SM. **Table 6-40** summarized the starting position for each SCN5-0 setting.

Table 6-40 (whenSM=0)

SCN5	SCN4	SCN3	SCN2	SCN1	SCN0	Scan Start Position (Gate line)	
						GS = "0"	GS = "1"
0	0	0	0	0	0	G1	G432
0	0	0	0	0	1	G9	G424
0	0	0	0	1	0	G17	G416
0	0	0	0	1	1	G25	G408
0	0	0	1	0	0	G33	G400
0	0	0	1	0	1	G41	G392
0	0	0	1	1	0	G49	G384
0	0	0	1	1	1	G57	G376
0	0	1	0	0	0	G65	G368
0	0	1	0	0	1	G73	G360

SC N5	SC N4	SC N3	SC N2	SC N1	SC N0	Scan Start Position (Gate line)	
						GS = "0"	GS = "1"
0	0	1	0	1	0	G81	G352
0	0	1	0	1	1	G89	G344
0	0	1	1	0	0	G97	G336
0	0	1	1	0	1	G105	G328
0	0	1	1	1	0	G113	G320
0	0	1	1	1	1	G121	G312
0	1	0	0	0	0	G129	G304
0	1	0	0	0	1	G137	G296
0	1	0	0	1	0	G145	G288
0	1	0	0	1	1	G153	G280
0	1	0	1	0	0	G161	G272
0	1	0	1	0	1	G169	G264
0	1	0	1	1	0	G177	G256
0	1	0	1	1	1	G185	G248
0	1	1	0	0	0	G193	G240
0	1	1	0	0	1	G201	G232
0	1	1	0	1	0	G209	G224
0	1	1	0	1	1	G217	G216
0	1	1	1	0	0	G225	G208
0	1	1	1	0	1	G233	G200
0	1	1	1	1	0	G241	G192
0	1	1	1	1	1	G249	G184
1	0	0	0	0	0	G257	G176
1	0	0	0	0	1	G265	G168
1	0	0	0	1	0	G273	G160
1	0	0	0	1	1	G281	G152
1	0	0	1	0	0	G289	G144
1	0	0	1	0	1	G297	G136
1	0	0	1	1	0	G305	G128
1	0	0	1	1	1	G313	G120
1	0	1	0	0	0	G321	G112
1	0	1	0	0	1	G329	G104
1	0	1	0	1	0	G337	G96
1	0	1	0	1	1	G345	G88
1	0	1	1	0	0	G353	G80
1	0	1	1	0	1	G361	G72
1	0	1	1	1	0	G369	G64
1	0	1	1	1	1	G377	G56
1	1	0	0	0	0	G385	G48
1	1	0	0	0	1	G393	G40
1	1	0	0	1	0	G401	G32
1	1	0	0	1	1	G409	G24
1	1	0	1	0	0	G417	G16
1	1	0	1	0	1	G425	G8
1	1	0	1	1	0	Setting disabled	
Setting disabled							
1	1	1	1	1	1	Setting disabled	

Table 6-41 (whenSM=1)

SC N5	SC N4	SC N3	SC N2	SC N1	SC N0	Scan Start Position (Gate line)	
						GS = "0"	GS = "1"
0	0	0	0	0	0	G1	G432
0	0	0	0	0	1	G17	G416
0	0	0	0	1	0	G33	G400
0	0	0	0	1	1	G49	G384
0	0	0	1	0	0	G65	G368
0	0	0	1	0	1	G81	G352
0	0	0	1	1	0	G97	G336
0	0	0	1	1	1	G113	G320
0	0	1	0	0	0	G129	G304
0	0	1	0	0	1	G145	G288
0	0	1	0	1	0	G161	G272
0	0	1	0	1	1	G177	G256
0	0	1	1	0	0	G193	G240
0	0	1	1	0	1	G209	G224
0	0	1	1	1	0	G225	G208
0	0	1	1	1	1	G241	G192
0	1	0	0	0	0	G257	G176
0	1	0	0	0	1	G273	G160
0	1	0	0	1	0	G289	G144
0	1	0	0	1	1	G305	G128
0	1	0	1	0	0	G321	G112
0	1	0	1	0	1	G337	G96
0	1	0	1	1	0	G353	G80
0	1	0	1	1	1	G369	G64
0	1	1	0	0	0	G385	G48
0	1	1	0	0	1	G401	G32
0	1	1	0	1	0	G417	G16
0	1	1	0	1	1	G2	G431
0	1	1	1	0	0	G18	G415
0	1	1	1	0	1	G34	G399
0	1	1	1	1	0	G50	G383
0	1	1	1	1	1	G66	G367
1	0	0	0	0	0	G82	G351
1	0	0	0	0	1	G98	G335
1	0	0	0	1	0	G114	G319
1	0	0	0	1	1	G130	G303
1	0	0	1	0	0	G146	G287
1	0	0	1	0	1	G162	G271
1	0	0	1	1	0	G178	G255
1	0	0	1	1	1	G194	G239
1	0	1	0	0	0	G210	G223
1	0	1	0	0	1	G226	G207
1	0	1	0	1	0	G242	G191
1	0	1	0	1	1	G258	G175
1	0	1	1	0	0	G274	G159
1	0	1	1	0	1	G290	G143
1	0	1	1	1	0	G306	G127
1	0	1	1	1	1	G322	G111
1	1	0	0	0	0	G338	G95
1	1	0	0	0	1	G354	G79
1	1	0	0	1	0	G370	G63
1	1	0	0	1	1	G386	G47
1	1	0	1	0	0	G402	G31
1	1	0	1	0	1	G418	G15
1	1	0	1	1	0	Setting disabled	
Setting disabled							
1	1	1	1	1	1		

NL5-0: Set the number of gate lines for different resolution of display panel. The combination of NL5-NL0 represents the gate line number are summarized at **Table 6-42**.

Table 6-42

NL5	NL4	NL3	NL2	NL1	NL0	Display Size	No. of Lines	Driven gate lines
0	0	0	0	0	0	Setting disabled	Setting disabled	Setting disabled
0	0	0	0	0	1	720 x 16 dots	16	G1 ~ G16
0	0	0	0	1	0	720 x 24 dots	24	G1 ~ G24
0	0	0	0	1	1	720 x 32 dots	32	G1 ~ G32
0	0	0	1	0	0	720 x 40 dots	40	G1 ~ G40
0	0	0	1	0	1	720 x 48 dots	48	G1 ~G48
0	0	0	1	1	0	720 x 56 dots	56	G1 ~ G56
0	0	0	1	1	1	720 x 64 dots	64	G1 ~ G64
0	0	1	0	0	0	720 x 72 dots	72	G1 ~ G72
0	0	1	0	0	1	720 x 80 dots	80	G1 ~ G80
0	0	1	0	1	0	720 x 88 dots	88	G1 ~ G88
0	0	1	0	1	1	720 x 96 dots	96	G1 ~ G96
0	0	1	1	0	0	720 x 104 dots	104	G1 ~ G104
0	0	1	1	0	1	720 x 112 dots	112	G1 ~ 112
0	0	1	1	1	0	720 x 120 dots	120	G1 ~ 120
0	0	1	1	1	1	720 x 128 dots	128	G1 ~ 128
0	1	0	0	0	0	720 x 136 dots	136	G1 ~ 136
0	1	0	0	0	1	720 x 144 dots	144	G1 ~ 144
0	1	0	0	1	0	720 x 152 dots	152	G1 ~ 152
0	1	0	0	1	1	720 x 160 dots	160	G1 ~ 160
0	1	0	1	0	0	720 x 168 dots	168	G1 ~ 168
0	1	0	1	0	1	720 x 176 dots	176	G1 ~ 176
0	1	0	1	1	0	720 x 184 dots	184	G1 ~ 184
0	1	0	1	1	1	720 x 192 dots	192	G1 ~ 192
0	1	1	0	0	0	720 x 200 dots	200	G1 ~ 200
0	1	1	0	0	1	720 x 208 dots	208	G1 ~ 208
0	1	1	0	1	0	720 x 216 dots	216	G1 ~ 216
0	1	1	0	1	1	720 x 224 dots	224	G1 ~ 224
0	1	1	1	0	0	720 x 232 dots	232	G1 ~ 232
0	1	1	1	0	1	720 x 240 dots	240	G1 ~ 240
0	1	1	1	1	0	720 x 248 dots	248	G1 ~ 248
0	1	1	1	1	1	720 x 256 dots	256	G1 ~ 256
1	0	0	0	0	0	720 x 264 dots	264	G1 ~ 264
1	0	0	0	0	1	720 x 272 dots	272	G1 ~ 272
1	0	0	0	1	0	720 x 280 dots	280	G1 ~ 280
1	0	0	0	1	1	720 x 288 dots	288	G1 ~ 288
1	0	0	1	0	0	720 x 296 dots	296	G1 ~ 296
1	0	0	1	0	1	720 x 304 dots	304	G1 ~ 304
1	0	0	1	1	0	720 x 312 dots	312	G1 ~ 312
1	0	0	1	1	1	720 x 320 dots	320	G1 ~ 320
1	0	1	0	0	0	720 x 328 dots	328	G1 ~ 328

NL5	NL4	NL3	NL2	NL1	NL0	Display Size	No. of Lines	Driven gate lines
1	0	1	0	0	1	720 x 336 dots	336	G1 ~ 336
1	0	1	0	1	0	720 x 344 dots	344	G1 ~ 344
1	0	1	0	1	1	720 x 352 dots	352	G1 ~ 352
1	0	1	1	0	0	720 x 360 dots	360	G1 ~ 360
1	0	1	1	0	1	720 x 368 dots	368	G1 ~ 368
1	0	1	1	1	0	720 x 376 dots	376	G1 ~ 376
1	0	1	1	1	1	720 x 384 dots	384	G1 ~ 384
1	1	0	0	0	0	720 x 392 dots	392	G1 ~ 392
1	1	0	0	0	1	720 x 400 dots	400	G1 ~ 400
1	1	0	0	1	0	720 x 408 dots	408	G1 ~ 408
1	1	0	0	1	1	720 x 416 dots	416	G1 ~ 416
1	1	0	1	0	0	720 x 424 dots	424	G1 ~ 424
1	1	0	1	0	1	720 x 430 dots	430	G1 ~ 430
Setting Disabled								

Note: Back porch and a front porch (set with BP/FP bits respectively) are inserted before/ after driving all gate lines.

GS: Shift direction of the gate driver output selection. When
GS="0", gate driver shift from G1 to G320. When GS = "1", gate driver shift from G432 to G1.

6.2.38. Base Image Display Control (R401h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL (0)	VLE (0)	REV (0)

REV: To set the grayscale corresponding to normally white or normally black LCD panel from same data input. **Table 6-43** summarized REV bit function.

Table 6-43

REV	GRAM data	Source Driver Output	
		Positive Polarity	Negative Polarity
0	18'h00000	V63	V0
	⋮	⋮	⋮
	18'h3FFFF	V0	V63
1	18'h00000	V0	V63
	⋮	⋮	⋮
	18'h3FFFF	V63	V0

VLE: SPFD5420A provides vertical scrolling function which can be set by VLE bit.
VLE = "1", vertical scrolling function enable. The amout of scrolling line from the first line is determined by VL[8:0].
VLE = "0", normal display.

NDL: set the source driver output level in non-lit area..
NDL = "1", Positive = V0, Negative = V31;
NDL = "0", Postive = V31 and Negative = V0.

6.2.39. Based Image Vertical Scroll Control (R404h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	VL8 (0)	VL7 (0)	VL6 (0)	VL5 (0)	VL4 (0)	VL3 (0)	VL2 (0)	VL1 (0)	VL0 (0)

VL8-0: SPFD5420A provides scrolling function. The start position for displaying the image is shifted vertically by the number of lines based on the setting of the VL8-0 bits. Be aware that the vertical scrolling function is not available in the external (RGB) display interface mode. **Table 6-44** summarized the function of VL8-0 setting.

Table 6-44

VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	Scrolling lines
0	0	0	0	0	0	0	0	0	0 line
0	0	0	0	0	0	0	0	1	1 line
0	0	0	0	0	0	0	1	0	2 lines
	:	:	:	:	:	:	:	:	:
1	1	0	1	0	1	1	1	0	431 lines
1	1	0	1	0	1	1	1	1	432 lines

Note: VL8-0 bits cannot set more than 432 lines.

6.2.40. Display Position - Partial Display 1 (R500h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTD P08	PTD P07	PTD P06	PTD P05	PTD P04	PTD P03	PTD P02	PTD P01	PTD P00

See R505h.

6.2.41. RAM Address Start – Partial Display 1 (R501h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTS A08	PTS A07	PTS A06	PTS A05	PTS A04	PTS A03	PTS A02	PTS A01	PTS A00

See R505h.

6.2.42. RAM Address End – Partail Display 1 (R502h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTE A08	PTE A07	PTE A06	PTE A05	PTE A04	PTE A03	PTE A02	PTE A01	PTE A00

See R505h.

6.2.43. Display Position – Partial Display 2 (R503h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTD P18	PTD P17	PTD P16	PTD P15	PTD P14	PTD P13	PTD P12	PTD P11	PTD P10

See R505h.

6.2.44. RAM Address Start – Partial Display 2 (R504h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTSA18	PTSA17	PTSA16	PTSA15	PTSA14	PTSA13	PTSA12	PTSA11	PTSA10

See R505h.

6.2.45. RAM Address End – Partial Display 2 (R505h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTEA18	PTEA17	PTEA16	PTEA15	PTEA14	PTEA13	PTEA12	PTEA11	PTEA10

PTDP0[8:0]: Set the physical starting position of partial display 1 on the LCD panel

PTDP1[8:0]: Set the physical starting position of partial display 2 on the LCD panel

The partial display 1 and partial display 2 should not overlap with each other. And make sure the PTDP0[8:0] < PTDP1[8:0].

PTSA0[8:0]: Set the start line address of display RAM of partial display 1 which will be display according to PTDP0[8:0].

PTEA0[8:0]: Set the end line address of display RAM of partial display 1 which will be display according to PTDP0[8:0].

Make sure PTSA0≤PTEA0.

PTSA1[8:0]: Set the start line address of display RAM of partial display2 which will be display according to PTDP1[8:0].

PTEA1[8:0]: Set the end line address of display RAM of partial display2 which will be display according to PTDP1[8:0]

Make sure PTSA1≤PTEA1.

6.2.46. Pin Control (R606h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	TCREV1(0)	0	0	0	0	0	0	0	TCREV0(0)

TCREV1-0: Set the order of receiving data when using i80 interface.

TCREV1-0	2 Transfers/Pixel	3 Transfers/Pixel
00	1st to 2nd	1st to 3rd
01 – 10	Setting Disabled	
11	2nd to 1st	3rd to 1st

Note 1: During read operation, the setting of TCREV is ignored; data is transferred from 1st to 2nd/1st to 3rd.

Note 2: Reset TCREV after reset and power-on.

6.2.47. NVM Access Control (R6F0h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	TE	0	EOP1 (0)	EOP0 (0)	0	0	EAD1 (0)	EAD0 (0)

EDA1 – 0: Determine the address of the NVM.

EAD1 – 0	Data written into NVM
00	UID(3 – 0)
01	VCM1(4 – 0)
10	VCMSEL, VCM2(4 – 0)
11	Setting Disabled

EOP: EOP = 00: Halt the write operation; EOP = 01: Enable the write operation.

TE: TE = 1, Enable the NVM control sequence.

7. GRAM

Table 7-1 GRAM address and display panel position (SS = "0")

S/G pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	....	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	DB17-0			DB17-0			DB17-0			DB17-0			....	DB17-0			DB17-0			DB17-0			DB17-0		
G1	G400	"00000"H			"00001"H			"00002"H			"00003"H			....	"000EC"H			"000ED"H			"000EE"H			"000EF"H		
G2	G399	"00100"H			"00101"H			"00102"H			"00103"H			....	"001EC"H			"001ED"H			"001EE"H			"001EF"H		
G3	G398	"00200"H			"00201"H			"00202"H			"00203"H			....	"002EC"H			"002ED"H			"002EE"H			"002EF"H		
G4	G397	"00300"H			"00301"H			"00302"H			"00303"H			....	"003EC"H			"003ED"H			"003EE"H			"003EF"H		
G5	G396	"00400"H			"00401"H			"00402"H			"00403"H			....	"004EC"H			"004ED"H			"004EE"H			"004EF"H		
G6	G395	"00500"H			"00501"H			"00502"H			"00503"H			....	"005EC"H			"005ED"H			"005EE"H			"005EF"H		
G7	G394	"00600"H			"00601"H			"00602"H			"00603"H			....	"006EC"H			"06ED"H			"06EE"H			"06EF"H		
G8	G393	"00700"H			"00701"H			"00702"H			"00703"H			....	"007EC"H			"007ED"H			"007EE"H			"007EF"H		
G9	G392	"00800"H			"00801"H			"00802"H			"00803"H			....	"008EC"H			"008ED"H			"008EE"H			"008EF"H		
G10	G391	"00900"H			"00901"H			"00902"H			"00903"H			....	"009EC"H			"009ED"H			"009EE"H			"009EF"H		
G11	G390	"00E00"H			"00E01"H			"00E02"H			"00E03"H			....	"00EEC"H			"00EED"H			"00EEE"H			"00EEF"H		
G12	G389	"00B00"H			"00B01"H			"00B02"H			"00B03"H			....	"00BEC"H			"00BED"H			"00BEE"H			"00BEF"H		
G13	G388	"00C00"H			"00C01"H			"00C02"H			"00C03"H			....	"00CEC"H			"00CED"H			"00CEE"H			"00CEF"H		
G14	G387	"00D00"H			"00D01"H			"00D02"H			"00D03"H			....	"00DEC"H			"00DED"H			"00DEE"H			"00DEF"H		
G15	G386	"00E00"H			"00E01"H			"00E02"H			"00E03"H			....	"00EEC"H			"00EED"H			"00EEE"H			"00EEF"H		
G16	G385	"00F00"H			"00F01"H			"00F02"H			"00F03"H			....	"00FEC"H			"00FED"H			"00FEE"H			"00FEF"H		
G17	G384	"01000"H			"01001"H			"01002"H			"01003"H			....	"010EC"H			"010ED"H			"010EE"H			"010EF"H		
G18	G383	"01100"H			"01101"H			"01102"H			"01103"H			....	"011EC"H			"011ED"H			"011EE"H			"011EF"H		
G19	G382	"01200"H			"01201"H			"01202"H			"01203"H			....	"012EC"H			"012ED"H			"012EE"H			"012EF"H		
G20	G381	"01300"H			"01301"H			"01302"H			"01303"H			....	"013EC"H			"013ED"H			"013EE"H			"013EF"H		
:	:	:			:			:			:				:			:			:			:		
:	:	:			:			:			:				:			:			:			:		
G393	G8	"1A900"H			"1A801"H			"1A802"H			"1A803"H			....	"1A8EC"H			"1A8ED"H			"1A8EE"H			"1A8EF"H		
G394	G7	"1AA00"H			"1A901"H			"1A902"H			"1A903"H			....	"1A9EC"H			"1A9ED"H			"1A9EE"H			"1A9EF"H		
G395	G6	"1AB00"H			"1AA01"H			"1AA02"H			"1AA03"H			....	"1AAEC"H			"1AAED"H			"1AAEE"H			"1AAEF"H		
G396	G5	"1AC00"H			"1AB01"H			"1AB02"H			"1AB03"H			....	"1ABEC"H			"1ABED"H			"1ABEE"H			"1ABEF"H		
G397	G4	"1AD00"H			"1AC01"H			"1AC02"H			"1AC03"H			....	"1ACEC"H			"1ACED"H			"1ACEE"H			"1ACEF"H		
G398	G3	"1AD00"H			"1AD01"H			"1AD02"H			"1AD03"H			....	"1ADEC"H			"1ADED"H			"1ADEE"H			"1ADEF"H		
G399	G2	"1AE00"H			"1AE01"H			"1AE02"H			"1AE03"H			....	"1AEEC"H			"1AEED"H			"1AEEE"H			"1AEEF"H		
G400	G1	"1AF00"H			"1AF01"H			"1AF02"H			"1AF03"H			....	"1AFEC"H			"1AFED"H			"1AFEE"H			"1AFEF"H		

Table 7-2 GRAM address and display panel position (SS = "1")

S/G pin		S1	S2	S3	S4	S5	…	S7	S8	S9	S10	S11	S12	….	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	DB17-0			DB17-0			DB17-0			DB17-0			….	DB17-0			DB17-0			DB17-0			DB17-0		
G1	G432	"000EF"H			"000EE"H			"000ED"H			"000EC"H			….	"00003"H			"00002"H			"00001"H			"00000"H		
G2	G431	"001EF"H			"001EE"H			"001ED"H			"001EC"H			….	"00103"H			"00102"H			"00101"H			"00100"H		
G3	G430	"002EF"H			"002AE"H			"002ED"H			"002EC"H			….	"00203"H			"00202"H			"00201"H			"00200"H		
G4	G429	"003EF"H			"003EE"H			"003ED"H			"003EC"H			….	"00303"H			"00302"H			"00301"H			"00300"H		
G5	G428	"004EF"H			"004EE"H			"004ED"H			"004EC"H			….	"00403"H			"00402"H			"00401"H			"00400"H		
G6	G427	"005EF"H			"005EE"H			"005ED"H			"005EC"H			….	"00503"H			"00502"H			"00501"H			"00500"H		
G7	G426	"006EF"H			"006EE"H			"006ED"H			"006EC"H			….	"00603"H			"00602"H			"00601"H			"00600"H		
G8	G425	"007EF"H			"007EE"H			"007ED"H			"007EC"H			….	"00703"H			"00702"H			"00701"H			"00700"H		
G9	G424	"008EF"H			"008EE"H			"008ED"H			"008EC"H			….	"00803"H			"00802"H			"00801"H			"00800"H		
G10	G423	"009EF"H			"009EE"H			"009ED"H			"009EC"H			….	"00903"H			"00902"H			"00901"H			"00900"H		
G11	G422	"00AEF"H			"00AEE"H			"00AED"H			"00AEC"H			….	"00E03"H			"00A02"H			"00A01"H			"00A00"H		
G12	G421	"00BEF"H			"00BEE"H			"00BED"H			"00BEC"H			….	"00B03"H			"00B02"H			"00B01"H			"00B00"H		
G13	G420	"00CEF"H			"00CEE"H			"00CED"H			"00CEC"H			….	"00C03"H			"00C02"H			"00C01"H			"00C00"H		
G14	G419	"00DEF"H			"00DEE"H			"00DED"H			"00DEC"H			….	"00D03"H			"00D02"H			"00D01"H			"00D00"H		
G15	G418	"00EEF"H			"00EEE"H			"00EED"H			"00EEC"H			….	"00E03"H			"00E02"H			"00E01"H			"00E00"H		
G16	G417	"00FEF"H			"00FEE"H			"00FED"H			"00FEC"H			….	"00F03"H			"00F02"H			"00F01"H			"00F00"H		
G17	G416	"010EF"H			"010EE"H			"010ED"H			"010EC"H			….	"01003"H			"01002"H			"01001"H			"01000"H		
G18	G415	"011EF"H			"011EE"H			"011ED"H			"011EC"H			….	"01103"H			"01102"H			"01101"H			"01100"H		
G19	G414	"012EF"H			"012EE"H			"012ED"H			"012EC"H			….	"01203"H			"01202"H			"01201"H			"01200"H		
G20	G413	"013EF"H			"013EE"H			"013ED"H			"013EC"H			….	"01303"H			"01302"H			"01301"H			"01300"H		
:	:	:			:			:			:				:			:			:			:		
:	:	:			:			:			:				:			:			:			:		
G425	G8	"1A8EF"H			"1A8EE"H			"1A8ED"H			"1A8EC"H			….	"1A803"H			"1A802"H			"1A801"H			"1A900"H		
G426	G7	"1A9EF"H			"1A9EE"H			"1A9ED"H			"1A9EC"H			….	"1A903"H			"1A902"H			"1A901"H			"1AA00"H		
G427	G6	"1AAEF"H			"1AAEE"H			"1AAED"H			"1AAEC"H			….	"1AA03"H			"1AA02"H			"1AA01"H			"1AB00"H		
G428	G5	"1ABEF"H			"1ABEE"H			"1ABED"H			"1ABEC"H			….	"1AB03"H			"1AB02"H			"1AB01"H			"1AC00"H		
G429	G4	"1ACEF"H			"1ACEE"H			"1ACED"H			"1ACEC"H			….	"1AC03"H			"1AC02"H			"1AC01"H			"1AD00"H		
G430	G3	"1ADEF"H			"1ADEE"H			"1ADED"H			"1ADEC"H			….	"1AD03"H			"1AD02"H			"1AD01"H			"1AD00"H		
G431	G2	"1AEEF"H			"1AEEE"H			"1AEED"H			"1AEEC"H			….	"1AE03"H			"1AE02"H			"1AE01"H			"1AE00"H		
G432	G1	"1AFEF"H			"1AFEE"H			"1AFED"H			"1AFEC"H			….	"1AF03"H			"1AF02"H			"1AF01"H			"1AF00"H		

8. INTERFACES

The SPFD5420A provides different interfaces to meet the diverse need of small/medium size LCD. Based on the application requirement, there are three different display modes which are most used in end product.

1. Still picture display
2. Moving picture display.
3. Re-writing still pictures while moving picture are display.

For above three different display requirements, SPFD5420A provides different interfaces to meet the requirement.

1. System interface
2. External interface (RGB interface)
3. VSYNC interface

System interface is suitable for still picture display while RGB interface and VSYNC interface are suitable for moving picture display. Be aware that RGB or VSYNC interface still can used to display still picture and system interface can also display moving picture. **Table 8-1** summarized different interfaces for different display requirement.

Table 8-1

Operation Mode	Display Mode	RAM Access Setting (RM)	Display Operation Mode (DM1-0)
System	Still picture	System interface (RM = 0)	Internal operating clock (DM1-0 = 00)
RGB interface (1)	Moving picture	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
RGB interface (2)	Rewriting still pictures while displaying moving pictures	System interface (RM = 0)	RGB interface (DM1-0 = 01)
VSYNC interface	Moving pictures	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)

8.1. System Interface

The system interfaces of SPFD5420A can support 8-bit, 9-bit, 16-bit, 18-bit 80-system Interface and Serial Peripheral Interface (SPI), which can be set by the IM2/1/0 pins. The system interface can set instructions and access RAM. **Table 8-2** summarized the interface corresponding to IM2-0 setting.

Table 8-2

IM2	IM1	IM0	MPU-Interface Mode	DB Pin in use
0	0	0	80-system 18-bit interface	DB17 to 0
0	0	1	80-system 9-bit interface	DB17 to 9
0	1	0	80-system 16-bit interface	DB17 to 10 and 8 to 1
0	1	1	80-system 8-bit interface	DB17 to 10
1	0	*	Serial peripheral interface (SPI)	DB1 to 0
1	1	0	Setting disabled	-
1	1	1	Setting disabled	-

8.1.1. 80-system 18-bit interface

The instruction and GRAM accessing format of 80-system 18-bit interface are shown in **Figure 8-1** and **Figure 8-2**, respectively.

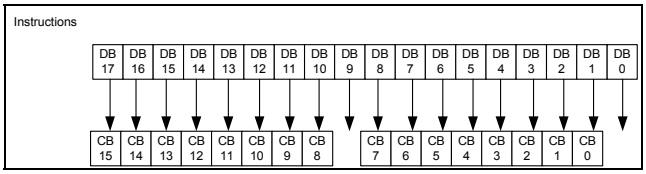


Figure 8-1

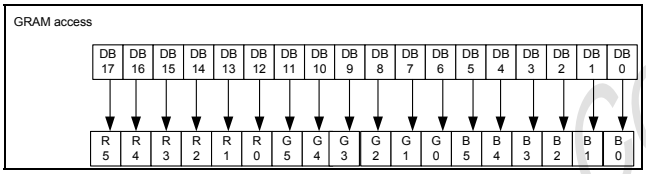


Figure 8-2

8.1.2. 80-system 16-bit interface

The instruction and GRAM accessing format of 80-system 16-bit interface are shown in **Figure 8-3** and **Figure 8-4**, respectively.

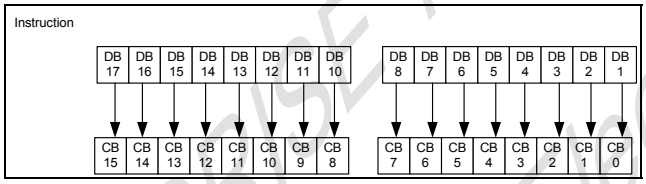


Figure 8-3

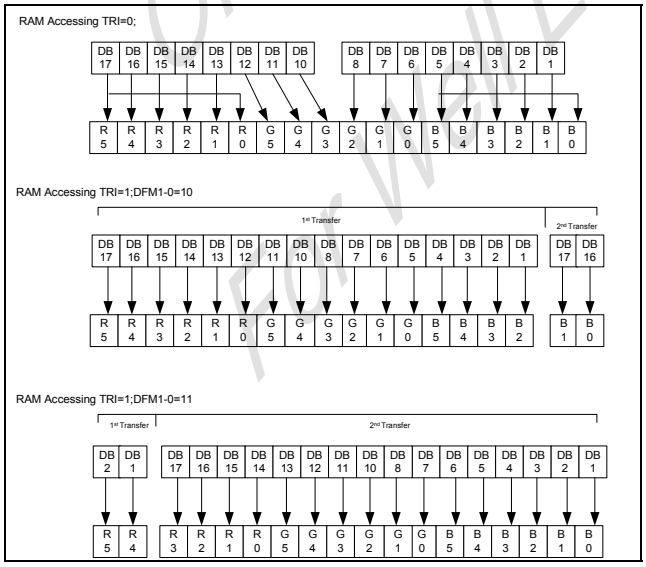


Figure 8-4

8.1.3. 80-system 9-bit interface

The instruction and GRAM accessing format of 80-system 9-bit interface are shown in **Figure 8-5** and **Figure 8-6**, respectively.

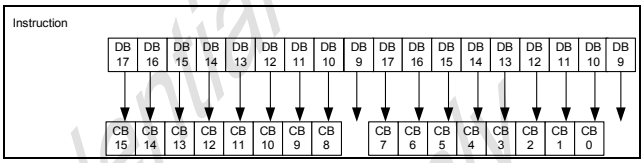


Figure 8-5

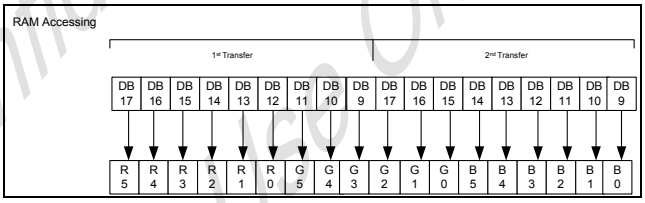


Figure 8-6

8.1.4. 80-system 8-bit interface

The instruction and GRAM accessing format of 80-system 8-bit interface are shown in **Figure 8-7** and **Figure 8-8**, respectively.

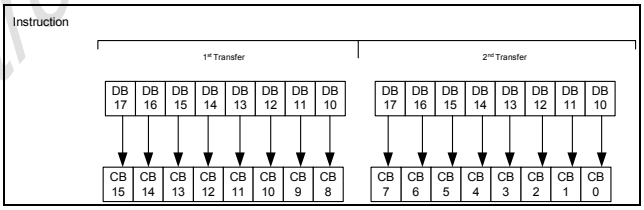


Figure 8-7

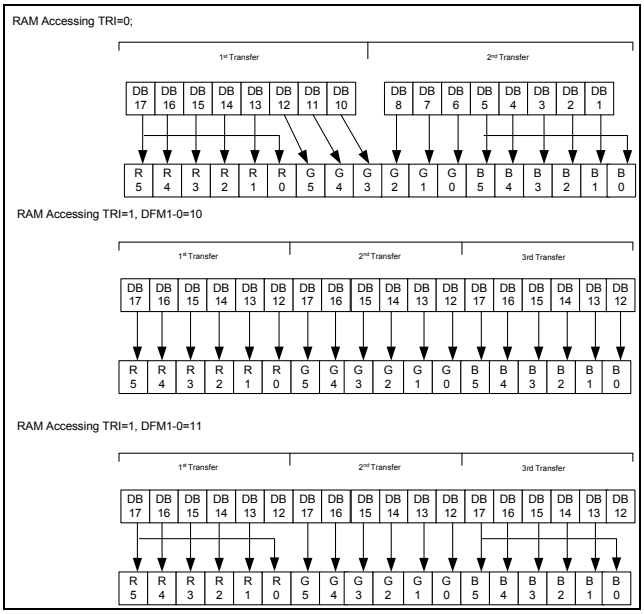


Figure 8-8

8.1.5. Serial Peripheral interface (SPI)

The system interface of SPFD5420A also includes the Serial Peripheral Interface (SPI). In SPI mode, /CS, SCL, SDI and SDO are used to transfer data between MCU and SPFD5420A. IM0/ID pin served as the ID pin. **Figure 8-9** illustrates the detail timing while using SPI. Be aware that the unused pins such as DB17-0 pins must be fixed at either IOVCC or GND level.

The instruction and GRAM accessing format of SPI interface are shown in **Figure 8-10** and **Figure 8-11**, respectively.

When read operation is desired In SPI mode, valid data are read out as the SPFD5420A reads out the 6th byte data from the internal GRAM. The RAM data transfer in SPI mode, in SPI mode with TRI=1/ DFM1-0=10 and status read are illustrated in **Figure 8-12**, **Figure 8-13** and **Figure 8-14**, respectively.

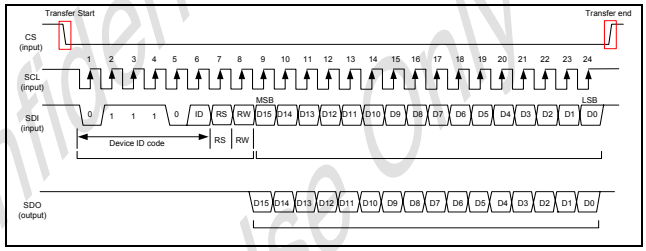


Figure 8-9

Start Byte Format

Transferred bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note 1) ID bit is selected by setting the IM0/ID pin.

RS	R/W	Function
0	0	Set an index register
0	1	Read a status
1	0	Write an instruction or RAM data
1	1	Read an instruction or RAM data

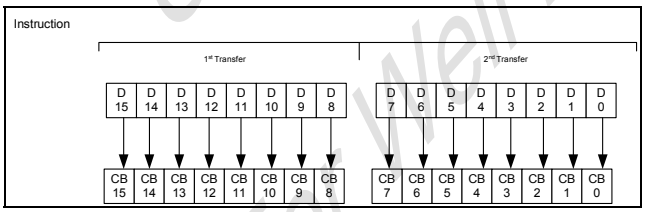


Figure 8-10

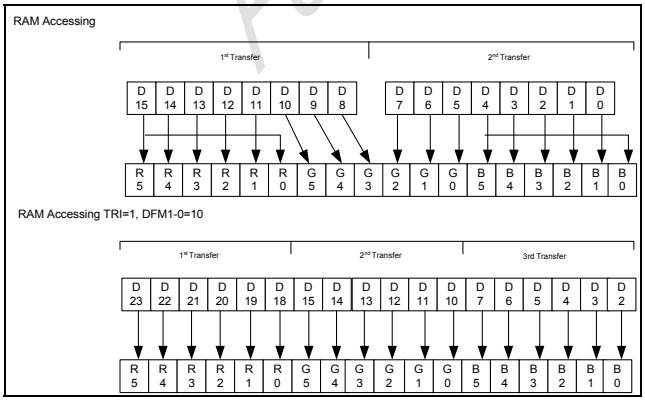


Figure 8-11

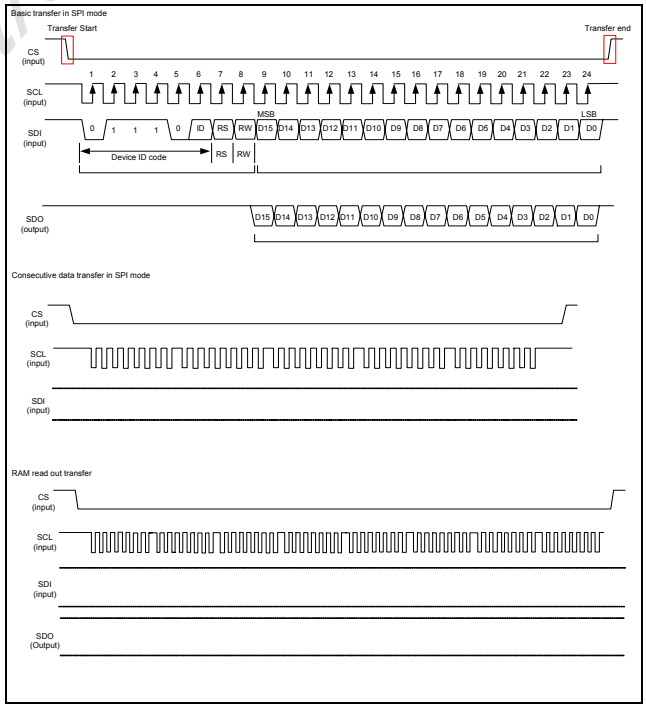


Figure 8-12

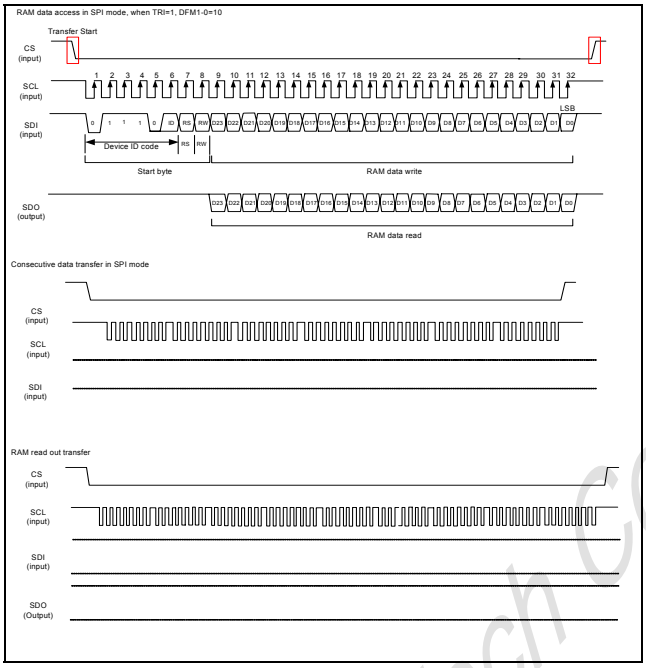


Figure 8-13

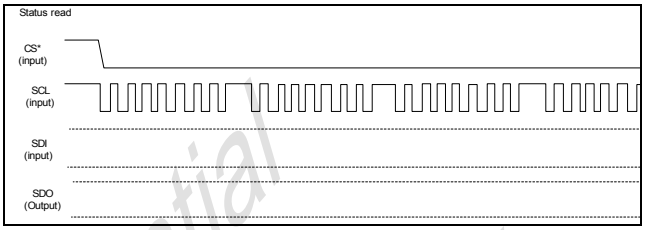


Figure 8-14

8.2. VSYNC Interface

The SPFD5420A also supports VSYNC interface for moving picture display, which is the system interface in synchronization with the frame-synchronizing signal (VSYNC). The VSYNC interface can display a moving picture without tremendous modification.

DM1-0 = “10” and RM = “0” can initialized VSYNC interface. In VSYNC interface mode, the internal display operation is synchronized with the VSYNC signal. In VSYNC interface mode, the graphic data are stored in GRAM to minimize the data transfer to overwrite on the moving picture GRAM area. **Figure 8-15** illustrates moving picture data transfer through VSYNC interface.

In VSYNC mode, Internal operation is executed in synchronization with the internal clock generated from internal oscillators and VSYNC input. Therefore the frame rate is determined by the frequency of VSYNC. SPFD5420A can access the internal RAM in high speed with less power consumption in VSYNC interface mode while using high-speed write mode

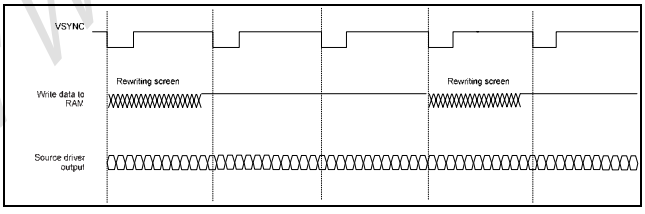


Figure 8-15

In VSYNC interface mode, the formula for Internal clock frequency and frame rate is shown below:

Input clock frequency = FrameRate x (DisplayLines + FrontPorch + BackPorch) x 16 x variance

Due to the possible cause of variances while set the internal clock frequency; be sure to complete the display operation in one VSYNC cycle.

8.3. External Display Interface

SPFD5420A also includes external (RGB) interface for displaying moving picture. External interface can be set by RIM1-0 bit. **Table 8-3** summarized the corresponding types of RGB interface with RM1-0 setting.

Table 8-3

RIM1	RIM0	RGB Interface	DB Pin
0	0	18-bit RGB interface	DB17-0
0	1	16-bit RGB interface	DB17-13, 11-1
1	0	6-bit RGB interface	DB17-12
1	1	Setting disabled	

RGB interface cab access SPFD5420A by VSYNC, HSYNC, ENABLE, DOTCLK and DB17-0 signals, where VSYNC is used for frame synchronization; HSYNC is used for line synchronization and ENABLE is served as the valid data synchronized signals. The RGB interface can be rewriting minimum necessary data to the GRAM area which need to be overwritten with use of window address function and high-speed write mode. It is necessary for RGB interface to set front and back porch periods after and before a display period, respectively. **Figure 8-16** illustrates the general timing for RGB interface. There are some constrain while using RGB interface. The following summarized the conditions,

(a) Partial display/ scroll function / interlace and graphics operation function are not available for RGB interface.

(b) In RGB interface VSYNC, HSYNC, and DOTCLK signals must be input through a display operation period.

(c) The setting of the NO1-0 bits, STD1-0 bits and EQ1-0 bits are based on DOTCLK in RGB interface mode. In 6-bit RGB interface mode, it takes 3 DOTCLK inputs to transfer one pixel. Be aware data transfer in units of 3 DOTCLK inputs in 6-bit RGB interface mode is necessary. Set the cycle of each signal in 6-bit interface mode (VSYNC, HSYNC ENABLE, DB17-0) to input 3x clock to complete data transfer in units of pixels.

(d) In RGB-I/F mode, while writing data to the internal RAM make sure to use the high-speed write mode (HWM = “1”)

(e) In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.

(f) In RGB interface mode, a GRAM address (DB17-0) is set in the address counter every frame on the falling edge of VSYNC.

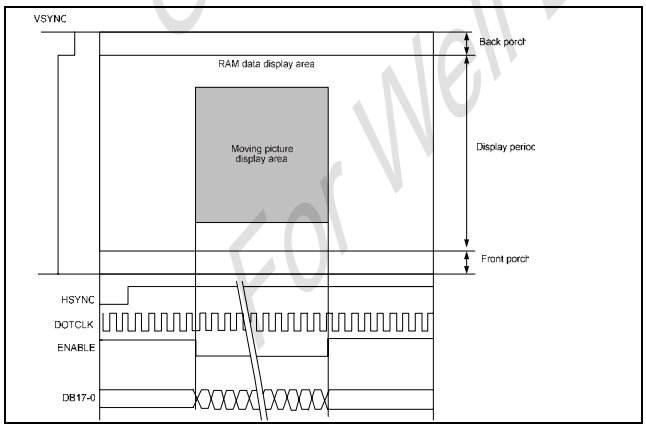


Figure 8-16

RGB interface includes ENABLE signal served as valid data synchronized signals. Moreover, the active level for ENABLE can be set by EPL. The EPL bit inverts the polarity of ENABLE signal. **Table 8-4** summarized the setting of EPL and ENABLE active level for GRAM accessing. Setting both EPL and ENABLE bits to automatically update RAM address in the AC is necessary while writing data to the GRAM.

Table 8-4

EPL	ENABLE	RAM Write	RAM Address
0	0	Enabled	Updated
0	1	Disabled	Retained
1	0	Disabled	Retained
1	1	Enabled	Updated

SPFD5420A can support 18-bit, 16-bit and 6-bit RGB interface. The detail timing diagram for 18-bit, 16-bit and 6-bit RGB interfaces are shown in **Figure 8-17** and **Figure 8-18** respectively.

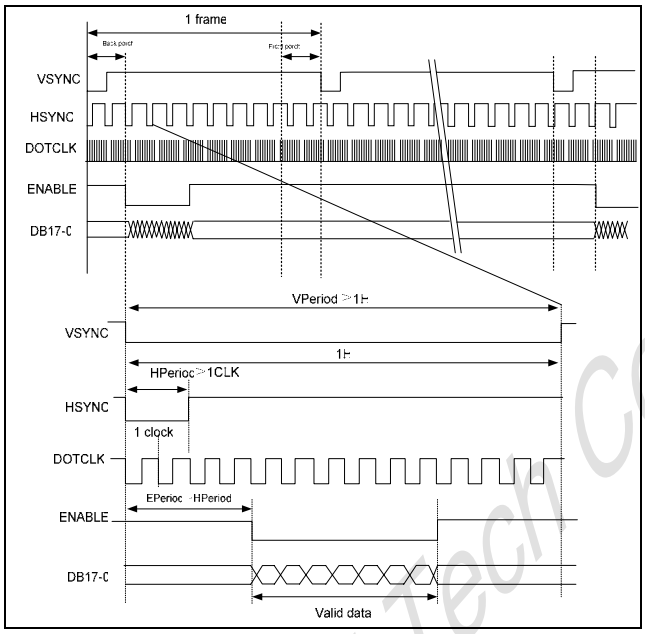


Figure 8-17

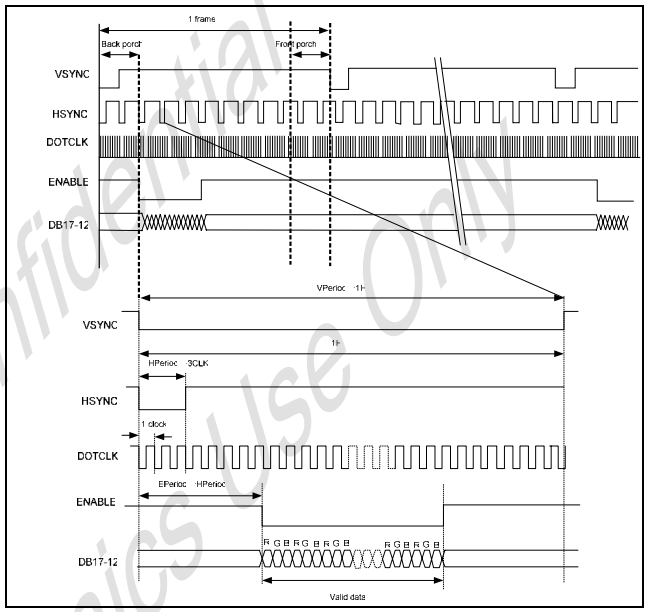


Figure 8-18

The RGB interface also has the window address function to transfer only minimum necessary data on the moving picture GRAM area, which can lower the power consumption and still can use system interface to rewrite data in still picture RAM area while displaying a moving picture. Setting RM = 0 while in RGB interface mode can make GRAM access CBIe through the system interface. When RGB interface accessing GRAM is desired, wait for one read/write bus cycle following by RM = 1 setting.

Figure 8-19 illustrates the timing diagram when displaying a moving picture through the RGB interface and rewriting data in the still picture GRAM area through the system interface.

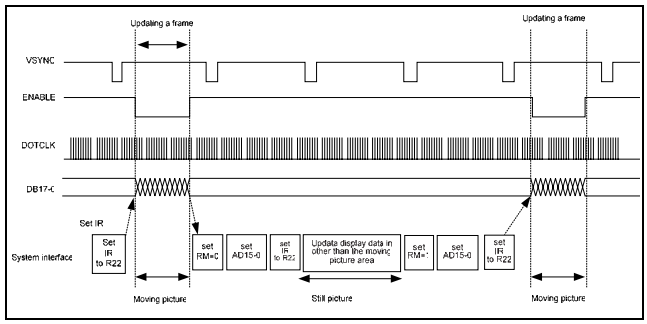


Figure 8-19

8.3.1. 6-bit RGB interface

RAM accessing format and data transmission synchronization of 6-bit RGB interface are shown in **Figure 8-20** and **Figure 8-21**, respectively.

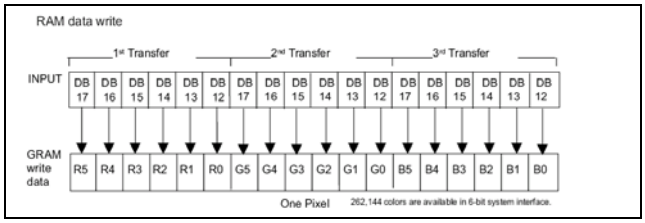


Figure 8-20

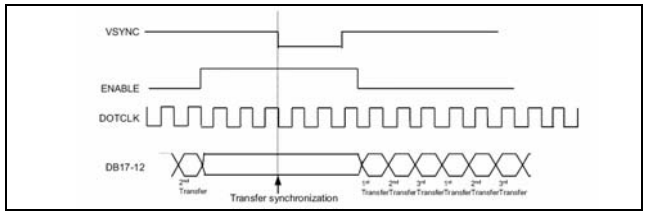


Figure 8-21

8.3.2. 16-bit RGB interface

RAM accessing format of 16-bit RGB interface are shown in **Figure 8-22**.

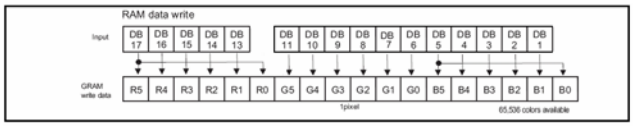


Figure 8-22

8.3.3. 18-bit RGB interface

RAM accessing format of 18-bit RGB interface are shown in **Figure 8-23**.

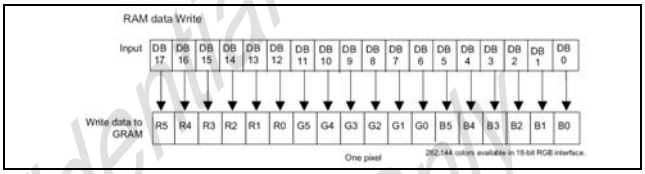


Figure 8-23

9. Display Feature Function:

9.1. FMARK function:

SPFD5420A provided FMARK function which output signal to alert host MCU via FMARK I/O pad so that LCD display can avoid flicker effect. FMARK output position and onterval can be set by FMP[8:0] and FMI[2:0], respectively.

Figure 9-1 illustrated the FMARK output position when FMP[8:0]=9'h008.

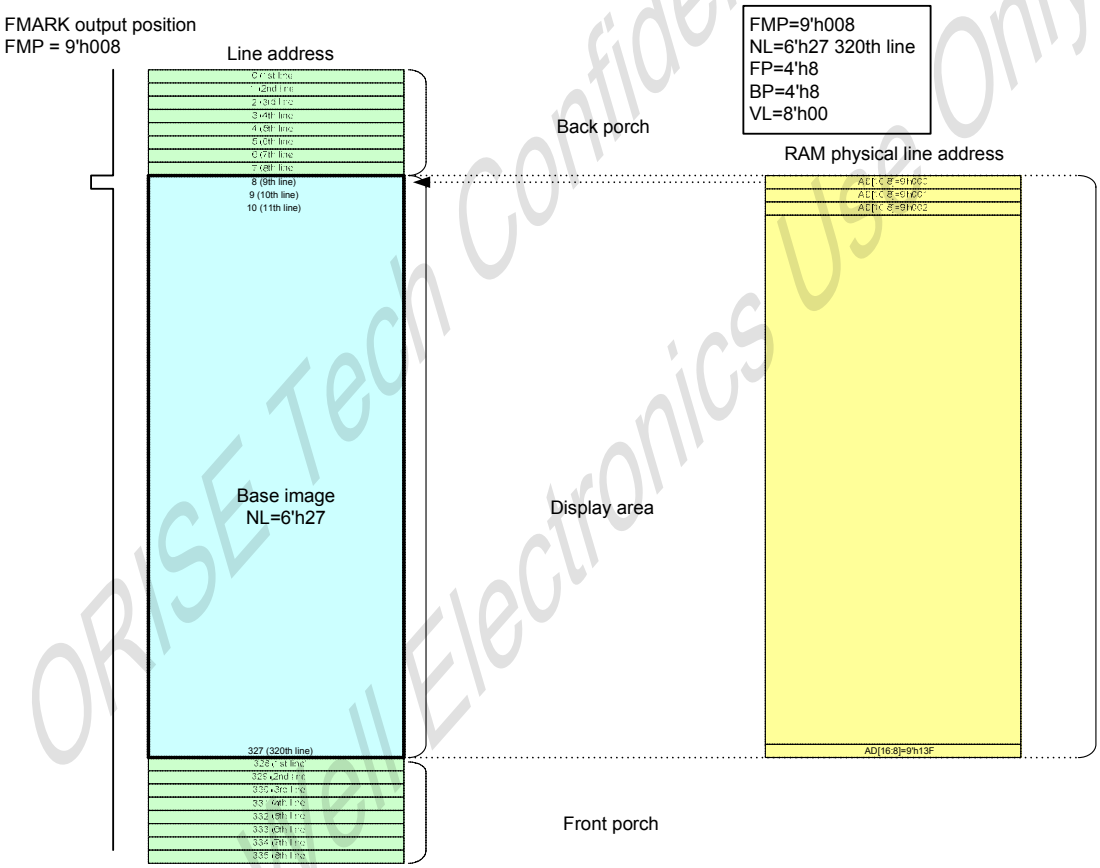
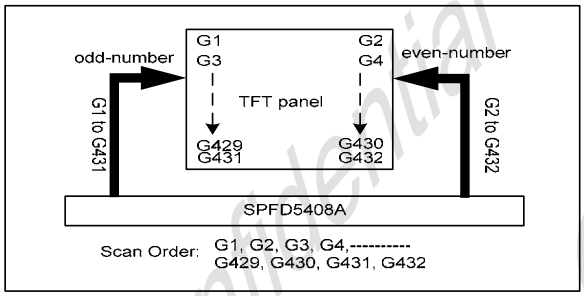
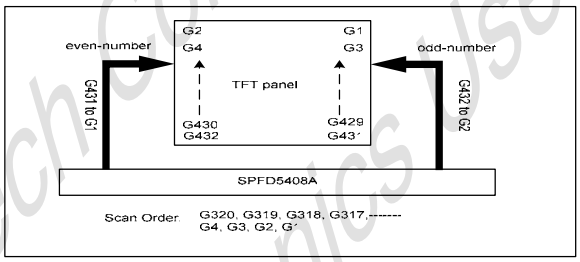
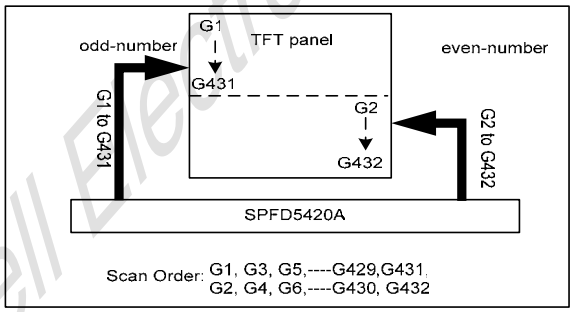
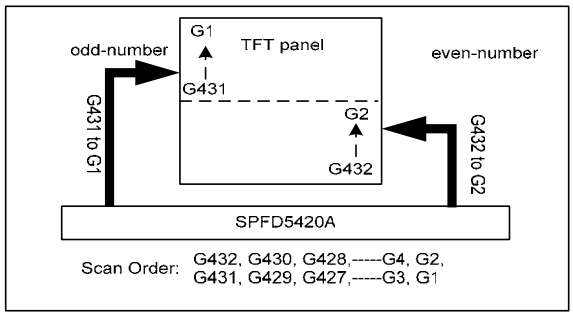


Figure 9-1 Example of FMARK signal.

9.2. Scan Mode function:

SM	GS	Scan Direction
0	0	
0	1	
1	0	
1	1	

9.3. Partial Display function:

SPFD5420A has partial display function feature which can provide only partial display for power saving purpose. Partial display function can be accessed by setting BSEE="0",. Moreover, 2 partial display area (partial image 1/ partial image 2) can be initialized by setted PTDE0="1" and PTDE1="1", respectively. The partial display area for partial image 1 and partial 2 can be set by PTSA0 / PTEA0 and PTSA1/ PTEA1, respectively. **Table 9-1** and **Figure 9-2** summarized the full and partial display function.

Table 9-1 Partial display function summary table

Case	Function Setting	Display area setting	Display Position
Full dsiplay	**BASEE="1" PTDE0="x" PTDE1="x"**	**(BSA,BEA)**	**-**
Partail image1:0n Partial image2:Off	**BASEE="0" PTDE0="1" PTDE1="0"**	**(PTSA0,PTEA0)**	**PTDP0**
Partail image1:Off Partial image2:On	**BASEE="0" PTDE0="0" PTDE1="1"**	**(PTSA1,PTEA1)**	**PTDP1**
Partail image1:On Partial image2:On	**BASEE="0" PTDE0="1" PTDE1="1"**	**(PTSA0,PTEA0) (PTSA1,PTEA1)**	**PTDP0 & PTDP1**

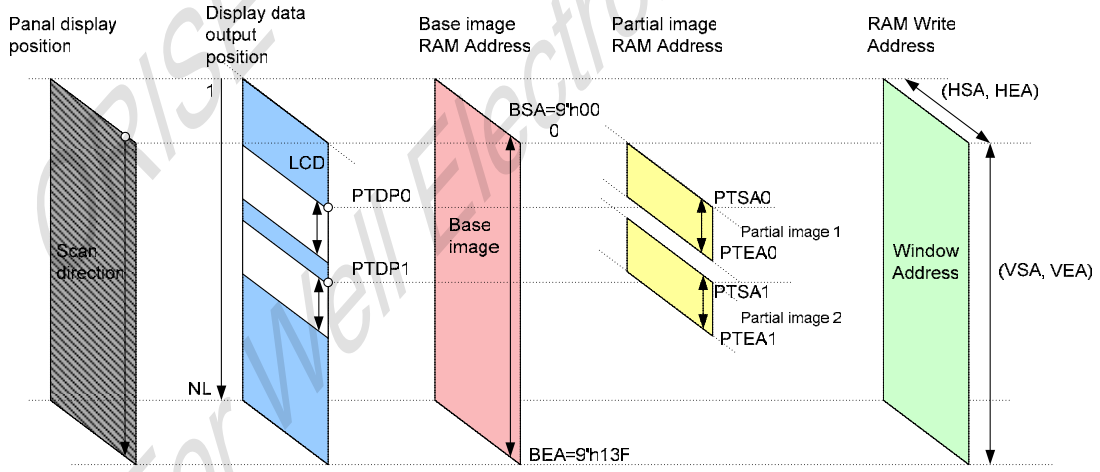


Figure 9-2 Partial display function diagram

Figure 9-3 indicated the case of NL[5:0] setting is < 6'h35 which active line is less than 432. Partial display image data can stored in not active area.

Figure 9-4 indicated the partial display area start position. The partial display area and start position can be set by (**PTSA0, PTEA0 , PTSA1, PTEA1) and (PTDP0, PTDP1).**

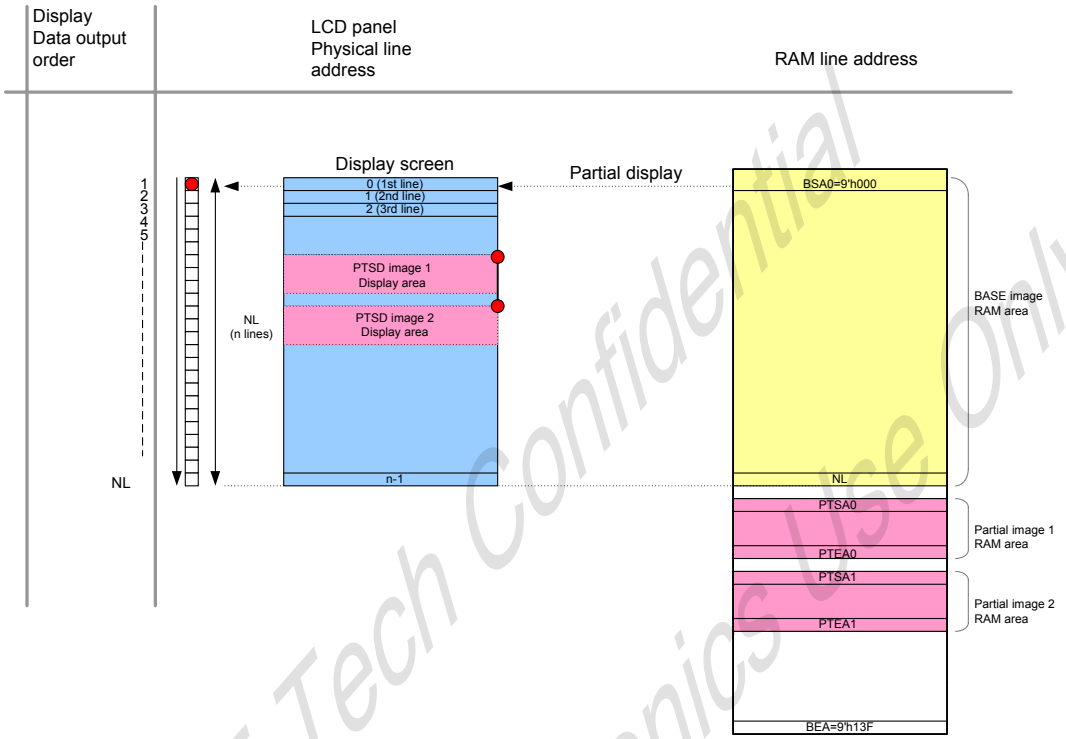


Figure 9-3 Example of NL[5:0] setting is < 6'h35 case

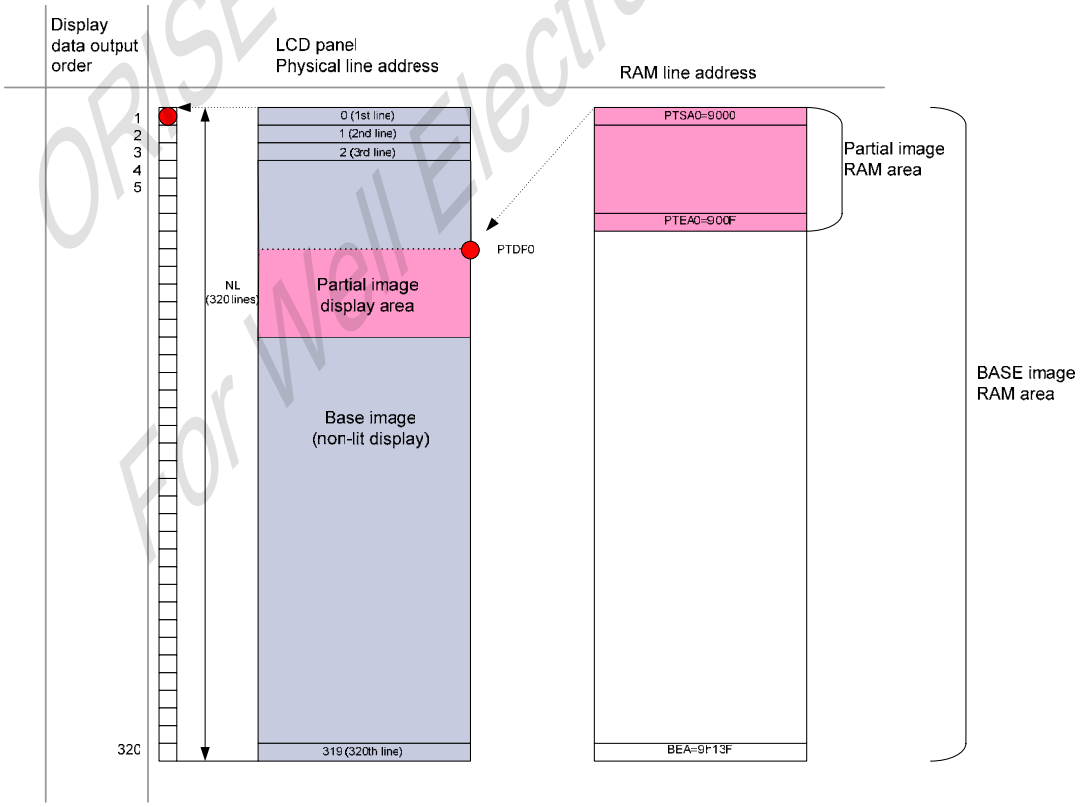


Figure 9-4 indicated the partial display area start position.

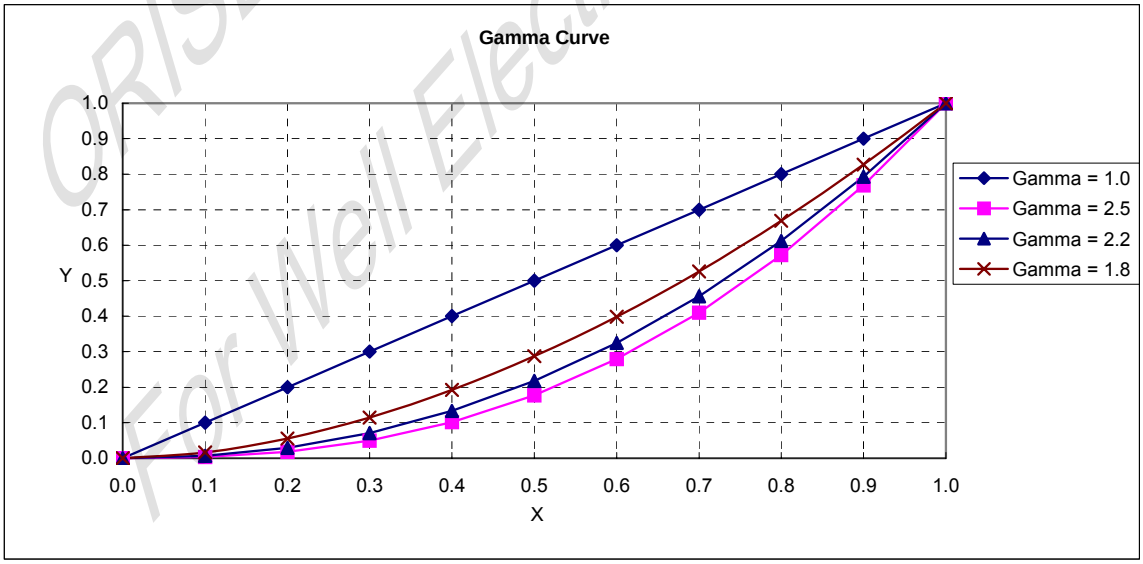
9.4. Gamma Correction functions:

SPFD5420A adopt Gamma voltage generation circuit which can provide wider output voltage range to fit the different kind of liquid crystal for Gamma curve from 1.0~2.5. The Gamma output voltage can be set by R300h~R3F0h.

V1RP[4:0]: register for positive VSD0 fine tune adjustment.
V2RP[5:0]: register for positive VSD1 fine tune adjustment.
V3RP[5:0]: register for positive VSD2 fine tune adjustment.
V4RP[5:0]: register for positive VSD61 fine tune adjustment.
V5RP[5:0]: register for positive VSD62 fine tune adjustment.
V6RP[4:0]: register for positive VSD63 fine tune adjustment
V7RP[4:0]: register for positive VSD13 fine tune adjustment
V8RP[4:0]: register for positive VSD50 fine tune adjustment
V9RP[3:0]: register for positive VSD4 fine tune adjustment
V10RP[3:0]: register for positive VSD8 fine tune adjustment
V11RP[3:0]: register for positive VSD20 fine tune adjustment
V12RP[3:0]: register for positive VSD27 fine tune adjustment
V13RP[3:0]: register for positive VSD36 fine tune adjustment
V14RP[3:0]: register for positive VSD43 fine tune adjustment
V15RP[3:0]: register for positive VSD55 fine tune adjustment
V16RP[3:0]: register for positive VSD59 fine tune adjustment

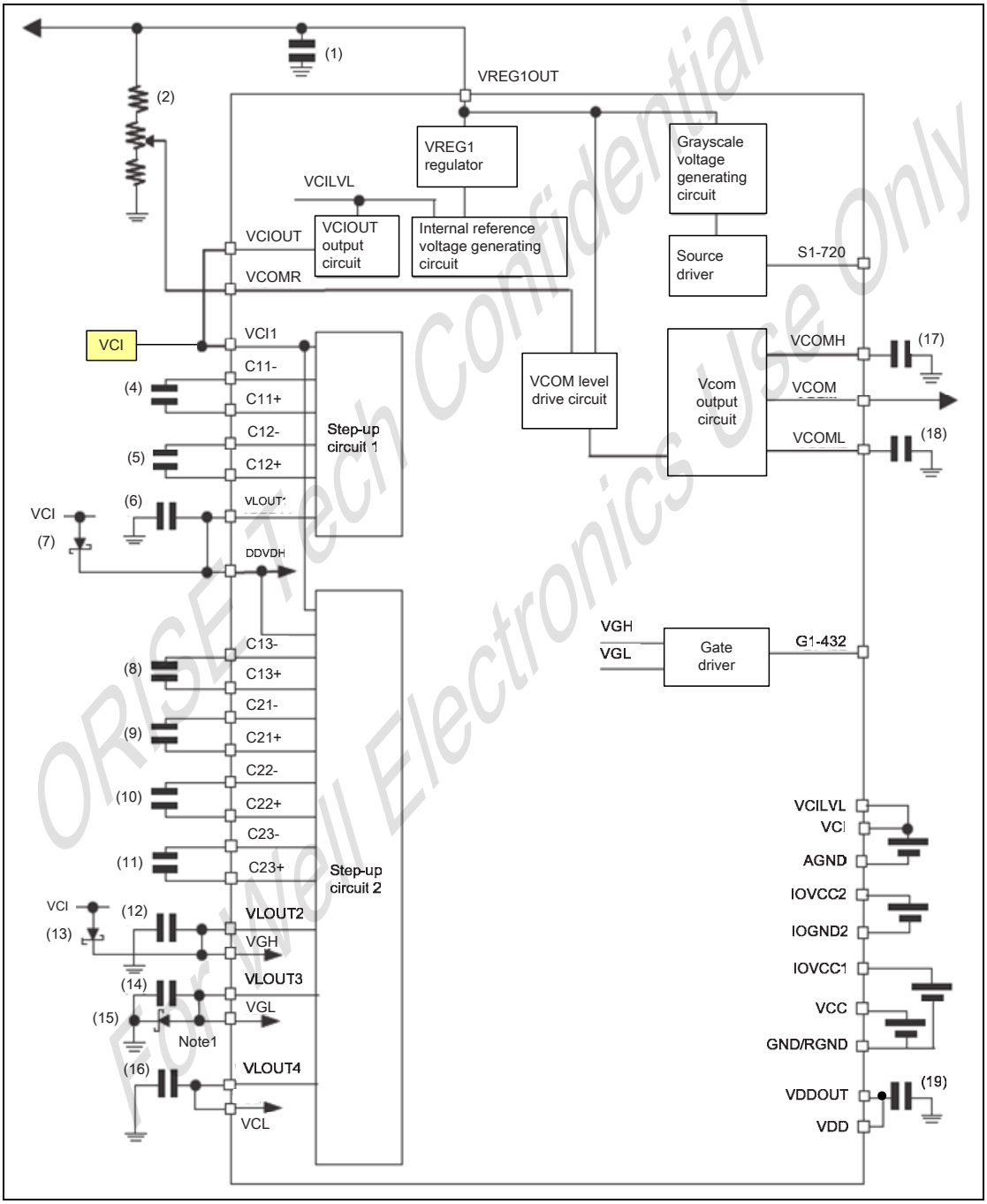
V1RN[4:0]: register for negative VSD0 fine tune adjustment.
V2RN[5:0]: register for negative VSD1 fine tune adjustment.
V3RN[5:0]: register for negative VSD2 fine tune adjustment.
V4RN[5:0]: register for negative VSD61 fine tune adjustment.
V5RN[5:0]: register for negative VSD62 fine tune adjustment.
V6RN[4:0]: register for negative VSD63 fine tune adjustment
V7RN[4:0]: register for negative VSD13 fine tune adjustment
V8RN[4:0]: register for negative VSD50 fine tune adjustment
V9RN[3:0]: register for negative VSD4 fine tune adjustment
V10RN[3:0]: register for negative VSD8 fine tune adjustment
V11RN[3:0]: register for negative VSD20 fine tune adjustment
V12RN[3:0]: register for negative VSD27 fine tune adjustment
V13RN[3:0]: register for negative VSD36 fine tune adjustment
V14RN[3:0]: register for negative VSD43 fine tune adjustment
V15RN[3:0]: register for negative VSD55 fine tune adjustment
V16RN[3:0]: register for negative VSD59 fine tune adjustment

Figure 9-5 illustrated 4 different Gamma Curve.

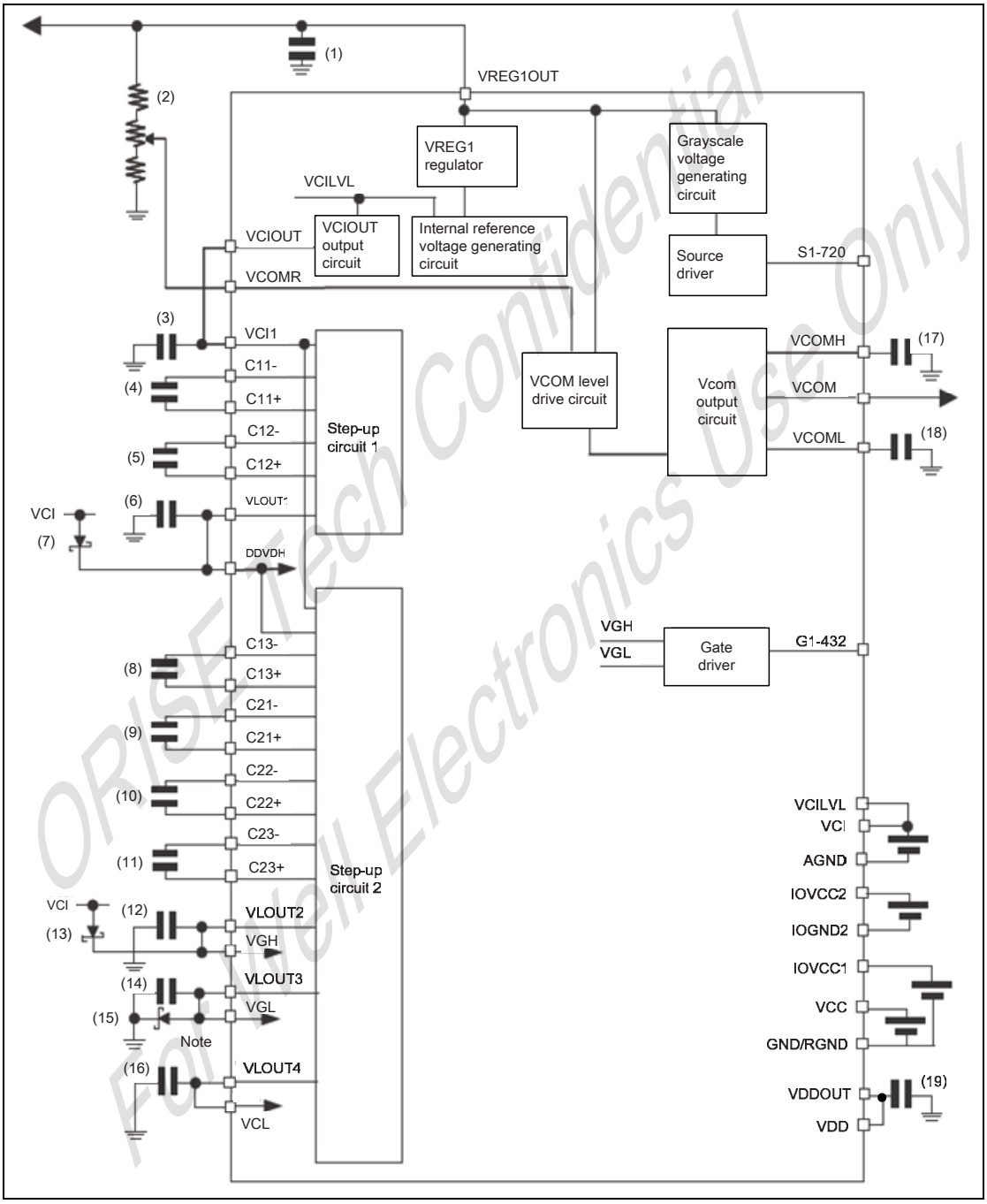


10. Power Management System:

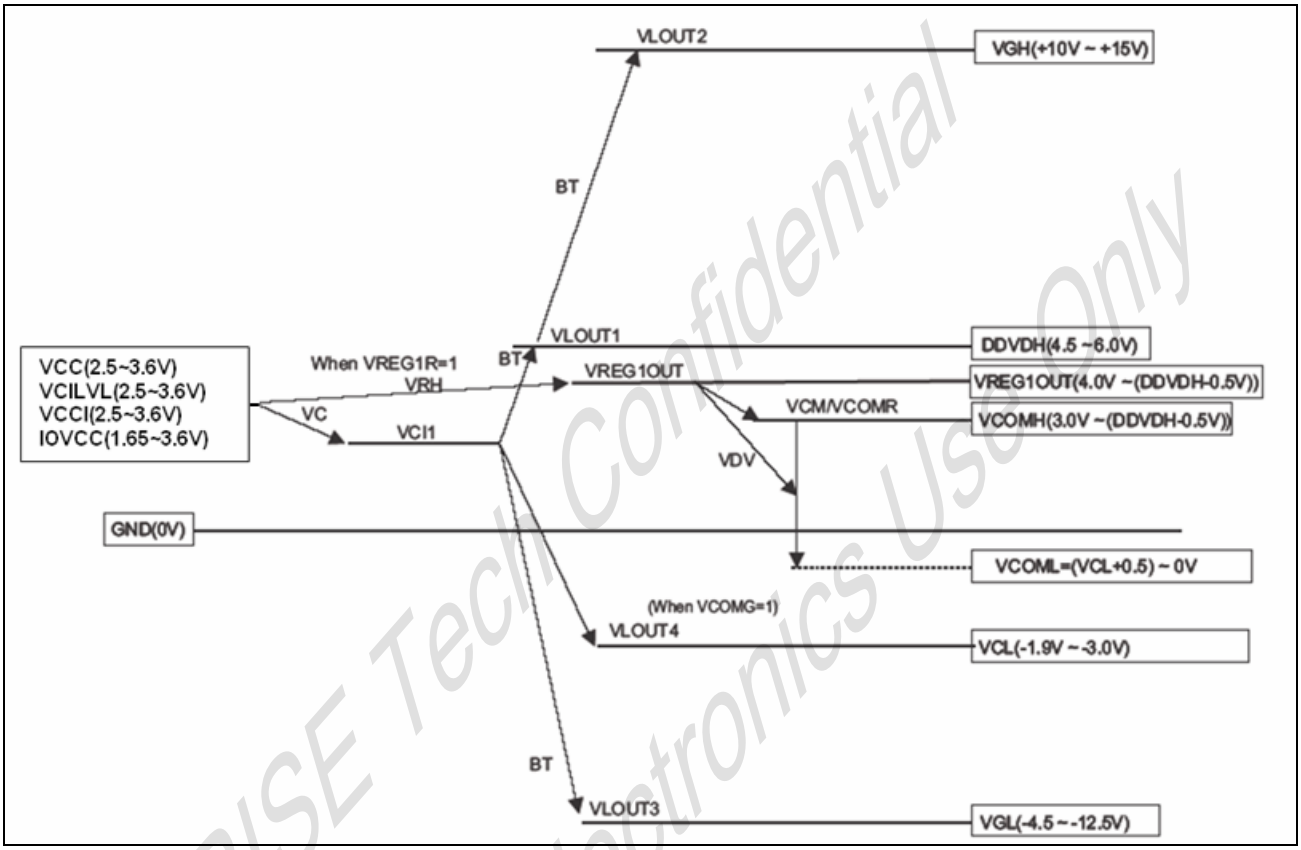
(a) VCI1=VCI direct input



(b) VCI1=VCIOUT

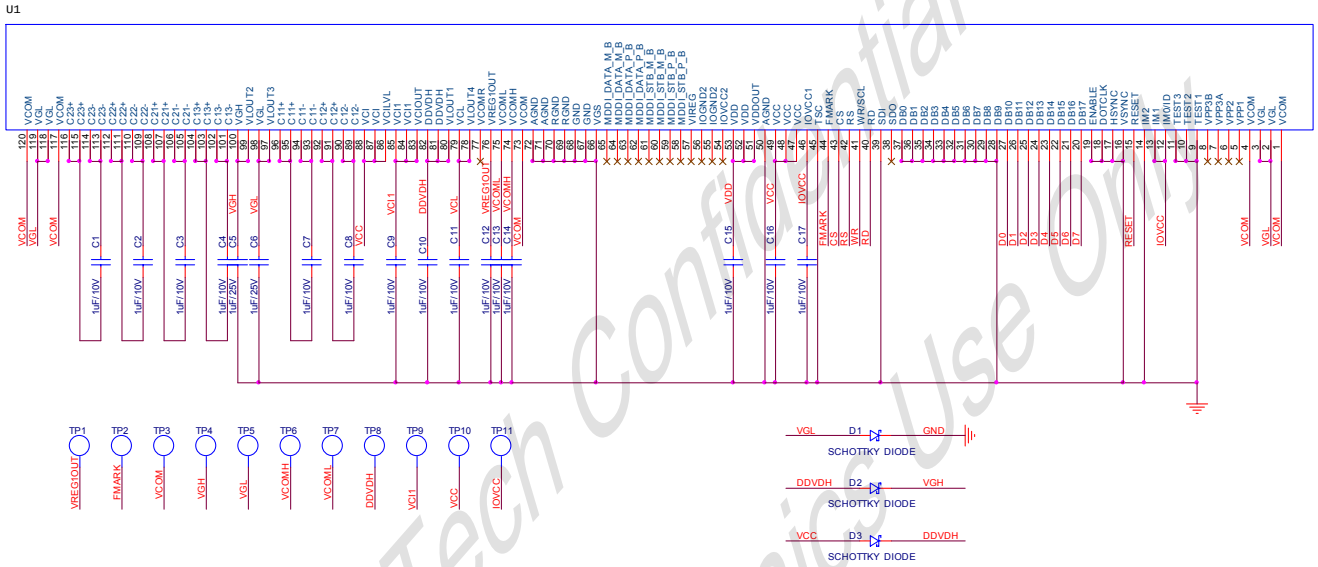


(**c) Voltage Generation Diagram**

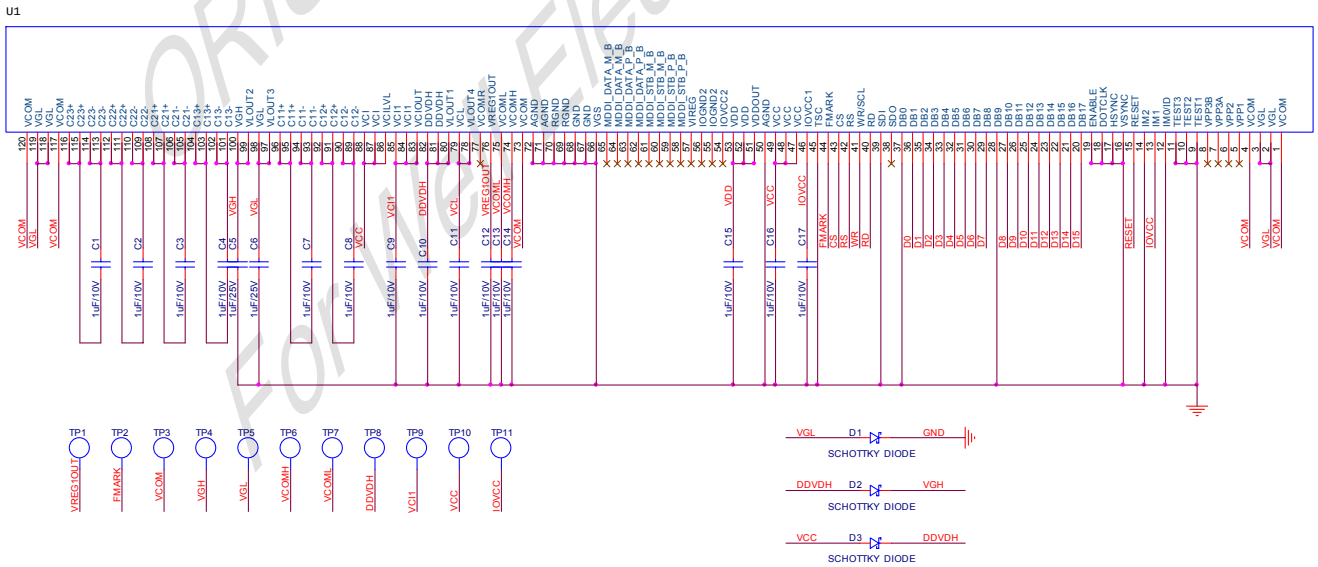


11. Application circuits :

CPU interface I80/8bit



CPU interface I80/16bit



12. Initial Code:

Step	Register Address	Register Value	Note	Step	Register Address	Register Value	Note
1	R0606h	0x0000		44	R0281h	0x000E	
2	Delay 10us			45	R0282h	0x0000	
3	R0007h	0x0001		46	R0300h	0x0101	
4	Delay 10us			47	R0301h	0x0B2C	
5	R0110h	0x0001		48	R0302h	0x1030	
6	Delay 10us			49	R0303h	0x3010	
7	R0100h	0x17B0		50	R0304h	0x2C0B	
8	R0101h	0x0147		51	R0305h	0x0101	
9	R0102h	0x019D		52	R0306h	0x0807	
10	R0103h	0x3600		53	R0307h	0x0708	
11	R0281h	0X0010		54	R0308h	0x0107	
12	Delay 10us			55	R0309h	0x0105	
13	R0102	0x01BD		56	R030Ah	0x0F04	
14	Delay10us			57	R030Bh	0x0F00	
14	R0000h	0x0000		58	R030Ch	0x000F	
15	R0001h	0x0000		59	R030Dh	0x040F	
16	R0002h	0x0100		60	R030Eh	0x0501	
17	R0003h	0xD0A0		61	R030Fh	0x0701	
18	R0006h	0x0000		62	R0400h	0x3500	
19	R0008h	0x0503		63	R0401h	0x0001	
20	R0009h	0x0001		64	R0404h	0x0000	
21	R000Bh	0x0010		65	R0500h	0x0000	
22	R000Ch	0x0000		66	R0501h	0x0000	
23	R000Fh	0x0000		67	R0502h	0x0000	
24	R0007h	0x0001		68	R0503h	0x0000	
25	R0010h	0x0013		69	R0504h	0x0000	
26	R0011h	0x0202		70	R0505h	0x0000	
27	R0012h	0x0300		71	R0600h	0x0000	
28	R0020h	0x021E		72	R0606h	0x0000	
29	R0021h	0x0202		73	R06F0h	0x0000	
30	R0022h	0x0100		74	R07F0h	0x5420	
31	R0090h	0x8000		75	R07F3h	0x288A	
32	R0092h	0x0000		76	R07F4h	0x0022	
33	R0100h	0x16B0		77	R07F5h	0x0041	
34	R0101h	0x0147		78	R07F0h	0x0000	
35	R0102h	0x01BD		79	R0007h	0x0173	
36	R0103h	0x2A00					
37	R0107h	0x0000					
38	R0110h	0x0001					
39	R0210h	0x0000					
40	R0211h	0x00EF					
41	R0212h	0x0000					
42	R0213h	0x018F					
43	R0280h	0x0000					

13. Electrical Characteristics:

13.1. Absolute Maximum Ratings:

Table 13-1

Item	Symbol	Unit	Value	Note
Power Supply Voltage1	VCC,IOVCC	V	-0.3 ～+4.6	
Power Supply Voltage 2	VCI – AGND	V	-0.3 ～+4.6	
Power Supply Voltage 3	DDVDH – AGND	V	-0.3 ～+6.5	
Power Supply Voltage4	AGND – VCL	V	-0.3 ～+4.6	
Power Supply Voltage 5	DDVDH – VCL	V	-0.3 ～+9.0	
Power Supply Voltage7	AGND – VGL	V	-0.3 ～+14.0	
Power Supply Voltage 8	VGH– VGL	V	-0.3 ～+30.0	
Input Voltage	Vt	V	-0.3 ～IOVCC + 0.3	
Operating Temperature	Topr	℃	-40 ～+85	
Storage Temperature	Tstg	℃	-55 ～+110	

13.2. DC Characteristics

Table 13-2 VCC= 2.50V～3.60V，IOVCC=1.65V～ 3.60V，Ta=-40℃～+85℃

Item	Sym bol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input High level voltage	VIH	V	IOVCC=1.65V～3.60V	0.8xIOVCC	-	IOVCC	
Input Low level voltage	VIL	V	IOVCC=1.65V～3.60V	-0.3	-	0.2xIOVCC	
Output ”High” level voltage 1 （DB0-17）	VOH	V	IOVCC=1.65V～3.60V, IOH=-0.1mA	0.8xIOVCC	-	-	
Output ”Low” level voltage 1 （DB0-17）	VOL	V	IOVCC=1.65V～3.60V, IOL=0.1mA	-	-	0.2xIOVCC	
I/O leak current	ILI1	μA	Vin=0～IOVCC1	-1	-	1	
Current Consumption (IOVCC-IOGND)+(VCC-GND) Normal operation mode (262k-colors, display operation)	IOP1	μA	fosc=678kHz (432 line drive), IOVCC=VCC=3.00V fFLM=60Hz Ta=25℃ RAM data: 18’h000000	-	175	-	
Current Consumption (IOVCC-IOGND)+(VCC-GND) 8-color mode, 64-line, partial display operation	Iop2	μA	fosc=376kHz (64-line, partial display), IOVCC=VCC=3.00V, fFLM=40Hz Ta=25℃ RAM data: 18h’000000	-	140	-	

13.3. AC Characteristics

VCC= 2.50V～3.60V，IOVCC=1.65V～3.60V，Ta=-40℃～+85℃

13.3.1. Clock Characteristics

Table 13-3

Item	Symbol	Unit	Timing Diagram	Min.	Typ.	Max.	Note
RC Oscillation clock	fosc	kHz	IOVCC = VCC = 3.0V, 25°C	611	678	745	

13.3.2. 80-System Bus Interface Timing Characteristics

Table 13-4 Normal write operation (HWM=0), IOVCC=1.65V~3.60V

Item	Symbol		Unit	Min.	Typ.	Max.
Bus cycle time	Write	tCYCW	ns	150	-	-
	Read	tCYCR	ns	450	-	-
Write low-level pulse width		PWLW	ns	55	-	-
Read low-level pulse width		PWLR	ns	170	-	-
Write high-level pulse width		PWHW	ns	70	-	-
Read high-level pulse width		PWHR	ns	250	-	-
Write/Read rise/ fall time		tWRr, WRf	ns	-	-	10
Setup time	Write (RS to CS*,WR*)	tAS	ns	0	-	-
	Read (RS to CS*, RD*)		ns	10	-	-
Address Hold Time		tAH	ns	2	-	-
Write data setup time		tDSW	ns	25	-	-
Write data hold time		tH	ns	10	-	-
Read data delay time		tDDR	ns	-	-	150
Read data hold time		tDHR	ns	5	-	-

13.3.3. Clock-synchronized Serial Interface Timing Characteristics

Normal Write Function (HWM=0), High-speed Write Function (HWM=1), IOVCC=1.65~3.60V)

Table 13-5

Item	Symbol		Unit	Min.	Typ.	Max.
SerialTime Clock Cycle	Write (received)	tSCYC	ns	100	-	20.000
	Read (transmitted)	tSCYC	ns	350	-	20.000
Serial Clock high-level width	Write (received)	tSCH	ns	40	-	-
	Read (transmitted)	tSCH	ns	150	-	-
Serial Clock low-level width	Write (received)	tSCL	ns	40	-	-
	Read (transmitted)	tSCL	ns	150	-	-
Serial clock rise/fall time		tSCr, tSCf	ns	-	-	20
Chip select setup time		tCSU	ns	20	-	-
Chip select hold time		tCH	ns	60	-	-
Serial input data setup time		tSISU	ns	30	-	-
Serial input data hold time		tSIH	ns	30	-	-
Serial output data delay time		tSOD	ns	-	-	130
Serial output data hold time		tSOH	ns	5	-	-

13.3.4. Reset Timing Characteristics (IOVCC=1.65~3.60V)

Table 13-6

Item	Symbol	Unit	Min.	Typ.	Max.
Reset low-level width	tRES	ms	1	—	—
Reset rise time	trRES	μs	—	—	10

13.3.5. RGB Interface Timing Characterics

18-/ 16- bit RGB interface (HWM= 1), IOVCC=1.65~3.60V

Table 13-7

Item	Symbol	Unit	Min.	Typ.	Max.
VSYNC/HSYNC Setup time	TSYNCS	clock	0	-	1
ENABLE Setup time	TENS	ns	10	-	-
ENABLE Hold time	TENH	ns	20	-	-
DOTCLK low-level pulse width	PWDL	ns	40	-	-
DOTCLK high-level pulse width	PWDH	ns	40	-	-
DOTCLK cycle time	TCYCD	ns	100	-	-
Data setup time	TPDS	ns	10	-	-
Data hold time	TPDH	ns	40	-	-
DOTCLK, VSYNC and HSYNC rise/fall time	Trgbr Trgbf	ns	-	-	25

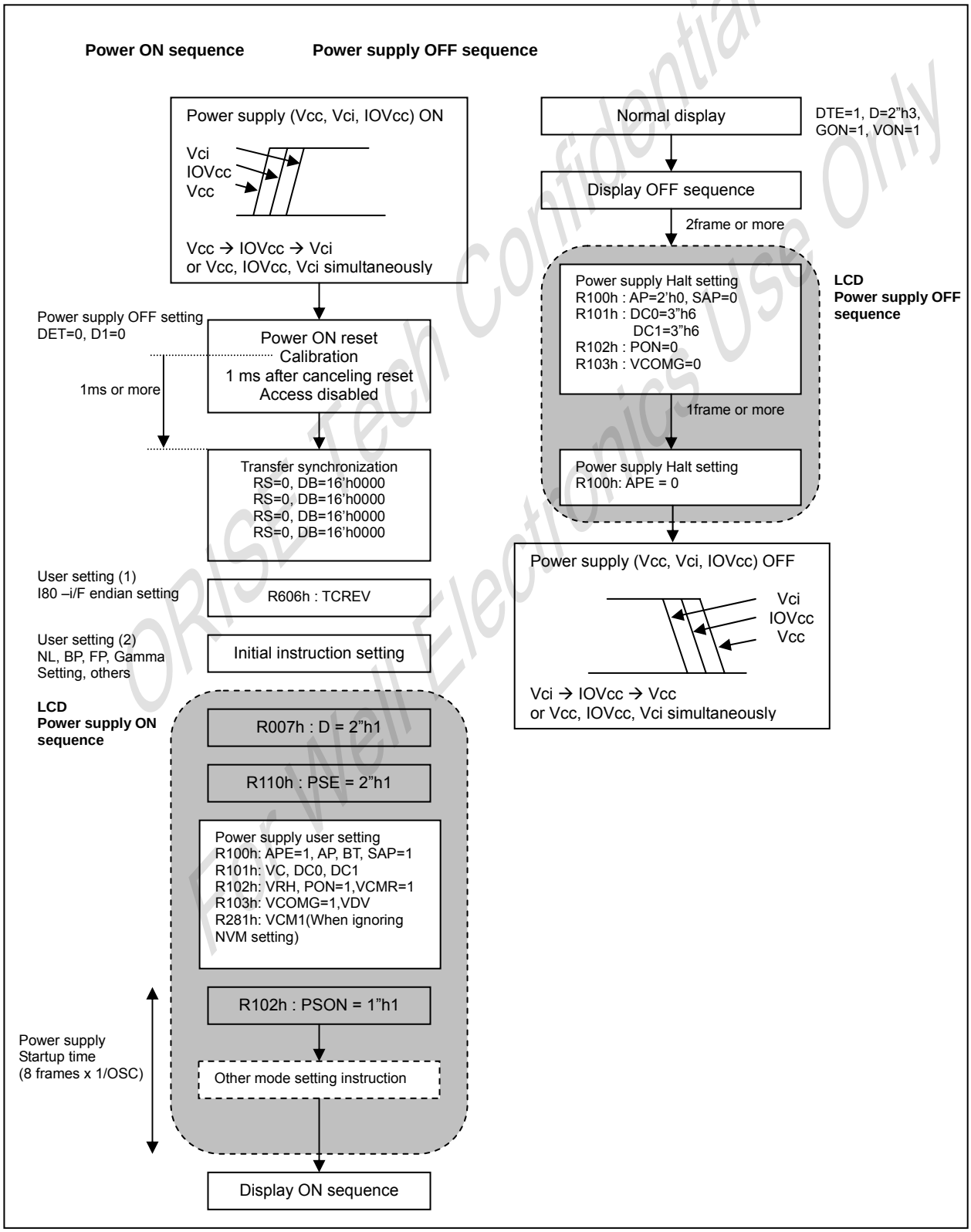
6-bit RGB interface (HWM = 1), IOVCC=1.65~3.60V

Table 13-8

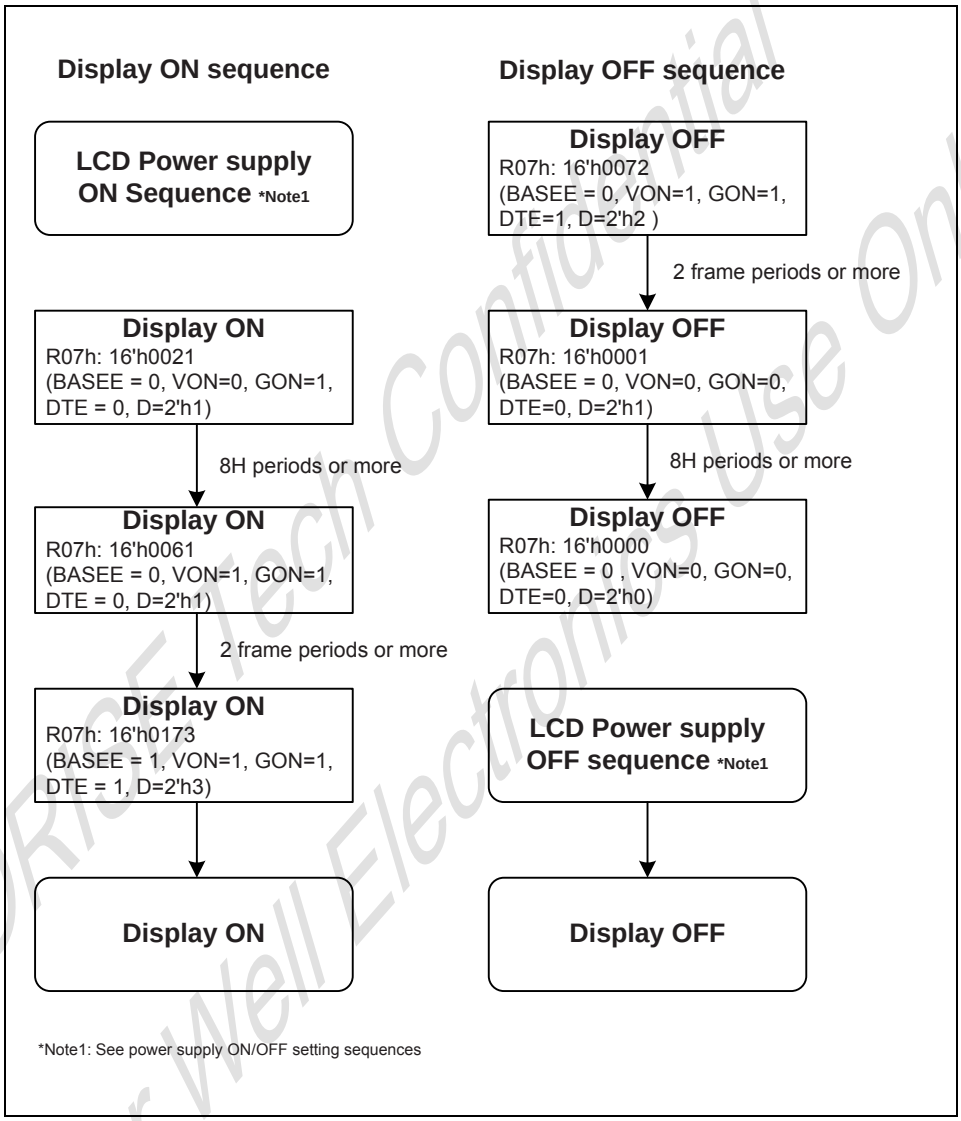
Item	Symbol	Unit	Min.	Typ.	Max.
VSYNC/HSYNC setup time	TSYNCS	clock	0	-	1
ENABLE setup time	TENS	ns	10	-	-
ENABLE hold time	TENH	ns	25	-	-
DOTCLK low-level pulse width	PWDL	ns	25	-	-
DOTCLK high-level pulse width	PWDH	ns	25	-	-
DOTCLK cycle time	TCYCD	ns	60	-	-
Data setup-time	TPDS	ns	10	-	-
Data hold time	TPDH	ns	25	-	-
DOTCLK, VSYNC, and HSYNC rise/fall time	Trgb Ttrgbf	ns	-	-	25

14. Power On/Off sequence

14.1. Power On / Off sequence diagram

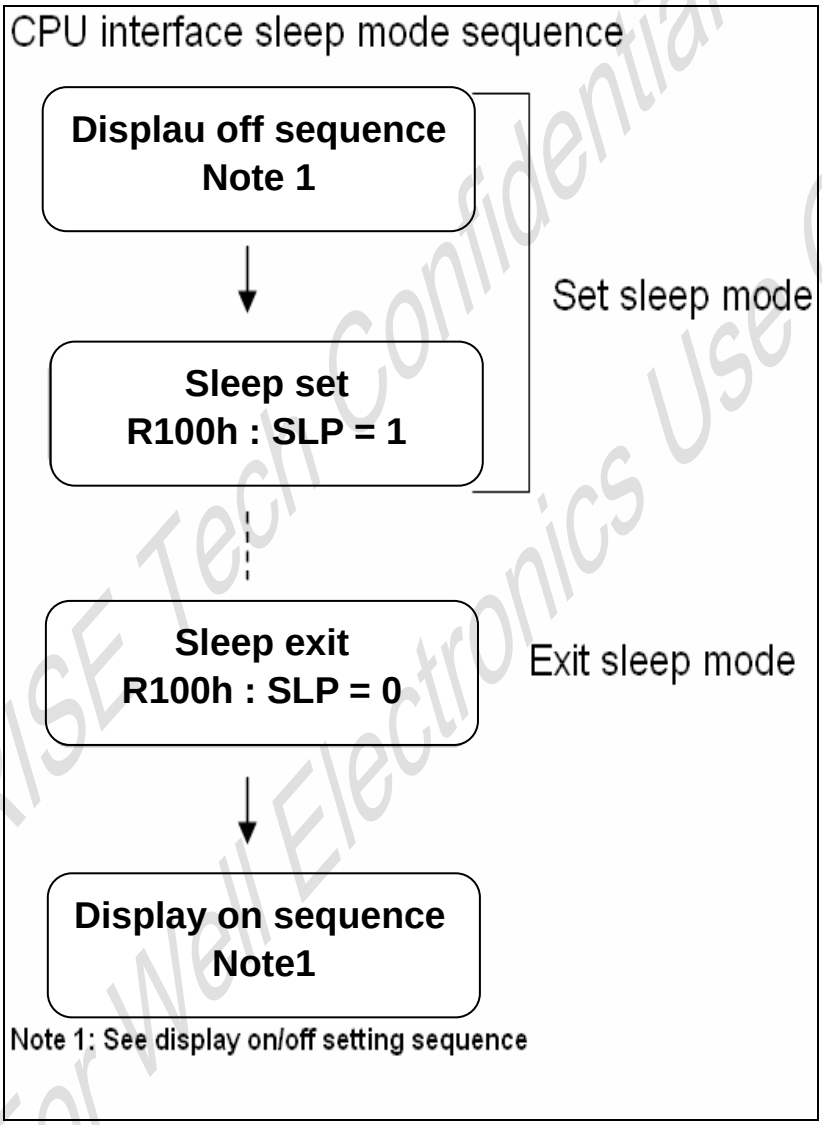


14.2. Display On / Off sequence :

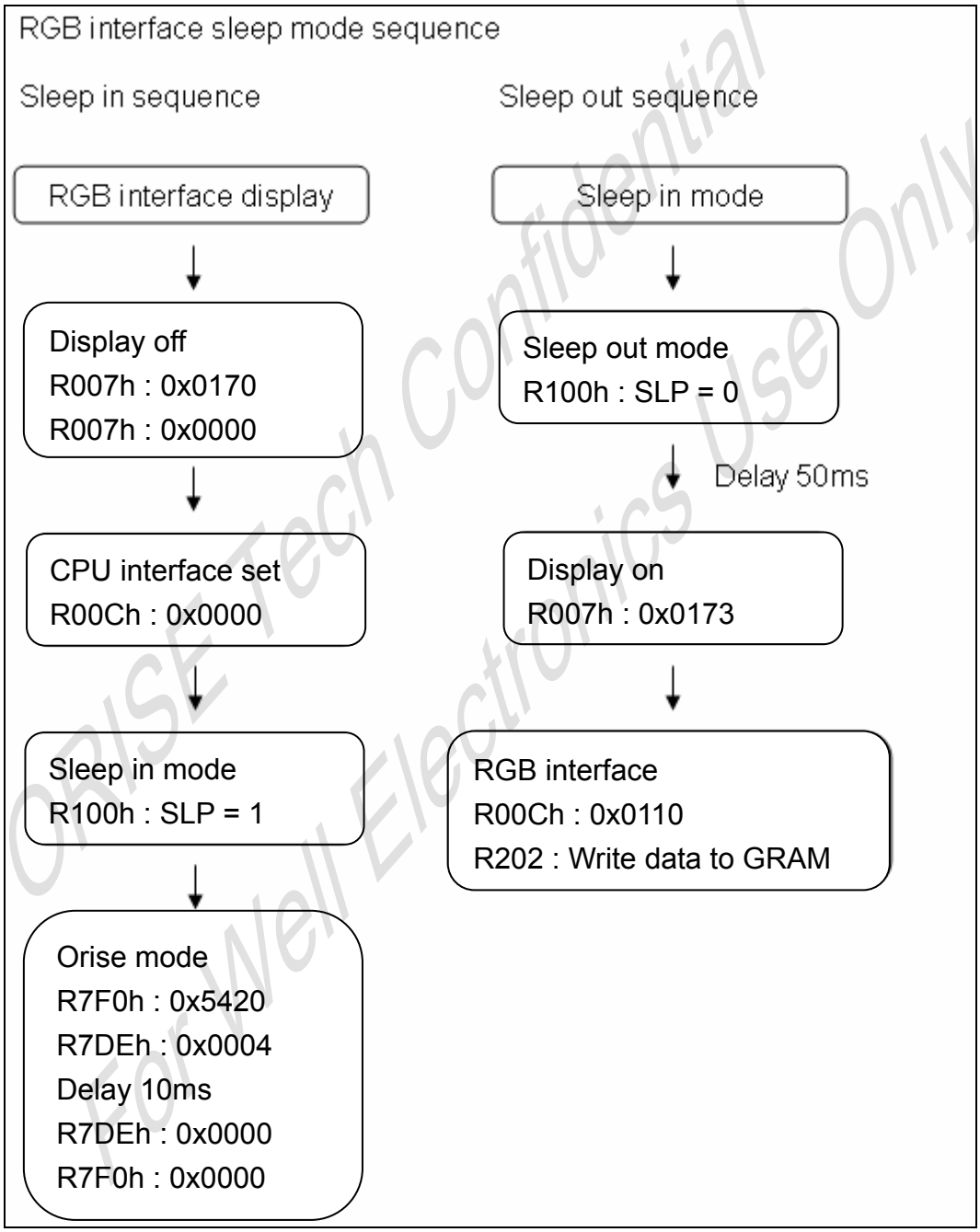


14.3. Sequence to enter and exit sleep mode :

14.3.1. CPU interface mode

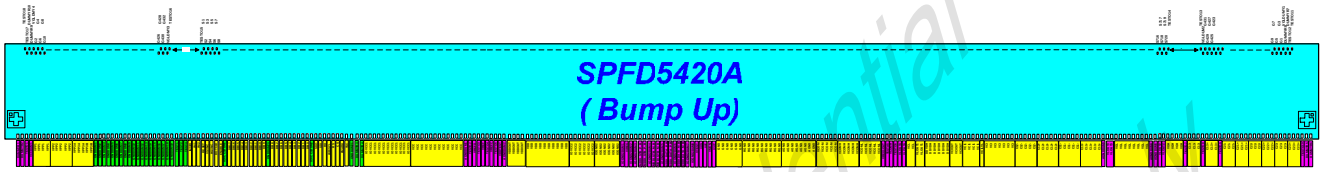


14.3.2. RGB interface mode



15. CHIP INFORMATION

15.1. PAD Assignment

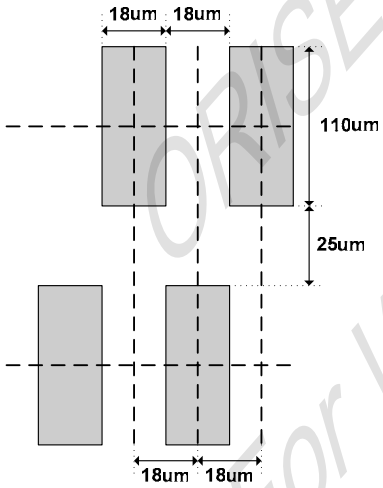


15.2. PAD Dimension

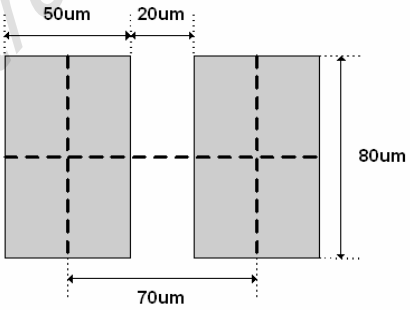
Item	PAD No.	Size		Unit
		X	Y	
Chip Size	-	21550	930	μm
Chip thickness	-	300 ± 25		
Pad pitch	1-299	70	-	
	300-1467	18	-	
Pad size	1-299	50	80	
	300-1467	18	110	

Note1: Chip size included scribe line.

15.2.1. Output Pads



15.2.2. Input Pads



15.3. Bump Characteristics

Item	Standard	Note
Bump Hardness	75Hv	± 25Hv
Bump Height	15μm	± 3μm
Co-planarity (in Chip)	R≦ 2μm	R : Max-Min
Roughness (in Bump)	R≦ 2μm	R : Max-Min
Bump Size	"X" ± 3μm x "Y" ± 3μm	X/Y: bump size
Shear Force	>4.5g/mil^2	

15.4. Pad Locations

NO.	PAD Name	X	Y
1	DUMMYR1	-10430	-359
2	DUMMYR2	-10360	-359
3	TESTO1	-10290	-359
4	VCCDUM1	-10220	-359
5	VPP1	-10150	-359
6	VPP1	-10080	-359
7	VPP1	-10010	-359
8	VPP1	-9940	-359
9	VPP2	-9870	-359
10	VPP2	-9800	-359
11	VPP2	-9730	-359
12	VPP2	-9660	-359
13	VPP2	-9590	-359
14	VPP3A	-9520	-359
15	VPP3A	-9450	-359
16	VPP3A	-9380	-359
17	VPP3B	-9310	-359
18	VPP3B	-9240	-359
19	GNDDUM1	-9170	-359
20	GNDDUM2	-9100	-359
21	GNDDUM3	-9030	-359
22	GNDDUM4	-8960	-359
23	GNDDUM5	-8890	-359
24	GNDDUM6	-8820	-359
25	GNDDUM7	-8750	-359
26	GNDDUM8	-8680	-359
27	GNDDUM9	-8610	-359
28	GNDDUM10	-8540	-359
29	GNDDUM11	-8470	-359
30	GNDDUM12	-8400	-359
31	GNDDUM13	-8330	-359
32	GNDDUM14	-8260	-359
33	GNDDUM15	-8190	-359
34	GNDDUM16	-8120	-359
35	GNDDUM17	-8050	-359
36	GNDDUM18	-7980	-359
37	GNDDUM19	-7910	-359
38	TEST1	-7840	-359
39	TEST2	-7770	-359
40	TEST3	-7700	-359
41	IM0_ID	-7630	-359
42	IM1	-7560	-359
43	IM2	-7490	-359
44	RESET	-7420	-359
45	VSYNC	-7350	-359
46	HSYNC	-7280	-359
47	DOTCLK	-7210	-359
48	ENABLE	-7140	-359
49	IOVCC1DUM1	-7070	-359
50	DB17	-7000	-359
51	DB16	-6930	-359
52	DB15	-6860	-359
53	DB14	-6790	-359
54	DB13	-6720	-359
55	DB12	-6650	-359
56	DB11	-6580	-359
57	DB10	-6510	-359
58	DB9	-6440	-359
59	GNDDUM20	-6370	-359
60	DB8	-6300	-359
61	DB7	-6230	-359
62	DB6	-6160	-359
63	DB5	-6090	-359
64	DB4	-6020	-359
65	DB3	-5950	-359
66	DB2	-5880	-359
67	DB1	-5810	-359
68	DB0	-5740	-359
69	IOVCC1DUM2	-5670	-359
70	SDO	-5600	-359
71	SDI	-5530	-359
72	RD	-5460	-359
73	WR_SCL	-5390	-359
74	RS	-5320	-359
75	CS	-5250	-359
76	FMARK	-5180	-359
77	TSC	-5110	-359
78	GNDDUM21	-5040	-359
79	DUMMYR3	-4970	-359
80	DUMMYR4	-4900	-359
81	IOVCC1	-4830	-359
82	IOVCC1	-4760	-359
83	IOVCC1	-4690	-359
84	IOVCC1	-4620	-359
85	IOVCC1	-4550	-359
86	IOVCC1	-4480	-359
87	IOVCC1	-4410	-359
88	IOVCC1	-4340	-359
89	IOVCC1	-4270	-359
90	IOVCC1	-4200	-359
91	IOVCC1	-4130	-359
92	VCC	-4060	-359
93	VCC	-3990	-359
94	VCC	-3920	-359
95	VCC	-3850	-359
96	VCC	-3780	-359
97	VCC	-3710	-359
98	VCC	-3640	-359
99	VCC	-3570	-359
100	VCC	-3500	-359
101	VCC	-3430	-359
102	VCC	-3360	-359
103	VCC	-3290	-359
104	AGNDDUM1	-3220	-359
105	TESTO2	-3150	-359
106	VREFD	-3080	-359
107	TESTO3	-3010	-359
108	VREF	-2940	-359
109	TESTO4	-2870	-359
110	VREFC	-2800	-359
111	TESTO5	-2730	-359
112	VDDTEST	-2660	-359
113	AGNDDUM2	-2590	-359
114	VDDOUT	-2520	-359
115	VDDOUT	-2450	-359
116	VDDOUT	-2380	-359
117	VDDOUT	-2310	-359
118	VDD	-2240	-359
119	VDD	-2170	-359
120	VDD	-2100	-359
121	VDD	-2030	-359
122	VDD	-1960	-359
123	VDD	-1890	-359
124	VDD	-1820	-359
125	VDD	-1750	-359
126	VDD	-1680	-359
127	VDD	-1610	-359
128	IOVCC2	-1540	-359
129	IOVCC2	-1470	-359
130	IOVCC2	-1400	-359
131	IOVCC2	-1330	-359
132	IOVCC2	-1260	-359
133	IOVCC2	-1190	-359
134	IOGND2	-1120	-359
135	IOGND2	-1050	-359
136	IOGND2	-980	-359
137	IOGND2	-910	-359
138	IOGND2	-840	-359
139	IOGND2	-770	-359
140	IOGND2DUM1	-700	-359
141	VIREG	-630	-359
142	IOGND2DUM2	-560	-359
143	IOGND2DUM3	-490	-359
144	MDDI_STB_P_B	-420	-359
145	MDDI_STB_P_B	-350	-359
146	IOGND2DUM4	-280	-359
147	MDDI_STB_M_B	-210	-359
148	MDDI_STB_M_B	-140	-359
149	IOGND2DUM5	-70	-359
150	MDDI_DATA_P_B	0	-359
151	MDDI_DATA_P_B	70	-359
152	IOGND2DUM6	140	-359
153	MDDI_DATA_M_B	210	-359
154	MDDI_DATA_M_B	280	-359
155	IOGND2DUM7	350	-359
156	IOGND2DUM8	420	-359
157	VTEST	490	-359
158	VGS	560	-359
159	V0T	630	-359
160	VMON	700	-359
161	V31T	770	-359
162	GND	840	-359
163	GND	910	-359
164	GND	980	-359
165	GND	1050	-359
166	GND	1120	-359
167	GND	1190	-359
168	RGND	1260	-359
169	RGND	1330	-359
170	RGND	1400	-359
171	RGND	1470	-359
172	RGND	1540	-359
173	RGND	1610	-359
174	RGND	1680	-359
175	RGND	1750	-359
176	RGND	1820	-359
177	AGND	1890	-359
178	AGND	1960	-359
179	AGND	2030	-359
180	AGND	2100	-359
181	AGND	2170	-359
182	AGND	2240	-359
183	AGND	2310	-359

NO.	PAD Name	X	Y
184	AGND	2380	-359
185	VCOM	2450	-359
186	VCOM	2520	-359
187	VCOM	2590	-359
188	VCOM	2660	-359
189	VCOM	2730	-359
190	VCOMH	2800	-359
191	VCOMH	2870	-359
192	VCOMH	2940	-359
193	VCOMH	3010	-359
194	VCOMH	3080	-359
195	VCOML	3150	-359
196	VCOML	3220	-359
197	VCOML	3290	-359
198	VCOML	3360	-359
199	VCOML	3430	-359
200	VREG1OUT	3500	-359
201	TESTA5	3570	-359
202	VCOMR	3640	-359
203	TESTO6	3710	-359
204	VLOUT4	3780	-359
205	VLOUT4	3850	-359
206	VCL	3920	-359
207	VCL	3990	-359
208	VLOUT1	4060	-359
209	VLOUT1	4130	-359
210	DDVDH	4200	-359
211	DDVDH	4270	-359
212	DDVDH	4340	-359
213	DDVDH	4410	-359
214	DDVDH	4480	-359
215	DDVDH	4550	-359
216	VCIOUT	4620	-359
217	VCIOUT	4690	-359
218	VCIOUT	4760	-359
219	VCI1	4830	-359
220	VCI1	4900	-359
221	VCI1	4970	-359
222	VCI1	5040	-359
223	VCILVL	5110	-359
224	VCI	5180	-359
225	VCI	5250	-359
226	VCI	5320	-359
227	VCI	5390	-359
228	VCI	5460	-359
229	VCI	5530	-359
230	VCI	5600	-359
231	C12N	5670	-359
232	C12N	5740	-359
233	C12N	5810	-359
234	C12N	5880	-359
235	C12N	5950	-359
236	C12P	6020	-359
237	C12P	6090	-359
238	C12P	6160	-359
239	C12P	6230	-359
240	C12P	6300	-359
241	C11N	6370	-359
242	C11N	6440	-359
243	C11N	6510	-359
244	C11N	6580	-359
245	C11N	6650	-359
246	C11P	6720	-359

NO.	PAD Name	X	Y
247	C11P	6790	-359
248	C11P	6860	-359
249	C11P	6930	-359
250	C11P	7000	-359
251	AGNDDUM3	7070	-359
252	VLOUT3	7140	-359
253	VLOUT3	7210	-359
254	VGL	7280	-359
255	VGL	7350	-359
256	VGL	7420	-359
257	VGL	7490	-359
258	VGL	7560	-359
259	VGL	7630	-359
260	VGL	7700	-359
261	VGL	7770	-359
262	AGNDDUM4	7840	-359
263	AGNDDUM5	7910	-359
264	VLOUT2	7980	-359
265	VLOUT2	8050	-359
266	VGH	8120	-359
267	VGH	8190	-359
268	VGH	8260	-359
269	VGH	8330	-359
270	TESTO7	8400	-359
271	C13N	8470	-359
272	C13N	8540	-359
273	C13N	8610	-359
274	TESTO8	8680	-359
275	C13P	8750	-359
276	C13P	8820	-359
277	C13P	8890	-359
278	TESTO9	8960	-359
279	C21N	9030	-359
280	C21N	9100	-359
281	C21N	9170	-359
282	C21P	9240	-359
283	C21P	9310	-359
284	C21P	9380	-359
285	C22N	9450	-359
286	C22N	9520	-359
287	C22N	9590	-359
288	C22P	9660	-359
289	C22P	9730	-359
290	C22P	9800	-359
291	C23N	9870	-359
292	C23N	9940	-359
293	C23N	10010	-359
294	C23P	10080	-359
295	C23P	10150	-359
296	C23P	10220	-359
297	TESTO10	10290	-359
298	DUMMYR5	10360	-359
299	DUMMYR6	10430	-359
300	TESTO11	10647	340
301	TESTO12	10629	205
302	DUMMYR7	10611	340
303	DUMMYR8	10593	205
304	VGLDMY1	10575	340
305	G1	10557	205
306	G3	10539	340
307	G5	10521	205
308	G7	10503	340
309	G9	10485	205

NO.	PAD Name	X	Y
310	G11	10467	340
311	G13	10449	205
312	G15	10431	340
313	G17	10413	205
314	G19	10395	340
315	G21	10377	205
316	G23	10359	340
317	G25	10341	205
318	G27	10323	340
319	G29	10305	205
320	G31	10287	340
321	G33	10269	205
322	G35	10251	340
323	G37	10233	205
324	G39	10215	340
325	G41	10197	205
326	G43	10179	340
327	G45	10161	205
328	G47	10143	340
329	G49	10125	205
330	G51	10107	340
331	G53	10089	205
332	G55	10071	340
333	G57	10053	205
334	G59	10035	340
335	G61	10017	205
336	G63	9999	340
337	G65	9981	205
338	G67	9963	340
339	G69	9945	205
340	G71	9927	340
341	G73	9909	205
342	G75	9891	340
343	G77	9873	205
344	G79	9855	340
345	G81	9837	205
346	G83	9819	340
347	G85	9801	205
348	G87	9783	340
349	G89	9765	205
350	G91	9747	340
351	G93	9729	205
352	G95	9711	340
353	G97	9693	205
354	G99	9675	340
355	G101	9657	205
356	G103	9639	340
357	G105	9621	205
358	G107	9603	340
359	G109	9585	205
360	G111	9567	340
361	G113	9549	205
362	G115	9531	340
363	G117	9513	205
364	G119	9495	340
365	G121	9477	205
366	G123	9459	340
367	G125	9441	205
368	G127	9423	340
369	G129	9405	205
370	G131	9387	340
371	G133	9369	205
372	G135	9351	340

NO.	PAD Name	X	Y
373	G137	9333	205
374	G139	9315	340
375	G141	9297	205
376	G143	9279	340
377	G145	9261	205
378	G147	9243	340
379	G149	9225	205
380	G151	9207	340
381	G153	9189	205
382	G155	9171	340
383	G157	9153	205
384	G159	9135	340
385	G161	9117	205
386	G163	9099	340
387	G165	9081	205
388	G167	9063	340
389	G169	9045	205
390	G171	9027	340
391	G173	9009	205
392	G175	8991	340
393	G177	8973	205
394	G179	8955	340
395	G181	8937	205
396	G183	8919	340
397	G185	8901	205
398	G187	8883	340
399	G189	8865	205
400	G191	8847	340
401	G193	8829	205
402	G195	8811	340
403	G197	8793	205
404	G199	8775	340
405	G201	8757	205
406	G203	8739	340
407	G205	8721	205
408	G207	8703	340
409	G209	8685	205
410	G211	8667	340
411	G213	8649	205
412	G215	8631	340
413	G217	8613	205
414	G219	8595	340
415	G221	8577	205
416	G223	8559	340
417	G225	8541	205
418	G227	8523	340
419	G229	8505	205
420	G231	8487	340
421	G233	8469	205
422	G235	8451	340
423	G237	8433	205
424	G239	8415	340
425	G241	8397	205
426	G243	8379	340
427	G245	8361	205
428	G247	8343	340
429	G249	8325	205
430	G251	8307	340
431	G253	8289	205
432	G255	8271	340
433	G257	8253	205
434	G259	8235	340
435	G261	8217	205

NO.	PAD Name	X	Y
436	G263	8199	340
437	G265	8181	205
438	G267	8163	340
439	G269	8145	205
440	G271	8127	340
441	G273	8109	205
442	G275	8091	340
443	G277	8073	205
444	G279	8055	340
445	G281	8037	205
446	G283	8019	340
447	G285	8001	205
448	G287	7983	340
449	G289	7965	205
450	G291	7947	340
451	G293	7929	205
452	G295	7911	340
453	G297	7893	205
454	G299	7875	340
455	G301	7857	205
456	G303	7839	340
457	G305	7821	205
458	G307	7803	340
459	G309	7785	205
460	G311	7767	340
461	G313	7749	205
462	G315	7731	340
463	G317	7713	205
464	G319	7695	340
465	G321	7677	205
466	G323	7659	340
467	G325	7641	205
468	G327	7623	340
469	G329	7605	205
470	G331	7587	340
471	G333	7569	205
472	G335	7551	340
473	G337	7533	205
474	G339	7515	340
475	G341	7497	205
476	G343	7479	340
477	G345	7461	205
478	G347	7443	340
479	G349	7425	205
480	G351	7407	340
481	G353	7389	205
482	G355	7371	340
483	G357	7353	205
484	G359	7335	340
485	G361	7317	205
486	G363	7299	340
487	G365	7281	205
488	G367	7263	340
489	G369	7245	205
490	G371	7227	340
491	G373	7209	205
492	G375	7191	340
493	G377	7173	205
494	G379	7155	340
495	G381	7137	205
496	G383	7119	340
497	G385	7101	205
498	G387	7083	340

NO.	PAD Name	X	Y
499	G389	7065	205
500	G391	7047	340
501	G393	7029	205
502	G395	7011	340
503	G397	6993	205
504	G399	6975	340
505	G401	6957	205
506	G403	6939	340
507	G405	6921	205
508	G407	6903	340
509	G409	6885	205
510	G411	6867	340
511	G413	6849	205
512	G415	6831	340
513	G417	6813	205
514	G419	6795	340
515	G421	6777	205
516	G423	6759	340
517	G425	6741	205
518	G427	6723	340
519	G429	6705	205
520	G431	6687	340
521	VGLDMY2	6669	205
522	TESTO13	6651	340
523	TESTO14	6417	340
524	S720	6399	205
525	S719	6381	340
526	S718	6363	205
527	S717	6345	340
528	S716	6327	205
529	S715	6309	340
530	S714	6291	205
531	S713	6273	340
532	S712	6255	205
533	S711	6237	340
534	S710	6219	205
535	S709	6201	340
536	S708	6183	205
537	S707	6165	340
538	S706	6147	205
539	S705	6129	340
540	S704	6111	205
541	S703	6093	340
542	S702	6075	205
543	S701	6057	340
544	S700	6039	205
545	S699	6021	340
546	S698	6003	205
547	S697	5985	340
548	S696	5967	205
549	S695	5949	340
550	S694	5931	205
551	S693	5913	340
552	S692	5895	205
553	S691	5877	340
554	S690	5859	205
555	S689	5841	340
556	S688	5823	205
557	S687	5805	340
558	S686	5787	205
559	S685	5769	340
560	S684	5751	205
561	S683	5733	340

NO.	PAD Name	X	Y
562	S682	5715	205
563	S681	5697	340
564	S680	5679	205
565	S679	5661	340
566	S678	5643	205
567	S677	5625	340
568	S676	5607	205
569	S675	5589	340
570	S674	5571	205
571	S673	5553	340
572	S672	5535	205
573	S671	5517	340
574	S670	5499	205
575	S669	5481	340
576	S668	5463	205
577	S667	5445	340
578	S666	5427	205
579	S665	5409	340
580	S664	5391	205
581	S663	5373	340
582	S662	5355	205
583	S661	5337	340
584	S660	5319	205
585	S659	5301	340
586	S658	5283	205
587	S657	5265	340
588	S656	5247	205
589	S655	5229	340
590	S654	5211	205
591	S653	5193	340
592	S652	5175	205
593	S651	5157	340
594	S650	5139	205
595	S649	5121	340
596	S648	5103	205
597	S647	5085	340
598	S646	5067	205
599	S645	5049	340
600	S644	5031	205
601	S643	5013	340
602	S642	4995	205
603	S641	4977	340
604	S640	4959	205
605	S639	4941	340
606	S638	4923	205
607	S637	4905	340
608	S636	4887	205
609	S635	4869	340
610	S634	4851	205
611	S633	4833	340
612	S632	4815	205
613	S631	4797	340
614	S630	4779	205
615	S629	4761	340
616	S628	4743	205
617	S627	4725	340
618	S626	4707	205
619	S625	4689	340
620	S624	4671	205
621	S623	4653	340
622	S622	4635	205
623	S621	4617	340
624	S620	4599	205

NO.	PAD Name	X	Y
625	S619	4581	340
626	S618	4563	205
627	S617	4545	340
628	S616	4527	205
629	S615	4509	340
630	S614	4491	205
631	S613	4473	340
632	S612	4455	205
633	S611	4437	340
634	S610	4419	205
635	S609	4401	340
636	S608	4383	205
637	S607	4365	340
638	S606	4347	205
639	S605	4329	340
640	S604	4311	205
641	S603	4293	340
642	S602	4275	205
643	S601	4257	340
644	S600	4239	205
645	S599	4221	340
646	S598	4203	205
647	S597	4185	340
648	S596	4167	205
649	S595	4149	340
650	S594	4131	205
651	S593	4113	340
652	S592	4095	205
653	S591	4077	340
654	S590	4059	205
655	S589	4041	340
656	S588	4023	205
657	S587	4005	340
658	S586	3987	205
659	S585	3969	340
660	S584	3951	205
661	S583	3933	340
662	S582	3915	205
663	S581	3897	340
664	S580	3879	205
665	S579	3861	340
666	S578	3843	205
667	S577	3825	340
668	S576	3807	205
669	S575	3789	340
670	S574	3771	205
671	S573	3753	340
672	S572	3735	205
673	S571	3717	340
674	S570	3699	205
675	S569	3681	340
676	S568	3663	205
677	S567	3645	340
678	S566	3627	205
679	S565	3609	340
680	S564	3591	205
681	S563	3573	340
682	S562	3555	205
683	S561	3537	340
684	S560	3519	205
685	S559	3501	340
686	S558	3483	205
687	S557	3465	340

NO.	PAD Name	X	Y
688	S556	3447	205
689	S555	3429	340
690	S554	3411	205
691	S553	3393	340
692	S552	3375	205
693	S551	3357	340
694	S550	3339	205
695	S549	3321	340
696	S548	3303	205
697	S547	3285	340
698	S546	3267	205
699	S545	3249	340
700	S544	3231	205
701	S543	3213	340
702	S542	3195	205
703	S541	3177	340
704	S540	3159	205
705	S539	3141	340
706	S538	3123	205
707	S537	3105	340
708	S536	3087	205
709	S535	3069	340
710	S534	3051	205
711	S533	3033	340
712	S532	3015	205
713	S531	2997	340
714	S530	2979	205
715	S529	2961	340
716	S528	2943	205
717	S527	2925	340
718	S526	2907	205
719	S525	2889	340
720	S524	2871	205
721	S523	2853	340
722	S522	2835	205
723	S521	2817	340
724	S520	2799	205
725	S519	2781	340
726	S518	2763	205
727	S517	2745	340
728	S516	2727	205
729	S515	2709	340
730	S514	2691	205
731	S513	2673	340
732	S512	2655	205
733	S511	2637	340
734	S510	2619	205
735	S509	2601	340
736	S508	2583	205
737	S507	2565	340
738	S506	2547	205
739	S505	2529	340
740	S504	2511	205
741	S503	2493	340
742	S502	2475	205
743	S501	2457	340
744	S500	2439	205
745	S499	2421	340
746	S498	2403	205
747	S497	2385	340
748	S496	2367	205
749	S495	2349	340
750	S494	2331	205

NO.	PAD Name	X	Y
751	S493	2313	340
752	S492	2295	205
753	S491	2277	340
754	S490	2259	205
755	S489	2241	340
756	S488	2223	205
757	S487	2205	340
758	S486	2187	205
759	S485	2169	340
760	S484	2151	205
761	S483	2133	340
762	S482	2115	205
763	S481	2097	340
764	S480	2079	205
765	S479	2061	340
766	S478	2043	205
767	S477	2025	340
768	S476	2007	205
769	S475	1989	340
770	S474	1971	205
771	S473	1953	340
772	S472	1935	205
773	S471	1917	340
774	S470	1899	205
775	S469	1881	340
776	S468	1863	205
777	S467	1845	340
778	S466	1827	205
779	S465	1809	340
780	S464	1791	205
781	S463	1773	340
782	S462	1755	205
783	S461	1737	340
784	S460	1719	205
785	S459	1701	340
786	S458	1683	205
787	S457	1665	340
788	S456	1647	205
789	S455	1629	340
790	S454	1611	205
791	S453	1593	340
792	S452	1575	205
793	S451	1557	340
794	S450	1539	205
795	S449	1521	340
796	S448	1503	205
797	S447	1485	340
798	S446	1467	205
799	S445	1449	340
800	S444	1431	205
801	S443	1413	340
802	S442	1395	205
803	S441	1377	340
804	S440	1359	205
805	S439	1341	340
806	S438	1323	205
807	S437	1305	340
808	S436	1287	205
809	S435	1269	340
810	S434	1251	205
811	S433	1233	340
812	S432	1215	205
813	S431	1197	340

NO.	PAD Name	X	Y
814	S430	1179	205
815	S429	1161	340
816	S428	1143	205
817	S427	1125	340
818	S426	1107	205
819	S425	1089	340
820	S424	1071	205
821	S423	1053	340
822	S422	1035	205
823	S421	1017	340
824	S420	999	205
825	S419	981	340
826	S418	963	205
827	S417	945	340
828	S416	927	205
829	S415	909	340
830	S414	891	205
831	S413	873	340
832	S412	855	205
833	S411	837	340
834	S410	819	205
835	S409	801	340
836	S408	783	205
837	S407	765	340
838	S406	747	205
839	S405	729	340
840	S404	711	205
841	S403	693	340
842	S402	675	205
843	S401	657	340
844	S400	639	205
845	S399	621	340
846	S398	603	205
847	S397	585	340
848	S396	567	205
849	S395	549	340
850	S394	531	205
851	S393	513	340
852	S392	495	205
853	S391	477	340
854	S390	459	205
855	S389	441	340
856	S388	423	205
857	S387	405	340
858	S386	387	205
859	S385	369	340
860	S384	351	205
861	S383	333	340
862	S382	315	205
863	S381	297	340
864	S380	279	205
865	S379	261	340
866	S378	243	205
867	S377	225	340
868	S376	207	205
869	S375	189	340
870	S374	171	205
871	S373	153	340
872	S372	135	205
873	S371	117	340
874	S370	99	205
875	S369	81	340
876	S368	63	205

NO.	PAD Name	X	Y
877	S367	45	340
878	S366	27	205
879	S365	9	340
880	S364	-9	205
881	S363	-27	340
882	S362	-45	205
883	S361	-63	340
884	S360	-81	205
885	S359	-99	340
886	S358	-117	205
887	S357	-135	340
888	S356	-153	205
889	S355	-171	340
890	S354	-189	205
891	S353	-207	340
892	S352	-225	205
893	S351	-243	340
894	S350	-261	205
895	S349	-279	340
896	S348	-297	205
897	S347	-315	340
898	S346	-333	205
899	S345	-351	340
900	S344	-369	205
901	S343	-387	340
902	S342	-405	205
903	S341	-423	340
904	S340	-441	205
905	S339	-459	340
906	S338	-477	205
907	S337	-495	340
908	S336	-513	205
909	S335	-531	340
910	S334	-549	205
911	S333	-567	340
912	S332	-585	205
913	S331	-603	340
914	S330	-621	205
915	S329	-639	340
916	S328	-657	205
917	S327	-675	340
918	S326	-693	205
919	S325	-711	340
920	S324	-729	205
921	S323	-747	340
922	S322	-765	205
923	S321	-783	340
924	S320	-801	205
925	S319	-819	340
926	S318	-837	205
927	S317	-855	340
928	S316	-873	205
929	S315	-891	340
930	S314	-909	205
931	S313	-927	340
932	S312	-945	205
933	S311	-963	340
934	S310	-981	205
935	S309	-999	340
936	S308	-1017	205
937	S307	-1035	340
938	S306	-1053	205
939	S305	-1071	340

NO.	PAD Name	X	Y
940	S304	-1089	205
941	S303	-1107	340
942	S302	-1125	205
943	S301	-1143	340
944	S300	-1161	205
945	S299	-1179	340
946	S298	-1197	205
947	S297	-1215	340
948	S296	-1233	205
949	S295	-1251	340
950	S294	-1269	205
951	S293	-1287	340
952	S292	-1305	205
953	S291	-1323	340
954	S290	-1341	205
955	S289	-1359	340
956	S288	-1377	205
957	S287	-1395	340
958	S286	-1413	205
959	S285	-1431	340
960	S284	-1449	205
961	S283	-1467	340
962	S282	-1485	205
963	S281	-1503	340
964	S280	-1521	205
965	S279	-1539	340
966	S278	-1557	205
967	S277	-1575	340
968	S276	-1593	205
969	S275	-1611	340
970	S274	-1629	205
971	S273	-1647	340
972	S272	-1665	205
973	S271	-1683	340
974	S270	-1701	205
975	S269	-1719	340
976	S268	-1737	205
977	S267	-1755	340
978	S266	-1773	205
979	S265	-1791	340
980	S264	-1809	205
981	S263	-1827	340
982	S262	-1845	205
983	S261	-1863	340
984	S260	-1881	205
985	S259	-1899	340
986	S258	-1917	205
987	S257	-1935	340
988	S256	-1953	205
989	S255	-1971	340
990	S254	-1989	205
991	S253	-2007	340
992	S252	-2025	205
993	S251	-2043	340
994	S250	-2061	205
995	S249	-2079	340
996	S248	-2097	205
997	S247	-2115	340
998	S246	-2133	205
999	S245	-2151	340
1000	S244	-2169	205
1001	S243	-2187	340
1002	S242	-2205	205

NO.	PAD Name	X	Y
1003	S241	-2223	340
1004	S240	-2241	205
1005	S239	-2259	340
1006	S238	-2277	205
1007	S237	-2295	340
1008	S236	-2313	205
1009	S235	-2331	340
1010	S234	-2349	205
1011	S233	-2367	340
1012	S232	-2385	205
1013	S231	-2403	340
1014	S230	-2421	205
1015	S229	-2439	340
1016	S228	-2457	205
1017	S227	-2475	340
1018	S226	-2493	205
1019	S225	-2511	340
1020	S224	-2529	205
1021	S223	-2547	340
1022	S222	-2565	205
1023	S221	-2583	340
1024	S220	-2601	205
1025	S219	-2619	340
1026	S218	-2637	205
1027	S217	-2655	340
1028	S216	-2673	205
1029	S215	-2691	340
1030	S214	-2709	205
1031	S213	-2727	340
1032	S212	-2745	205
1033	S211	-2763	340
1034	S210	-2781	205
1035	S209	-2799	340
1036	S208	-2817	205
1037	S207	-2835	340
1038	S206	-2853	205
1039	S205	-2871	340
1040	S204	-2889	205
1041	S203	-2907	340
1042	S202	-2925	205
1043	S201	-2943	340
1044	S200	-2961	205
1045	S199	-2979	340
1046	S198	-2997	205
1047	S197	-3015	340
1048	S196	-3033	205
1049	S195	-3051	340
1050	S194	-3069	205
1051	S193	-3087	340
1052	S192	-3105	205
1053	S191	-3123	340
1054	S190	-3141	205
1055	S189	-3159	340
1056	S188	-3177	205
1057	S187	-3195	340
1058	S186	-3213	205
1059	S185	-3231	340
1060	S184	-3249	205
1061	S183	-3267	340
1062	S182	-3285	205
1063	S181	-3303	340
1064	S180	-3321	205
1065	S179	-3339	340

NO.	PAD Name	X	Y
1066	S178	-3357	205
1067	S177	-3375	340
1068	S176	-3393	205
1069	S175	-3411	340
1070	S174	-3429	205
1071	S173	-3447	340
1072	S172	-3465	205
1073	S171	-3483	340
1074	S170	-3501	205
1075	S169	-3519	340
1076	S168	-3537	205
1077	S167	-3555	340
1078	S166	-3573	205
1079	S165	-3591	340
1080	S164	-3609	205
1081	S163	-3627	340
1082	S162	-3645	205
1083	S161	-3663	340
1084	S160	-3681	205
1085	S159	-3699	340
1086	S158	-3717	205
1087	S157	-3735	340
1088	S156	-3753	205
1089	S155	-3771	340
1090	S154	-3789	205
1091	S153	-3807	340
1092	S152	-3825	205
1093	S151	-3843	340
1094	S150	-3861	205
1095	S149	-3879	340
1096	S148	-3897	205
1097	S147	-3915	340
1098	S146	-3933	205
1099	S145	-3951	340
1100	S144	-3969	205
1101	S143	-3987	340
1102	S142	-4005	205
1103	S141	-4023	340
1104	S140	-4041	205
1105	S139	-4059	340
1106	S138	-4077	205
1107	S137	-4095	340
1108	S136	-4113	205
1109	S135	-4131	340
1110	S134	-4149	205
1111	S133	-4167	340
1112	S132	-4185	205
1113	S131	-4203	340
1114	S130	-4221	205
1115	S129	-4239	340
1116	S128	-4257	205
1117	S127	-4275	340
1118	S126	-4293	205
1119	S125	-4311	340
1120	S124	-4329	205
1121	S123	-4347	340
1122	S122	-4365	205
1123	S121	-4383	340
1124	S120	-4401	205
1125	S119	-4419	340
1126	S118	-4437	205
1127	S117	-4455	340
1128	S116	-4473	205

NO.	PAD Name	X	Y
1129	S115	-4491	340
1130	S114	-4509	205
1131	S113	-4527	340
1132	S112	-4545	205
1133	S111	-4563	340
1134	S110	-4581	205
1135	S109	-4599	340
1136	S108	-4617	205
1137	S107	-4635	340
1138	S106	-4653	205
1139	S105	-4671	340
1140	S104	-4689	205
1141	S103	-4707	340
1142	S102	-4725	205
1143	S101	-4743	340
1144	S100	-4761	205
1145	S99	-4779	340
1146	S98	-4797	205
1147	S97	-4815	340
1148	S96	-4833	205
1149	S95	-4851	340
1150	S94	-4869	205
1151	S93	-4887	340
1152	S92	-4905	205
1153	S91	-4923	340
1154	S90	-4941	205
1155	S89	-4959	340
1156	S88	-4977	205
1157	S87	-4995	340
1158	S86	-5013	205
1159	S85	-5031	340
1160	S84	-5049	205
1161	S83	-5067	340
1162	S82	-5085	205
1163	S81	-5103	340
1164	S80	-5121	205
1165	S79	-5139	340
1166	S78	-5157	205
1167	S77	-5175	340
1168	S76	-5193	205
1169	S75	-5211	340
1170	S74	-5229	205
1171	S73	-5247	340
1172	S72	-5265	205
1173	S71	-5283	340
1174	S70	-5301	205
1175	S69	-5319	340
1176	S68	-5337	205
1177	S67	-5355	340
1178	S66	-5373	205
1179	S65	-5391	340
1180	S64	-5409	205
1181	S63	-5427	340
1182	S62	-5445	205
1183	S61	-5463	340
1184	S60	-5481	205
1185	S59	-5499	340
1186	S58	-5517	205
1187	S57	-5535	340
1188	S56	-5553	205
1189	S55	-5571	340
1190	S54	-5589	205
1191	S53	-5607	340

NO.	PAD Name	X	Y
1192	S52	-5625	205
1193	S51	-5643	340
1194	S50	-5661	205
1195	S49	-5679	340
1196	S48	-5697	205
1197	S47	-5715	340
1198	S46	-5733	205
1199	S45	-5751	340
1200	S44	-5769	205
1201	S43	-5787	340
1202	S42	-5805	205
1203	S41	-5823	340
1204	S40	-5841	205
1205	S39	-5859	340
1206	S38	-5877	205
1207	S37	-5895	340
1208	S36	-5913	205
1209	S35	-5931	340
1210	S34	-5949	205
1211	S33	-5967	340
1212	S32	-5985	205
1213	S31	-6003	340
1214	S30	-6021	205
1215	S29	-6039	340
1216	S28	-6057	205
1217	S27	-6075	340
1218	S26	-6093	205
1219	S25	-6111	340
1220	S24	-6129	205
1221	S23	-6147	340
1222	S22	-6165	205
1223	S21	-6183	340
1224	S20	-6201	205
1225	S19	-6219	340
1226	S18	-6237	205
1227	S17	-6255	340
1228	S16	-6273	205
1229	S15	-6291	340
1230	S14	-6309	205
1231	S13	-6327	340
1232	S12	-6345	205
1233	S11	-6363	340
1234	S10	-6381	205
1235	S9	-6399	340
1236	S8	-6417	205
1237	S7	-6435	340
1238	S6	-6453	205
1239	S5	-6471	340
1240	S4	-6489	205
1241	S3	-6507	340
1242	S2	-6525	205
1243	S1	-6543	340
1244	TESTO15	-6561	205
1245	TESTO16	-6651	340
1246	VGLDMY3	-6669	205
1247	G432	-6687	340
1248	G430	-6705	205
1249	G428	-6723	340
1250	G426	-6741	205
1251	G424	-6759	340
1252	G422	-6777	205
1253	G420	-6795	340
1254	G418	-6813	205

NO.	PAD Name	X	Y
1255	G416	-6831	340
1256	G414	-6849	205
1257	G412	-6867	340
1258	G410	-6885	205
1259	G408	-6903	340
1260	G406	-6921	205
1261	G404	-6939	340
1262	G402	-6957	205
1263	G400	-6975	340
1264	G398	-6993	205
1265	G396	-7011	340
1266	G394	-7029	205
1267	G392	-7047	340
1268	G390	-7065	205
1269	G388	-7083	340
1270	G386	-7101	205
1271	G384	-7119	340
1272	G382	-7137	205
1273	G380	-7155	340
1274	G378	-7173	205
1275	G376	-7191	340
1276	G374	-7209	205
1277	G372	-7227	340
1278	G370	-7245	205
1279	G368	-7263	340
1280	G366	-7281	205
1281	G364	-7299	340
1282	G362	-7317	205
1283	G360	-7335	340
1284	G358	-7353	205
1285	G356	-7371	340
1286	G354	-7389	205
1287	G352	-7407	340
1288	G350	-7425	205
1289	G348	-7443	340
1290	G346	-7461	205
1291	G344	-7479	340
1292	G342	-7497	205
1293	G340	-7515	340
1294	G338	-7533	205
1295	G336	-7551	340
1296	G334	-7569	205
1297	G332	-7587	340
1298	G330	-7605	205
1299	G328	-7623	340
1300	G326	-7641	205
1301	G324	-7659	340
1302	G322	-7677	205
1303	G320	-7695	340
1304	G318	-7713	205
1305	G316	-7731	340
1306	G314	-7749	205
1307	G312	-7767	340
1308	G310	-7785	205
1309	G308	-7803	340
1310	G306	-7821	205
1311	G304	-7839	340
1312	G302	-7857	205
1313	G300	-7875	340
1314	G298	-7893	205
1315	G296	-7911	340
1316	G294	-7929	205
1317	G292	-7947	340

NO.	PAD Name	X	Y
1318	G290	-7965	205
1319	G288	-7983	340
1320	G286	-8001	205
1321	G284	-8019	340
1322	G282	-8037	205
1323	G280	-8055	340
1324	G278	-8073	205
1325	G276	-8091	340
1326	G274	-8109	205
1327	G272	-8127	340
1328	G270	-8145	205
1329	G268	-8163	340
1330	G266	-8181	205
1331	G264	-8199	340
1332	G262	-8217	205
1333	G260	-8235	340
1334	G258	-8253	205
1335	G256	-8271	340
1336	G254	-8289	205
1337	G252	-8307	340
1338	G250	-8325	205
1339	G248	-8343	340
1340	G246	-8361	205
1341	G244	-8379	340
1342	G242	-8397	205
1343	G240	-8415	340
1344	G238	-8433	205
1345	G236	-8451	340
1346	G234	-8469	205
1347	G232	-8487	340
1348	G230	-8505	205
1349	G228	-8523	340
1350	G226	-8541	205
1351	G224	-8559	340
1352	G222	-8577	205
1353	G220	-8595	340
1354	G218	-8613	205
1355	G216	-8631	340
1356	G214	-8649	205
1357	G212	-8667	340
1358	G210	-8685	205
1359	G208	-8703	340
1360	G206	-8721	205
1361	G204	-8739	340
1362	G202	-8757	205
1363	G200	-8775	340
1364	G198	-8793	205
1365	G196	-8811	340
1366	G194	-8829	205
1367	G192	-8847	340
1368	G190	-8865	205
1369	G188	-8883	340
1370	G186	-8901	205

NO.	PAD Name	X	Y
1371	G184	-8919	340
1372	G182	-8937	205
1373	G180	-8955	340
1374	G178	-8973	205
1375	G176	-8991	340
1376	G174	-9009	205
1377	G172	-9027	340
1378	G170	-9045	205
1379	G168	-9063	340
1380	G166	-9081	205
1381	G164	-9099	340
1382	G162	-9117	205
1383	G160	-9135	340
1384	G158	-9153	205
1385	G156	-9171	340
1386	G154	-9189	205
1387	G152	-9207	340
1388	G150	-9225	205
1389	G148	-9243	340
1390	G146	-9261	205
1391	G144	-9279	340
1392	G142	-9297	205
1393	G140	-9315	340
1394	G138	-9333	205
1395	G136	-9351	340
1396	G134	-9369	205
1397	G132	-9387	340
1398	G130	-9405	205
1399	G128	-9423	340
1400	G126	-9441	205
1401	G124	-9459	340
1402	G122	-9477	205
1403	G120	-9495	340
1404	G118	-9513	205
1405	G116	-9531	340
1406	G114	-9549	205
1407	G112	-9567	340
1408	G110	-9585	205
1409	G108	-9603	340
1410	G106	-9621	205
1411	G104	-9639	340
1412	G102	-9657	205
1413	G100	-9675	340
1414	G98	-9693	205
1415	G96	-9711	340
1416	G94	-9729	205
1417	G92	-9747	340
1418	G90	-9765	205
1419	G88	-9783	340
1420	G86	-9801	205
1421	G84	-9819	340
1422	G82	-9837	205
1423	G80	-9855	340

NO.	PAD Name	X	Y
1424	G78	-9873	205
1425	G76	-9891	340
1426	G74	-9909	205
1427	G72	-9927	340
1428	G70	-9945	205
1429	G68	-9963	340
1430	G66	-9981	205
1431	G64	-9999	340
1432	G62	-10017	205
1433	G60	-10035	340
1434	G58	-10053	205
1435	G56	-10071	340
1436	G54	-10089	205
1437	G52	-10107	340
1438	G50	-10125	205
1439	G48	-10143	340
1440	G46	-10161	205
1441	G44	-10179	340
1442	G42	-10197	205
1443	G40	-10215	340
1444	G38	-10233	205
1445	G36	-10251	340
1446	G34	-10269	205
1447	G32	-10287	340
1448	G30	-10305	205
1449	G28	-10323	340
1450	G26	-10341	205
1451	G24	-10359	340
1452	G22	-10377	205
1453	G20	-10395	340
1454	G18	-10413	205
1455	G16	-10431	340
1456	G14	-10449	205
1457	G12	-10467	340
1458	G10	-10485	205
1459	G8	-10503	340
1460	G6	-10521	205
1461	G4	-10539	340
1462	G2	-10557	205
1463	VGLDMY4	-10575	340
1464	DUMMYR9	-10593	205
1465	DUMMYR10	-10611	340
1466	TESTO17	-10629	205
1467	TESTO18	-10647	340

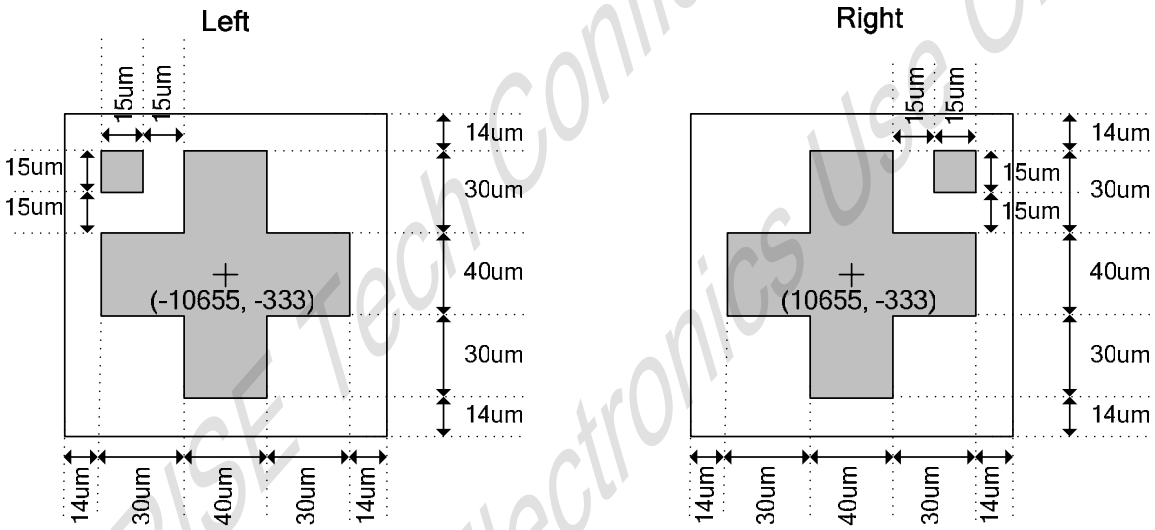
15.5. Alignment Mark

--Alignment Mark coordinate

Left (-10655.0, -333.0)

Right (10655.0, -333.0)

--Alignment Mark size



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17. REVISION HISTORY

Date	Revision #	Description	Page
NOV. 22, 2007	0.7	1. Modify Pad pitch and Pad size. 2. Modify Alignment Mark.	70 79
OCT. 31, 2007	0.6	1. Update ordering information. 2. Modify OTP power supply is 8.25V. 3. Modify Low Power Control (R00Bh). 4. Modify Voltage Generation Diagram. 5. Modify power on/off sequence. 6. Modify PAD Dimension. 7. Modify Bump Characteristics. 8. Typo correction.	4 9 19 59 66 70 71
SEP. 21, 2007	0.5	1.Add ordering information. 2. Modify ID code is 5420. 3. Modify R002h register. 4. Add γ Control table. 5. Modify RAM access data of 16-bit RGB interface in Figure 8-22. 6. Add gamma correction function contents. 7. Add application circuit. 8. Add initial code. 9. Add Power on/off, display on/off and sleep in/out sequence. 10. Modify PAD Dimension.	4 13 14 35 50 56 59 60 65~68 70
JUL. 30, 2007	0.4	1. Modify Power supply max input voltage, from 3.1V to 3.6V. 2. Modify PAD Assignment.	All 63
JUL. 23, 2007	0.3	Update Instruction R090h(CB15)	12, 25
JUL. 13, 2007	0.2	1. Add PAD Assignment, PAD Dimension, BUMP Dimension, BUMP Characteristic and Alignment Mark. 2. Modify Pad Locations	63-73 65-72
MAY. 20, 2007	0.1	Original	77