

**16 pin DIP** Page 1 of 4  
**SPG SERIES**

PROGRAMMABLE  
 OSCILLATORS

**General Specification**

Frequency range:	0.00027Hz to 1.0MHz
Supply Voltage (V <sub>DD</sub> -GND):	±0.3V to -7.0V max.
Operating Voltage:	5.0V±0.5V
Temperature Range	
Operating:	-10° to +70°C
Storage:	-55° to +125°C
Soldering Conditions:	Under 260°C within 10s.
Supply current:	2mA max.
Frequency/Temperature:	-10%/ -120ppm
Ageing:	±5ppm/year max.

**Electrical Specification**

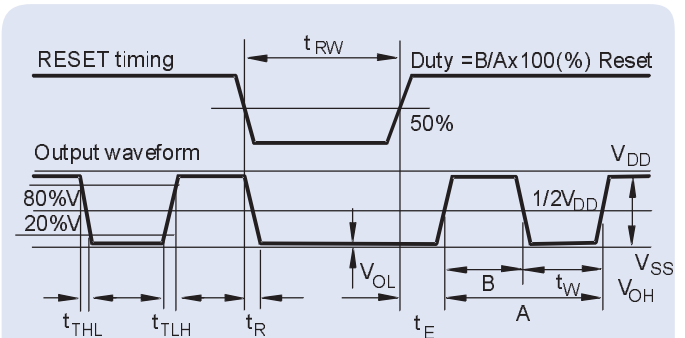
Item	Symb.	min.	typ.	max.	Unit
L.input voltage:	V <sub>IL</sub>	0		0.8	V
H.input voltage:	V <sub>IH</sub>	V <sub>DD</sub> -10		V <sub>DD</sub>	V
L. input current (Reset):	I <sub>RL</sub>	-30		-5	µA
				(Reset = V <sub>SS</sub> )	
H.input current (Reset):	I <sub>RH</sub>			0.5	µA
				(Reset = V <sub>DD</sub> )	
L.i/p current (exc.Reset):	I <sub>IL</sub>	-0.5			µA
H.i/p current (exc.Reset):	I <sub>IH</sub>	5		30	µA
L.output voltage:	V <sub>OL</sub>			0.4	V
				(I <sub>OL</sub> = 1.6mA)	
H.output voltage:	V <sub>OH</sub>	V <sub>DD</sub> -10			V
				(I <sub>OH</sub> = -40µA)	
L.output current:	I <sub>OL</sub>	1.6			µA
				(V <sub>OL</sub> = 0.4V)	
H.output current:	I <sub>OH</sub>			-40	µA
				(V <sub>OH</sub> =V <sub>DD</sub> -1.0V)	
Output rise time:	t <sub>TLH</sub>		30	60	µs
Output fall time:	t <sub>THL</sub>		25	50	µs
Duty:		40		60	%
				(Except 1/3 and 1/5)	
Min. reset pulse width:	t <sub>RW</sub>	1.0			µs
Reset delay time:	t <sub>R</sub>			1.0	µs
Reset release sync. error:	t <sub>E</sub>	t <sub>w</sub> -1/2*		t <sub>w</sub> **	µs
Ext. signal i/p frequency:	F <sub>IN</sub>			1M	Hz
				(8640N only)	
Ext signal i/p pulse width:	t <sub>IN</sub>	0.5			µs
				(8640N only)	
Osc. start-up time:	t <sub>osc</sub>		0.2	1***	s.

\* to = oscillation source cycle, \*\* t<sub>w</sub> = 1/2 cycle of preset frequency  
 \*\*\* for more than 1ms until V<sub>DD</sub> = 0~+4.5V. Time at 4.5V is to be zero

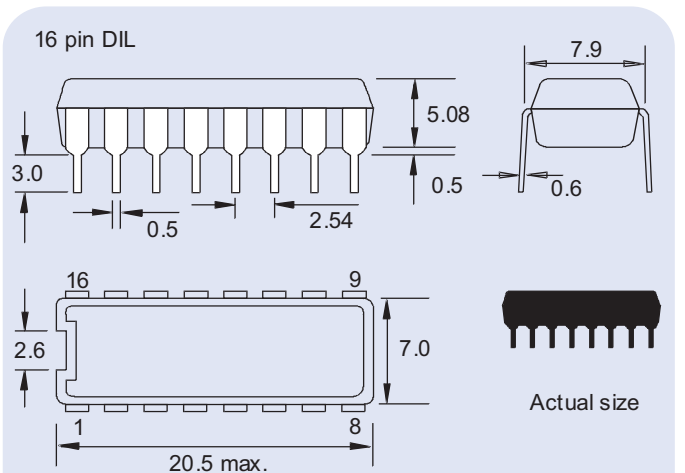
- 57 frequencies programmable from one device
- Low current consumption
- Readily mounted 16 pin DIP

**Part numbers for undivided fundamental frequencies with tolerances and supply current**

Type number	Fundamental Frequency (kHz)	Freq. Tol. (ppm)	Freq./Voltage (ppm)	Current max. (mA)
SPG 8650E	32.768	±50	±10	0.5
SPG 8650A	60.0	±50	±10	0.5
SPG 8650C	96.0	±50	±10	0.5
SPG 8650B	100.0	±50	±10	0.5
SPG 8650D	153.60	±50	±10	0.5
SPG 8640AN	600.0	±100	±20	1.0
SPG 8640CN	768.0	±100	±20	1.5
SPG 8640BN	1000.0	±100	±10	2.0



**RESET Timing**

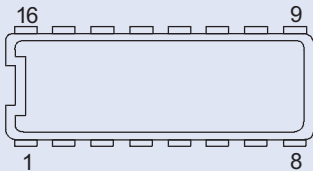


**Outline and Dimensions**

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**Terminal Connections**



**Connections**

- 1 n/c 16 Vdd
- 2 CTL3 15 n/c
- 3 CTL2 14 RESET
- 4 CTL1 13 n/c (CSEL)
- 5 CTL6 12 n/c (EXC)
- 6 CTL5 11 FOUT
- 7 CTL4 10 TEST
- 8 GND 9 OUT

( ) = 8640N only  
 n/c = Do not connect externally

- For 8640  $\bar{O}$
- 11 n/c
  - 12 CLOCK
  - 13 ENABLE

**Terminal connection details**

- CTL 1 - 6** Programmable dividing ratio. (Pull-down resistor incorp.)
- OUT** Output frequency preset by CTL 1 ~ 6. (Refer to the setting procedure of output freq.)
- FOUT** Constant output of the oscillator source frequency. (Built-in quartz crystal).
- RESET** Stops output at RESET = 'L'. (Pull-up resistor incorporated.)
- TEST** Used for testing the input terminal. When CTL 4 is H, output will be 1000 times larger than the preset value at TEST = 'H'. (Pull-down resistor incorp.)
- EXC (8640N only)** Serves as input terminal when using an external clock by changing to the built-in osc. Effective when CSEL is H.
- CSEL (8640N only)** When this terminal is made H, the external clock is selected. (Pull-down resistor incorp.)

**Unused terminals**

- RESET** When unused connect to Vdd.
- TEST** When unused connect to GND.
- CSEL** When unused connect to GND.
- CTL 1 ~ 6** When unused connect to GND.

- Terminals (8650 O)**
- CLOCK** Clock input (max. 1MHz)
  - ENABLE** Connect to Vdd.

**Divider Output Setting**

CTL 1	CTL 2	CTL 3	Division Ratio	CTL 4	CTL 5	CTL 6	Division Ratio
0	0	0	1/1	0	0	0	1/1(1/1)
0	0	1	1/10	0	0	1	1/10(1/2)
0	1	0	1/2	0	1	0	1/10 <sup>2</sup> (1/2 <sup>2</sup> )
0	1	1	1/3	0	1	1	1/10 <sup>3</sup> (1/2 <sup>3</sup> )
1	0	0	1/4	1	0	0	1/10 <sup>4</sup> (1/2 <sup>4</sup> )
1	0	1	1/5	1	0	1	1/10 <sup>5</sup> (1/2 <sup>5</sup> )
1	1	0	1/6	1	1	0	1/10 <sup>6</sup> (1/2 <sup>6</sup> )
1	1	1	1/7	1	1	1	1/10 <sup>7</sup> (1/2 <sup>7</sup> )

Combining the division ratios produces the total division ratio

**Output Frequency Settings**

**8640AN**

Set Terminal		CTL4	0	0	0	0	1	1	1	1
		CTL5	0	0	1	1	0	0	1	1
CTL1	CTL2	CTL6 CTL3	0	1	0	1	0	1	0	1
0	0	0	600k	60k	6k	600	60	6	0.6	0.06
0	0	1	60k	6k	600	60	6	0.6	0.06	0.006
0	1	0	300k	30k	3k	300	30	3	0.3	0.03
0	1	1	200k	20k	2k	200	20	2	0.2	0.02
1	0	0	150k	15k	1.5k	150	15	1.5	0.15	0.015
1	0	1	120k	12k	1.2k	120	12	1.2	0.12	0.012
1	1	0	100k	10k	1k	100	10	1	0.1	0.01
1	1	1	50k	5k	500	50	5	0.5	0.05	0.005

**8640BN**

Set Terminal		CTL4	0	0	0	0	1	1	1	1
		CTL5	0	0	1	1	0	0	1	1
CTL1	CTL2	CTL6 CTL3	0	1	0	1	0	1	0	1
0	0	0	1M	100k	10k	1k	100	10	1	1/10
0	0	1	100k	10k	1k	100	10	1	1/10	1/100
0	1	0	500k	50k	5k	500	50	5	1/2	1/20
0	1	1	333.3k	33.3k	3.3k	333.3	33.3	3.3	1/3	1/30
1	0	0	250k	25k	2.5k	250	25	2.5	1/4	1/40
1	0	1	200k	20k	2k	200	20	2	1/5	1/50
1	1	0	166.6k	16.6k	1.6k	166.6	16.6	1.6	1/6	1/60
1	1	1	83.3k	8.3k	833.3	83.3	8.3	0.83	1/12	1/120

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**Output Frequency Settings**

**8650A**

Set Terminal		CTL4	0	0	0	0	1	1	1	1
		CTL5	0	0	1	1	0	0	1	1
CTL1	CTL2	CTL6 CTL3	0	1	0	1	0	1	0	1
0	0	0	60k	6k	600	60	6	0.6	0.06	0.006
0	0	1	6k	600	60	6	0.6	0.06	0.006	0.0006
0	1	0	30k	3k	300	30	3	0.3	0.03	0.003
0	1	1	20k	2k	200	20	2	0.2	0.02	0.002
1	0	0	15k	1.5k	150	15	1.5	0.15	0.015	0.0015
1	0	1	12k	1.2k	120	12	1.2	0.12	0.012	0.0012
1	1	0	10k	1k	100	10	1	0.1	0.01	0.001
1	1	1	5k	500	50	5	0.5	0.05	0.005	0.0005

**8650B**

Set Terminal		CTL4	0	0	0	0	1	1	1	1
		CTL5	0	0	1	1	0	0	1	1
CTL1	CTL2	CTL6 CTL3	0	1	0	1	0	1	0	1
0	0	0	100k	10k	1k	100	10	1	1/10	1/100
0	0	1	10k	1k	100	10	1	1/10	1/100	1/1000
0	1	0	50k	5k	500	50	5	1/2	1/20	1/200
0	1	1	33.3k	3.3k	333.3	33.3	3.33	1/3	1/30	1/300
1	0	0	25k	2.5k	250	25	2.5	1/4	1/40	1/400
1	0	1	20k	2k	200	20	2	1/5	1/50	1/500
1	1	0	16.6k	1.6k	166.6	16.6	1.6	1/6	1/60	1/600
1	1	1	8.3k	833.3	83.3	8.3	0.83	1/12	1/120	1/1200

**8650E**

Set Terminal		CTL4	0	0	0	0	1	1	1	1
		CTL5	0	0	1	1	0	0	1	1
CTL1	CTL2	CTL6 CTL3	0	1	0	1	0	1	0	1
0	0	0	32768	3276.8	327.68	32.768	3.276	0.3276	0.03276	0.00327
0	0	1	3276.8	327.68	32.768	3.276	0.327	0.0327	0.00327	0.00032
0	1	0	16384	1638.4	163.84	16.384	1.638	0.1638	0.01638	0.00163
0	1	1	10922.6	1092.26	109.22	10.922	1.092	0.1092	0.01092	0.00109
1	0	0	8192	819.2	81.92	8.192	0.819	0.0819	0.00819	0.00081
1	0	1	6553.6	655.36	65.536	6.553	0.655	0.0655	0.00655	0.00065
1	1	0	5461.3	546.13	54.613	5.416	0.546	0.0546	0.00546	0.00054
1	1	1	2730.6	273.06	27.306	2.730	0.273	0.0273	0.00273	0.00027

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**Output Frequency Settings****Baud Rate Generators**  
**8640CN**

CTL1	CTL2	CTL3	CTL4	CTL5	CTL6	Output Frequency (kHz)	Baud Rate Output Example (fo/16)
0	0	0	0	0	0	768	48000 bits/sec
1	0	1	0	0	0	153.6	9600 bits/sec
0	0	1	0	0	0	76.8	4800 bits/sec
0	1	0	0	0	1	38.4	2400 bits/sec
1	0	0	0	0	1	19.2	1200 bits/sec

**8650C**

CTL1	CTL2	CTL3	CTL4	CTL5	CTL6	Output Frequency (kHz)	Baud Rate Output Example (fo/16)
0	0	0	0	0	0	96.0	8000 bits/sec
1	0	1	0	0	0	19.2	1200 bits/sec
0	0	1	0	0	0	9.6	600 bits/sec
0	1	0	0	0	1	4.8	300 bits/sec
0	1	1	0	0	1	3.2	200 bits/sec
1	0	0	0	0	1	2.4	150 bits/sec
1	1	0	0	0	1	1.6	100 bits/sec
1	1	1	0	0	1	0.8	50 bits/sec

**8650D**

CTL1	CTL2	CTL3	CTL4	CTL5	CTL6	Output Frequency (kHz)	Baud Rate Output Example (fo/16)
0	0	0	0	0	0	153.6	9600 bits/sec
0	0	0	0	0	1	76.8	4800 bits/sec
0	0	0	0	1	0	38.4	2400 bits/sec
0	0	0	0	1	1	19.2	1200 bits/sec
0	0	0	1	0	0	9.6	600 bits/sec
0	0	0	1	0	1	4.8	300 bits/sec
0	1	1	1	0	0	3.2	200 bits/sec
0	0	0	1	1	0	2.4	150 bits/sec
1	1	0	1	0	0	1.6	100 bits/sec
0	0	0	1	1	1	1.2	75 bits/sec
1	1	1	1	0	0	0.8	50 bits/sec

**To order**

Quote stock number according to the table on page 7-6.