DATA SHEET

SUNPLUS

SPHE1003A/Ax

DVB-T STB A/V SoC

Preliminary

Nov. 25, 2007

Version 0.1

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DVB STB A/V PROCESSOR

1.GENERAL DESCRIPTION

SPHE1003Ax A/V decoder is a cost effective DVB-T STB A/V decoder. It integrates a DVB-T demodulator, a MPEG-2 Transport Demultiplexer, a MPEG-1/-2/-4 A/V decoding engine, a 2-channel audio DAC and a 4-channel multi-format TV-encoder.

SPHE1003Ax performs real-time PID filtering of transport stream, decode and playback of MPEG-1 and MPEG-2 A/V from DVB-T half-NIM. MPEG-1, MPEG-2, and MPEG-4 can be real time decode and playback from SD/ MMC/ Memory Stick/ Memory Stick Pro memory card or USB2.0 Mass Storage Device inputs by SPHE1003Ax. For audio, it supports MPEGI/II Layer1/2/3, PCM, LPCM audio playback. The TV-encoder supports CVBS, S-video, Component YCbCr/YPbPr, and RGB.

SPHE1003Ax offers state-of-art MPEG decoding function for mainstream DVB STB on desktop, portable or car applications.

In terrestrial field, SPHE1003Ax integrates the COFDM (Coded Orthogonal Frequency Division Multiplex) television demodulator which is compliant with DVB-T (as defined in ESTI EN 300 744 specification). It can be used in either 2K or 8K modes with 6, 7 or 8 MHz channels and supports QPSK/16QAM/64QAM reception. Also, its built-in mobility enhancement channel estimator is special suitable for the mobile applications.

In addition to normal DVB-T STB functions, by having multimedia functions embedded such as MP3, JPEG, and MPEG-1/-2/-4 playback from USB or Storage Devices, SPHE1003Ax delivers an unique position to offer a new level of standard for current STB solution in the market.

SPHE1003Ax has embedded eCOS OS Operating System for customers to develop their own STB solutions. SPHE1003Ax also provides PCB board design reference and developing tools to help customers easier to adopt Sunplus STB solution.

Application utilizing the SPHE1003Ax is presented below:

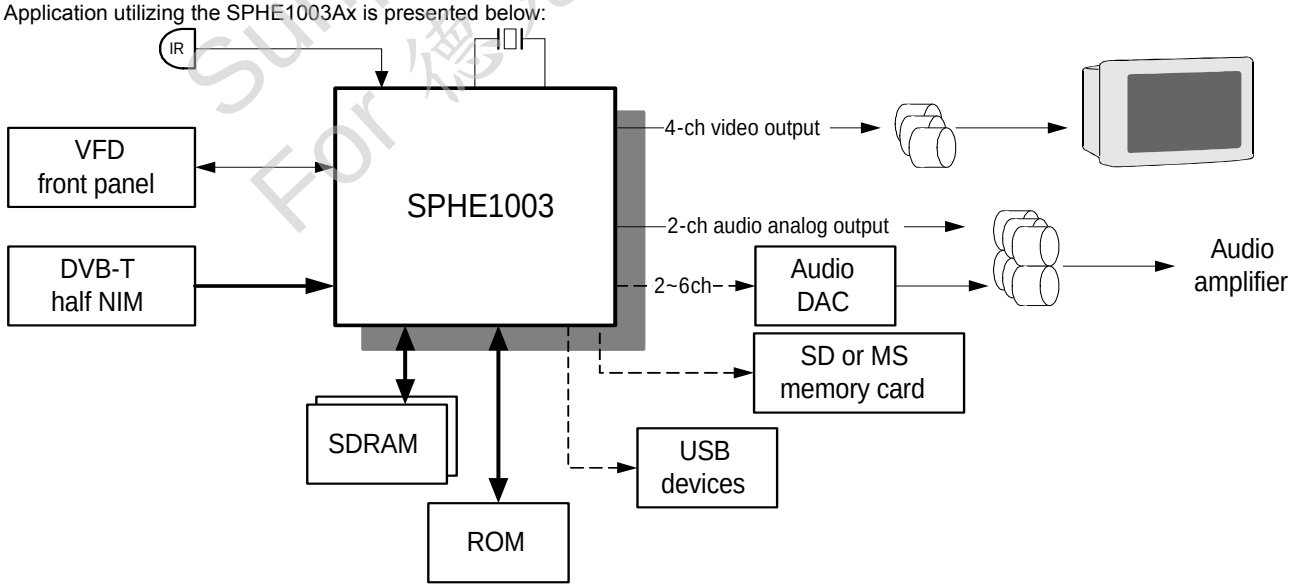


Figure 1-1: SPHE1003Ax system application diagram

2.FEATURE

- DVB-T OFDM demodulator and channel decoder compliant with ESTI EN 300 744
  - Hardware accelerator for channel scan
  - Impulsive interference suppressor
  - Mobility enhancement channel estimator
- MPEG Transport Demux and A/V Decoder
- 32 programmable PID filters
  - One video PID
  - One audio PID
  - 30 general purpose PIDs for generic section or private PES data
- Embedded 32-bit RISC Processor
- Embedded Audio Processor supports multiple audio standards
- Embedded 8-bit I/O processor supports programmable interface control
- Embedded TV encoder with multi-channel built-in high-speed video DAC supports various display standards
- Embedded 2-channel 24-bit audio DAC
- Built-in system PLL and audio PLL generate all clock sources required from single 27MHz crystal input
- Video Decoder
  - Real time MPEG-2 MP@ML decoding
  - Real time MPEG-4 ASP D1 resolution decoding
  - Real time MPEG-1 D1 (720x480x30 /720x576x25) decoding
  - Advanced decoding and display control
  - Embedded hardware JPEG accelerator
- Audio Decoder
  - Flexible Programmable DSP Architecture
  - Support LPCM and PCM playback
  - Support WMA™*1 playback
  - Support MPEGI/II layer 1/2/3
- SDRAM controller
  - High Performance SDRAM controller
  - Support x16 operation
  - Support up to 2 SDRAM devices
  - Support 16M/64M-bit SDRAM devices
- Video Display
  - De-interlacing of interlaced video source
  - Flexible vertical interpolation
  - Flexible horizontal interpolation with optional CIF filter
  - Support YUV422, 8-bit indexed color format
- OSD
  - Multiple OSD regions with different formats
  - Support 2/4/16/256 indexed color with de-flickering
  - Support 16/24-bit direct color
- Embedded TV encoder
  - Support 480i/576i/480p/576p format
  - Support 720p/1080i HD format
  - Support CVBS and S-Video or Component (YUV/ SCART-RGB) output
- Interface
  - 27MHz crystal driver
  - MPEG parallel or serial Transport Stream I/F
  - 16-bit SDRAM interface
  - Serial 2-/4-bit SPI flash interface
  - 8-bit ROM/FLASH interface
  - One UART port
  - Support IR
  - 4-channel 12-bit video DAC analog output
  - Digital CCIR656 output
  - Memory card I/F supports SD, MMC, MS/MS-Pro, SMC, XD
  - Support USB2.0 embedded-host
  - IEC958/SPDIF digital output
  - 2-channel 24-bit audio DAC analog output
  - Support 32.768KHz RTC (Real Time Clock)
- Low power
  - Advanced low power design
  - Selective standby mode
  - Programmable low speed operation
- Technology
  - Advanced CMOS technology
  - 128-pin LQFP package (14x14x1.4mm) or 216-pin LQFP package (24x24x1.4mm)
  - 3v (I/O) and 1.8v (kernel) power supplies
  - 5v I/O tolerance

■ SPHE1003Ax Product Part Number:

For Detail SPHE1003Ax Family Product Part Number, please contact with Sunplus Sales.

*1 WMA is a trademark of Microsoft Corporation

3.BLOCK DIAGRAM

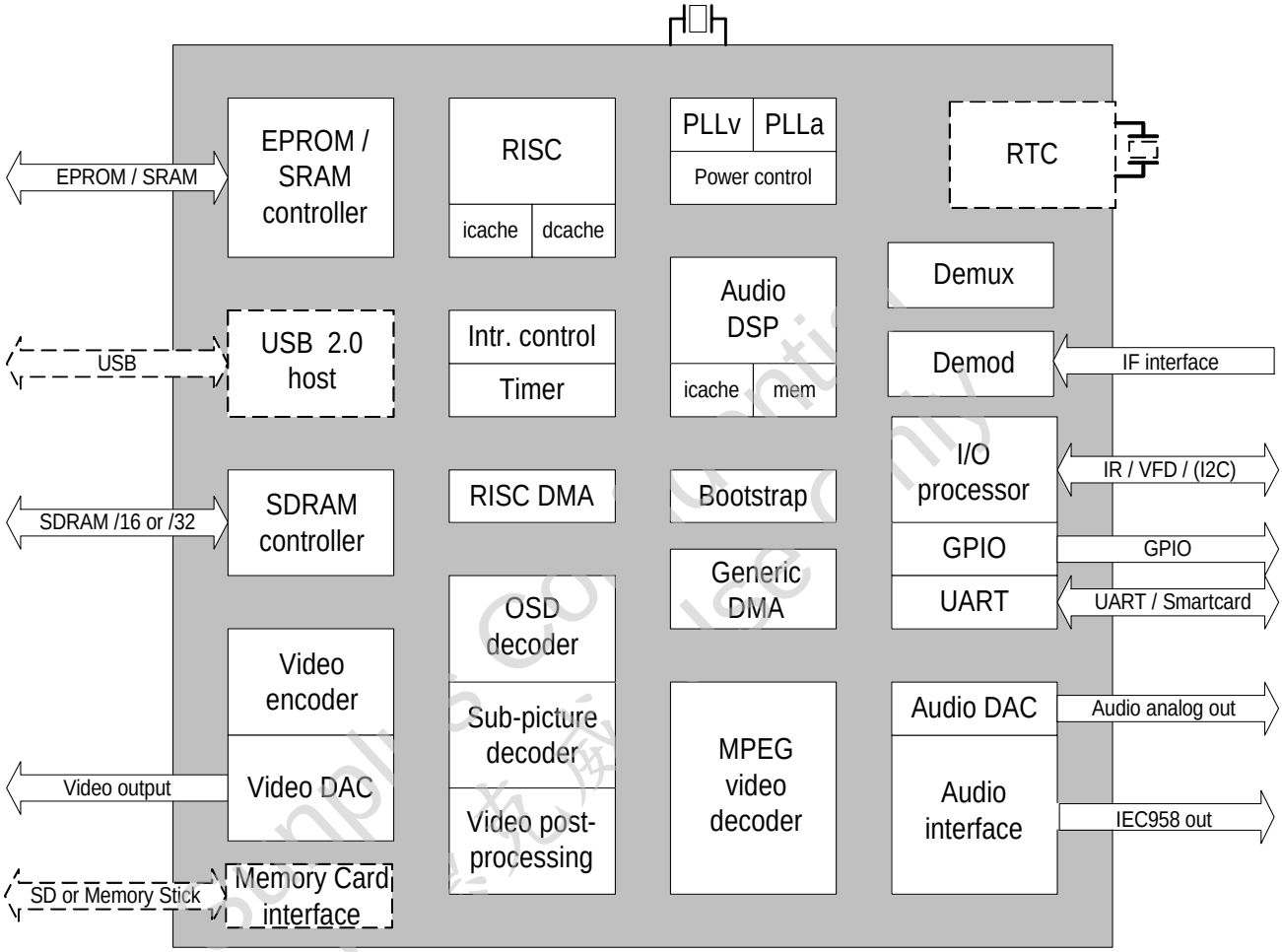
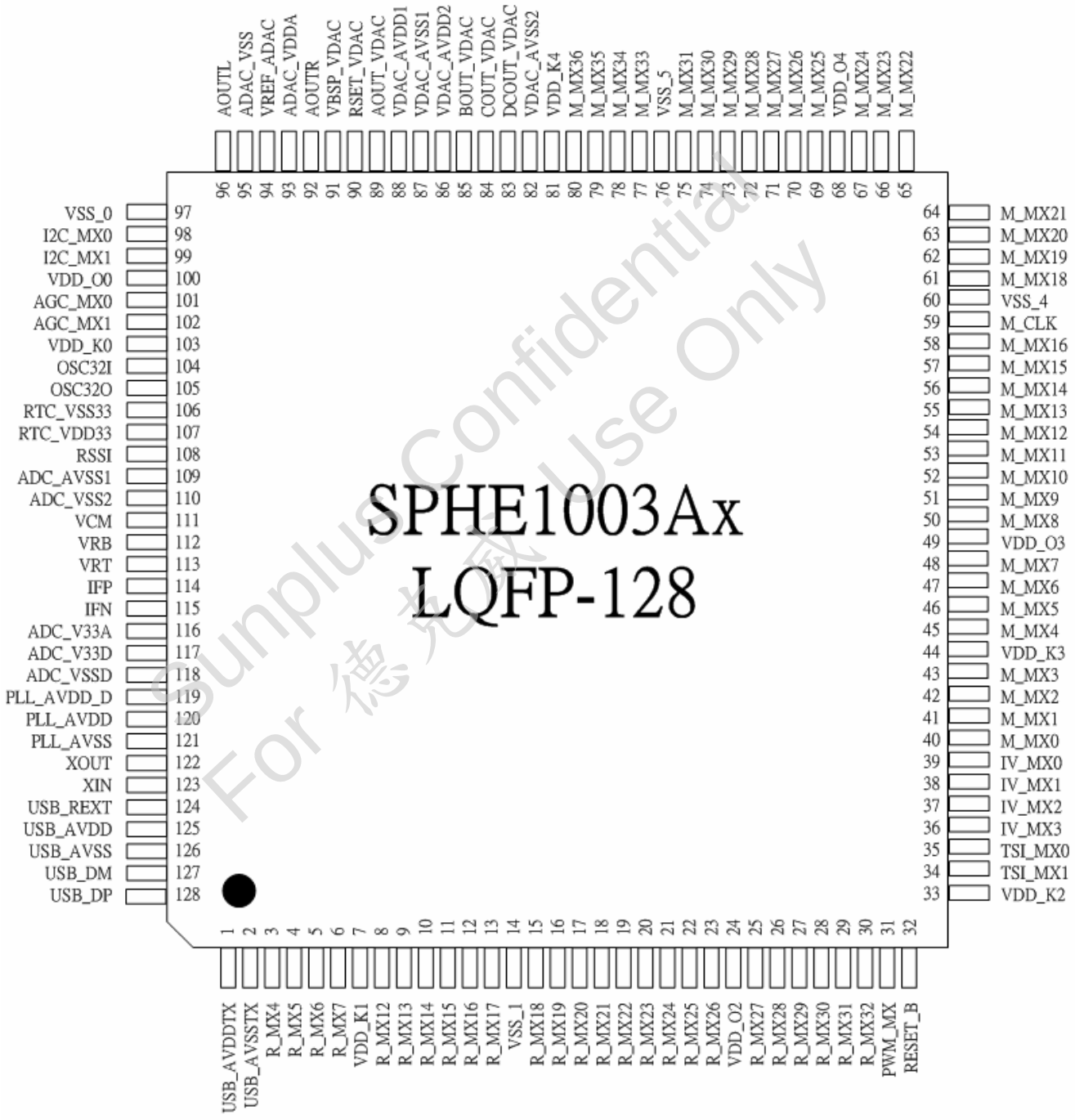


Figure 3-1: SPHE1003Ax block diagram

4.SIGNAL DESCRIPTION

4.1. Pin Configuration



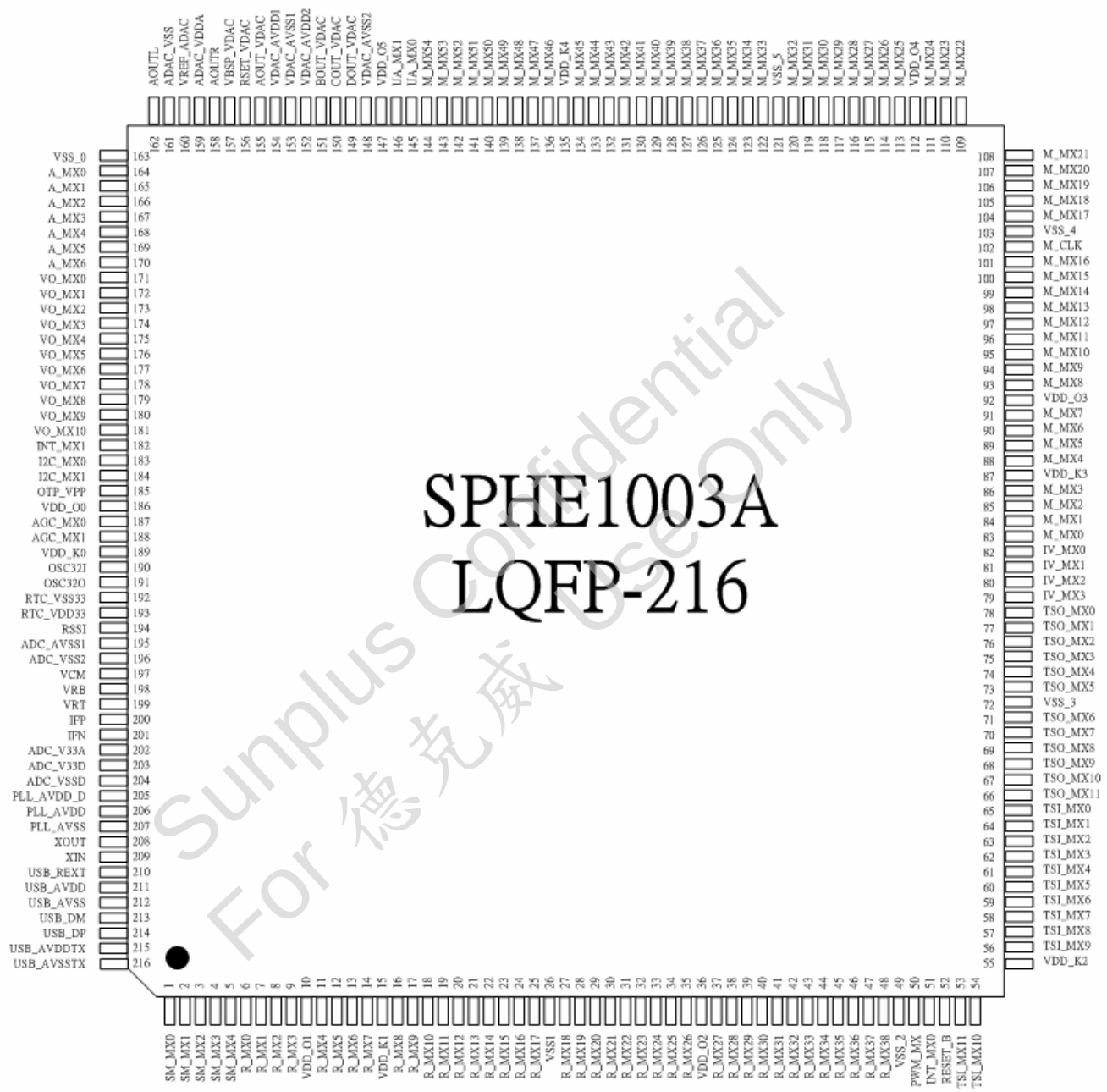


Figure 4-1: SPHE1003Ax Pin Configuration

4.2. Pin Description

LQFP-128:

Symbol	Pin #	I/O	Description
			BOTTOM
USB_AVDDTX	1	PWR	USB power for Tx
USB_AVSSTX	2	GND	USB ground for Tx
R_MX4	3	I/O	GPIO[9] / SMC_D[3] / TSI_CLK / VO656_CLK / VOSRGB_D[0]
R_MX5	4	I/O	GPIO[10] / SMC_D[2] / TSI_SYNC / VO656_D[0] / VOSRGB_D[1]
R_MX6	5	I/O	GPIO[11] / SMC_D[1] / TSI_DEN / VO656_D[1] / VOSRGB_D[2]
R_MX7	6	I/O	GPIO[12] / SMC_D[0] / TSI_D[7] / VO656_D[2] / VOSRGB_D[3]
VDD_K1	7	PWR	1.8V kernel power
R_MX12	8	I/O	GPIO[17] / SD_CLK / MS_CLK / SMC_WP_B / TSI_D[6] / VO656_D[3] / VOSRGB_D[4]
R_MX13	9	I/O	GPIO[18] / SD_CMD / MS_BS / SMC_WE_B / TSI_D[5] / VO656_D[4] / VOSRGB_D[5]
R_MX14	10	I/O	GPIO[19] / SD_D[0] / MS_D[0] / SMC_ALE / TSI_D[4] / VO656_D[5] / VOSRGB_D[6]
R_MX15	11	I/O	GPIO[20] / SD_D[1] / MS_D[1] / SMC_CLE / TSI_D[3] / VO656_D[6] / VOSRGB_D[7]
R_MX16	12	I/O	GPIO[21] / SD_D[2] / MS_D[2] / SMC_CE_B / TSI_D[2] / VO656_D[7] / VOSRGB_CLK
R_MX17	13	I/O	GPIO[22] / SD_D[3] / MS_D[3] / SMC_RE_B / TSI_D[1] / VOSRGB_DEN / HD_VCLK / VGA_CLK
VSS_1	14	GND	Ground for 1.8V and 3.3V
R_MX18	15	I/O	GPIO[23] / SMC_RDY / TV_VS
R_MX19	16	I/O	GPIO[24] / SMC_CE_B / SMC_ALE / TV_HS
R_MX20	17	I/O	GPIO[25] / SPI_CS_B[1] / SMC_CLE / TSI_ERR / SPDIF
R_MX21	18	O	SPI_CS_B[0] / SMC_CLE / TSI_ERR / SPDIF
R_MX22	19	I/O	SPI_D[0]
R_MX23	20	O	SPI_CLK
R_MX24	21	I/O	GPIO[26] / SPI_D[1]
R_MX25	22	I/O	GPIO[27] / SPI_D[2] / SMC_D[7]
R_MX26	23	I/O	GPIO[28] SPI_D[3] / SMC_D[6]
VDD_O2	24	PWR	3.3V I/O power
R_MX27	25	I/O	GPIO[29] / SD_CLK / MS_CLK / SMC_D[5] / TSI_CLK
R_MX28	26	I/O	GPIO[30] / SD_CMD / MS_BS / SMC_D[4] / TSI_SYNC
R_MX29	27	I/O	GPIO[31] / SD_D[0] / MS_D[0] / SMC_D[0] / TSI_DEN
R_MX30	28	I/O	GPIO[70] / SD_D[1] / MS_D[1] / SMC_D[2] / TSI_D[0]
R_MX31	29	I/O	GPIO[33] / SD_D[2] / MS_D[2] / SMC_D[1]
R_MX32	30	I/O	GPIO[34] / SD_D[3] / MS_D[3] / SMC_D[0]
PWM_MX	31	I/O	GPIO[41] / TSI_D[0] / SPDIF / HD_VCLK / VGA_CLK / PWM
RESET_B	32	I	Chip reset
			RIGHT
VDD_K2	33	PWD	1.8V kernel power
TSI_MX1	34	I/O	GPIO[53] / UA_TXD
TSI_MX0	35	I/O	GPIO[54] / UA_RXD
IV_MX3	36	I/O	GPIO[67] / SMC_CE_B
IV_MX2	37	I/O	GPIO[68] / SMC_WP_B
IV_MX1	38	I/O	GPIO[69] / SMC_WE_B / SPDIF
IV_MX0	39	I/O	GPIO[32] / IR
M_MX0	40	I/O	M_D[7]
M_MX1	41	I/O	M_D[6]

Symbol	Pin #	I/O	Description
M_MX2	42	I/O	M_D[5]
M_MX3	43	I/O	M_D[4]
VDD_K3	44	PWR	1.8V kernel power
M_MX4	45	I/O	M_D[3]
M_MX5	46	I/O	M_D[2]
M_MX6	47	I/O	M_D[1]
M_MX7	48	I/O	M_D[0]
VDD_O3	49	PWR	3.3V I/O power
M_MX8	50	I/O	GPIO[71] / M_D[15]
M_MX9	51	I/O	GPIO[72] / M_D[14]
M_MX10	52	I/O	GPIO[73] / M_D[13]
M_MX11	53	I/O	GPIO[74] / M_D[12]
M_MX12	54	I/O	GPIO[75] / M_D[11]
M_MX13	55	I/O	GPIO[76] / M_D[10]
M_MX14	56	I/O	GPIO[77] / M_D[9]
M_MX15	57	I/O	GPIO[78] / M_D[8]
M_MX16	58	O	M_DQM[1]
M_CLK	59	I/O	M_CLK
VSS_4	60	GND	Ground for 1.8V and 3.3V
M_MX18	61	O	M_A[11]
M_MX19	62	O	M_A[9]
M_MX20	63	O	M_A[8]
M_MX21	64	O	M_A[7]
			TOP
M_MX22	65	O	M_A[6]
M_MX23	66	O	M_A[5]
M_MX24	67	O	M_A[4]
VDD_O4	68	PWR	3.3V I/O power
M_MX25	69	O	M_A[3]
M_MX26	70	O	M_A[2]
M_MX27	71	O	M_A[1]
M_MX28	72	O	M_A[0]
M_MX29	73	O	M_A[10]
M_MX30	74	O	M_BA[1]
M_MX31	75	O	M_BA[0]
VSS_5	76	GND	Ground for 1.8V and 3.3V
M_MX33	77	O	M_RAS_B
M_MX34	78	O	M_CAS_B
M_MX35	79	O	M_WE_B
M_MX36	80	O	M_DQM[0]
VDD_K4	81	PWR	1.8V kernel power
VDAC_AVSS2	82	GND	Video DAC ground #2
DOUT_VDAC	83	ANG	Video DAC D-channel output
COUT_VDAC	84	ANG	Video DAC C-channel output
BOUT_VDAC	85	ANG	Video DAC B-channel output

Symbol	Pin #	I/O	Description
VDAC_AVDD2	86	PWR	Video DAC 3.3V power #2
VDAC_AVSS1	87	GND	Video DAC ground #1
VDAC_AVDD1	88	PWR	Video DAC 3.3V power #1
AOUT_VDAC	89	ANG	Video DAC A-channel output
RSET_VDAC	90	ANG	Video DAC RSET; full-scale adjust control pin
VBSP_VDAC	91	ANG	Video DAC VBSP; bias voltage
AOUT_R	92	ANG	Audio DAC right-channel analog output
AVDAC_VDDA	93	PWR	Audio DAC 3.3V power
VREF_ADAC	94	ANG	Audio DAC VREF
ADAC_VSS	95	GND	Audio DAC ground
AOUTL	96	ANG	Audio DAC left-channel analog output
			LEFT
VSS_0	97	GND	Ground for 1.8V and 3.3V
I2C_MX0	98	I/O	GPIO[120] / VO656_D[4]
I2C_MX1	99	I/O	GPIO[121] / VO656_D[5]
VDD_O0	100	PWR	3.3V I/O power
AGC_MX0	101	I/O	GPIO[122] / VO656_D[6]
AGC_MX1	102	I/O	GPIO[123] / VO656_D[7]
VDD_K0	103	PWR	1.8V kernel power
OSC32I	104	ANG	RTC oscillator input
OSC32O	105	ANG	RTC oscillator output
RTC_VSS33	106	GND	RTC ground
RTC_VDD33	107	PWR	RTC 3.3V power
RSSI	108	ANG	SAR ADC input
ADC_AVSS1	109	GND	ADC analog ground #1
ADC_VSS2	110	GND	ADC analog ground #2
VCM	111	ANG	ADC VCM; middle reference voltage
VRB	112	ANG	ADC VRB; minimum reference voltage
VRT	113	ANG	ADC VRT; maximum reference voltage
IFP	114	ANG	ADC analog input positive
IFN	115	ANG	ADC analog input negative
ADC_V33A	116	PWR	ADC 3.3V analog power
ADC_V33D	117	PWR	ADC 3.3V digital power
ADC_VSSD	118	GND	ADC digital ground
PLL_AVDD_D	119	PWR	PLL 3.3V power
PLL_AVDD	120	PWR	PLL 3.3V power
PLL_AVSS	121	GND	PLL ground
XOUT	122	ANG	27MHz crystal output
XIN	123	ANG	27MHz crystal input
USB_REXT	124	ANG	USB REXT; bias resistor
USB_AVDD	125	PWR	USB power
USB_AVSS	126	GND	USB ground
USB_DM	127	ANG	USB DM
USB_DP	128	ANG	USB DP

LQFP-216:

Symbol	Pin #	I/O	Description
			BOTTOM
SM_MX0	1	I/O	GPIO[0] / SM_IO
SM_MX1	2	I/O	GPIO[1] / SM_CLK
SM_MX2	3	I/O	GPIO[2] / SM_PRES
SM_MX3	4	I/O	GPIO[3] / SM_RST
SM_MX4	5	I/O	GPIO[4] / SM_VCCB
R_MX0	6	I/O	GPIO[5] / R_A[17] / CF_D[3] / SMC_D[7] / VORGB_G[0] / VO601_VS
R_MX1	7	I/O	GPIO[6] / R_A[19] / CF_D[11] / SMC_D[6] / VORGB_G[1] / VO601_HS
R_MX2	8	I/O	GPIO[7] / R_A[10] / CF_CS0_B / SMC_D[5] / VORGB_G[2] / VO601_Y[0]
R_MX3	9	I/O	GPIO[8] / R_D[7] / CF_CS1_B / SMC_D[4] / VORGB_G[3] / VO601_Y[1]
VDD_O1	10	PWR	3.3V I/O power
R_MX4	11	I/O	GPIO[9] / SMC_D[3] / TSI_CLK / VO656_CLK / VOSRGB_D[0]
R_MX5	12	I/O	GPIO[10] / SMC_D[2] / TSI_SYNC / VO656_D[0] / VOSRGB_D[1]
R_MX6	13	I/O	GPIO[11] / SMC_D[1] / TSI_DEN / VO656_D[1] / VOSRGB_D[2]
R_MX7	14	I/O	GPIO[12] / SMC_D[0] / TSI_D[7] / VO656_D[2] / VOSRGB_D[3]
VDD_K1	15	PWR	1.8V kernel power
R_MX8	16	I/O	GPIO[13] / R_D[2] / VORGB_B[0] / VO601_Y[6]
R_MX9	17	I/O	GPIO[14] / R_D[1] / VORGB_B[1] / VO601_Y[7]
R_MX10	18	I/O	GPIO[15] / R_D[0] / VORGB_B[2] / VO601_C[0]
R_MX11	19	I/O	GPIO[16] / R_OE_B / VORGB_B[3] / VO601_C[1]
R_MX12	20	I/O	GPIO[17] / SD_CLK / MS_CLK / SMC_WP_B / TSI_D[6] / VO656_D[3] / VOSRGB_D[4]
R_MX13	21	I/O	GPIO[18] / SD_CMD / MS_BS / SMC_WE_B / TSI_D[5] / VO656_D[4] / VOSRGB_D[5]
R_MX14	22	I/O	GPIO[19] / SD_D[0] / MS_D[0] / SMC_ALE / TSI_D[4] / VO656_D[5] / VOSRGB_D[6]
R_MX15	23	I/O	GPIO[20] / SD_D[1] / MS_D[1] / SMC_CLE / TSI_D[3] / VO656_D[6] / VOSRGB_D[7]
R_MX16	24	I/O	GPIO[21] / SD_D[2] / MS_D[2] / SMC_CE_B / TSI_D[2] / VO656_D[7] / VOSRGB_CLK
R_MX17	25	I/O	GPIO[22] / SD_D[3] / MS_D[3] / SMC_RE_B / TSI_D[1] / VOSRGB_DEN / HD_VCLK / VGA_CLK
VSS_1	26	GND	Ground for 1.8V and 3.3V
R_MX18	27	I/O	GPIO[23] / SMC_RDY / TV_VS
R_MX19	28	I/O	GPIO[24] / SMC_CE_B / SMC_ALE / TV_HS
R_MX20	29	I/O	GPIO[25] / SPI_CS_B[1] / SMC_CLE / TSI_ERR / SPDIF
R_MX21	30	O	SPI_CS_B[0] / SMC_CLE / TSI_ERR / SPDIF
R_MX22	31	I/O	SPI_D[0]
R_MX23	32	O	SPI_CLK
R_MX24	33	I/O	GPIO[26] / SPI_D[1]
R_MX25	34	I/O	GPIO[27] / SPI_D[2] / SMC_D[7]
R_MX26	35	I/O	GPIO[28] SPI_D[3] / SMC_D[6]
VDD_O2	36	PWR	3.3V I/O power
R_MX27	37	I/O	GPIO[29] / SD_CLK / MS_CLK / SMC_D[5] / TSI_CLK
R_MX28	38	I/O	GPIO[30] / SD_CMD / MS_BS / SMC_D[4] / TSI_SYNC
R_MX29	39	I/O	GPIO[31] / SD_D[0] / MS_D[0] / SMC_D[0] / TSI_DEN
R_MX30	40	I/O	GPIO[70] / SD_D[1] / MS_D[1] / SMC_D[2] / TSI_D[0]
R_MX31	41	I/O	GPIO[33] / SD_D[2] / MS_D[2] / SMC_D[1]
R_MX32	42	I/O	GPIO[34] / SD_D[3] / MS_D[3] / SMC_D[0]
R_MX33	43	I/O	GPIO[35] / R_A[14]

Symbol	Pin #	I/O	Description
R_MX34	44	I/O	GPIO[36] / R_A[15]
R_MX35	45	I/O	GPIO[37] / R_A[16]
R_MX36	46	I/O	GPIO[38] / R_PCMCIA_IOW_B / SMC_RE_B
R_MX37	47	I/O	GPIO[39] / R_PCMCIA_IOR_B / SMC_CE_B
R_MX38	48	I/O	GPIO[40] / R_PCMCIA_WAIT_B / SMC_WE_B
VSS_2	49	GND	Ground for 1.8V and 3.3V
PWM_MX	50	I/O	GPIO[41] / TSI_D[0] / SPDIF / HD_VCLK / VGA_CLK / PWM
INT_MX0	51	I/O	GPIO[42] / SMC_CE_B / INT0
RESET_B	52	I	Chip reset
TSI_MX11	53	I/O	GPIO[43] / CF_D[1] / SMC_CLE / TSI_ERR / HD_VCLK / VGA_CLK
TSI_MX10	54	I/O	GPIO[44] / CF_D[2] / SMC_ALE / TSI_CLK / TSI_CLK
RIGHT			
VDD_K2	55	PWD	1.8V kernel power
TSI_MX9	56	I/O	GPIO[45] / CF_D[3] / SMC_WP_B / TSI_SYNC
TSI_MX8	57	I/O	GPIO[46] / CF_D[4] / SMC_D[0] / TSI_DEN
TSI_MX7	58	I/O	GPIO[47] / CF_D[5] / SMC_D[1] / TSI_D[7]
TSI_MX6	59	I/O	GPIO[48] / CF_D[6] / SMC_D[2] / TSI_D[6]
TSI_MX5	60	I/O	GPIO[49] / CF_D[7] / SMC_D[3] / TSI_D[5]
TSI_MX4	61	I/O	GPIO[50] / CF_D[8] / SMC_D[4] / TSI_D[4]
TSI_MX3	62	I/O	GPIO[51] / CF_D[9] / SMC_D[5] / TSI_D[3]
TSI_MX2	63	I/O	GPIO[52] / CF_D[10] / SMC_D[6] / TSI_D[2]
TSI_MX1	64	I/O	GPIO[53] / UA_TXD
TSI_MX0	65	I/O	GPIO[54] / UA_RXD
TSO_MX11	66	I/O	GPIO[55] / CF_D[13] / TSO_ERR / HD_VCLK / VGA_CLK
TSO_MX10	67	I/O	GPIO[56] / CF_D[14] / TSO_CLK
TSO_MX9	68	I/O	GPIO[57] / CF_D[15] / TSO_SYNC
TSO_MX8	69	I/O	GPIO[58] / CF_A[0] / TSO_DEN
TSO_MX7	70	I/O	GPIO[59] / CF_A[1] / TSO_D[7]
TSO_MX6	71	I/O	GPIO[60] / CF_A[2] / TSO_D[6]
VSS_3	72	GND	Ground for 1.8V and 3.3V
TSO_MX5	73	I/O	GPIO[61] / CF_IOW_B / TSO_D[5]
TSO_MX4	74	I/O	GPIO[62] / CF_IOR_B / TSO_D[4]
TSO_MX3	75	I/O	GPIO[63] / CF_IORDY / TSO_D[3]
TSO_MX2	76	I/O	GPIO[64] / CF_CS0_B / TSO_D[2]
TSO_MX1	77	I/O	GPIO[65] / CF_CS1_B / TSO_D[1]
TSO_MX0	78	I/O	GPIO[66] / CF_RST_B / TSO_D[0]
IV_MX3	79	I/O	GPIO[67] / SMC_CE_B
IV_MX2	80	I/O	GPIO[68] / SMC_WP_B
IV_MX1	81	I/O	GPIO[69] / SMC_WE_B / SPDIF
IV_MX0	82	I/O	GPIO[32] / IR
M_MX0	83	I/O	M_D[7]
M_MX1	84	I/O	M_D[6]
M_MX2	85	I/O	M_D[5]
M_MX3	86	I/O	M_D[4]
VDD_K3	87	PWR	1.8V kernel power

Symbol	Pin #	I/O	Description
M_MX4	88	I/O	M_D[3]
M_MX5	89	I/O	M_D[2]
M_MX6	90	I/O	M_D[1]
M_MX7	91	I/O	M_D[0]
VDD_O3	92	PWR	3.3V I/O power
M_MX8	93	I/O	GPIO[71] / M_D[15]
M_MX9	94	I/O	GPIO[72] / M_D[14]
M_MX10	95	I/O	GPIO[73] / M_D[13]
M_MX11	96	I/O	GPIO[74] / M_D[12]
M_MX12	97	I/O	GPIO[75] / M_D[11]
M_MX13	98	I/O	GPIO[76] / M_D[10]
M_MX14	99	I/O	GPIO[77] / M_D[9]
M_MX15	100	I/O	GPIO[78] / M_D[8]
M_MX16	101	O	M_DQM[1]
M_CLK	102	I/O	M_CLK
VSS_4	103	GND	Ground for 1.8V and 3.3V
M_MX17	104	I/O	GPIO[79] / M_CKE
M_MX18	105	O	M_A[11]
M_MX19	106	O	M_A[9]
M_MX20	107	O	M_A[8]
M_MX21	108	O	M_A[7]
TOP			
M_MX22	109	O	M_A[6]
M_MX23	110	O	M_A[5]
M_MX24	111	O	M_A[4]
VDD_O4	112	PWR	3.3V I/O power
M_MX25	113	O	M_A[3]
M_MX26	114	O	M_A[2]
M_MX27	115	O	M_A[1]
M_MX28	116	O	M_A[0]
M_MX29	117	O	M_A[10]
M_MX30	118	O	M_BA[1]
M_MX31	119	O	M_BA[0]
M_MX32	120	I/O	GPIO[80] / M_CS_B
VSS_5	121	GND	Ground for 1.8V and 3.3V
M_MX33	122	O	M_RAS_B
M_MX34	123	O	M_CAS_B
M_MX35	124	O	M_WE_B
M_MX36	125	O	M_DQM[0]
M_MX37	126	I/O	GPIO[81] / M_DQM[2]
M_MX38	127	I/O	GPIO[82] / M_D[23]
M_MX39	128	I/O	GPIO[83] / M_D[22]
M_MX40	129	I/O	GPIO[84] / M_D[21]
M_MX41	130	I/O	GPIO[85] / M_D[20]
M_MX42	131	I/O	GPIO[86] / M_D[19]

Symbol	Pin #	I/O	Description
M_MX43	132	I/O	GPIO[87] / M_D[18]
M_MX44	133	I/O	GPIO[88] / M_D[17]
M_MX45	134	I/O	GPIO[89] / M_D[16]
VDD_K4	135	PWR	1.8V kernel power
M_MX46	136	I/O	GPIO[90] / M_D[31]
M_MX47	137	I/O	GPIO[91] / M_D[30]
M_MX48	138	I/O	GPIO[92] / M_D[29] / SD_CLK / MS_CLK
M_MX49	139	I/O	GPIO[93] / M_D[28] / SD_CMD / MS_BS
M_MX50	140	I/O	GPIO[94] / M_D[27] / SD_D[0] / MS_D[0]
M_MX51	141	I/O	GPIO[95] / M_D[26] / SD_D[1] / MS_D[1] / CF_D[1]
M_MX52	142	I/O	GPIO[96] / M_D[25] / SD_D[2] / MS_D[2] / CF_D[8]
M_MX53	143	I/O	GPIO[97] / M_D[24] / SD_D[3] / MS_D[3] CF_D[2]
M_MX54	144	I/O	GPIO[98] / M_DQM[3]
UA_MX0	145	I/O	GPIO[99] / CF_D[9] / TV_VS_PC / UA_TXD
UA_MX1	146	I/O	GPIO[100] / CF_D[10] / TV_HS_PC / UA_RXD
VDD_O5	147	I/O	3.3V I/O power
VDAC_AVSS2	148	GND	Video DAC ground #2
DOUT_VDAC	149	ANG	Video DAC D-channel output
COUT_VDAC	150	ANG	Video DAC C-channel output
BOUT_VDAC	151	ANG	Video DAC B-channel output
VDAC_AVDD2	152	PWR	Video DAC 3.3V power #2
VDAC_AVSS1	153	GND	Video DAC ground #1
VDAC_AVDD1	154	PWR	Video DAC 3.3V power #1
AOUT_VDAC	155	ANG	Video DAC A-channel output
RSET_VDAC	156	ANG	Video DAC RSET; full-scale adjust control pin
VBSP_VDAC	157	ANG	Video DAC VBSP; bias voltage
AOUT_R	158	ANG	Audio DAC right-channel analog output
AVDAC_VDDA	159	PWR	Audio DAC 3.3V power
VREF_ADAC	160	ANG	Audio DAC VREF
ADAC_VSS	161	GND	Audio DAC ground
AOUTL	162	ANG	Audio DAC left-channel analog output
LEFT			
VSS_0	163	GND	Ground for 1.8V and 3.3V
A_MX0	164	I/O	GPIO[101] / SPDIF
A_MX1	165	I/O	GPIO[102] / SD_CLK / MS_CLK / I2SO_D[0]
A_MX2	166	I/O	GPIO[103] / SD_CMD / MS_BS / I2SO_D[1]
A_MX3	167	I/O	GPIO[104] / SD_D[0] / MS_D[0] / I2SO_D[2]
A_MX4	168	I/O	GPIO[105] / SD_D[1] / MS_D[1] / I2SO_LRCK
A_MX5	169	I/O	GPIO[106] / SD_D[2] / MS_D[2] / I2SO_BCK
A_MX6	170	I/O	GPIO[107] / SD_D[3] / MS_D[3] / I2S_XCK
VO_MX0	171	I/O	GPIO[108] / TV_VS / UA_TXD
VO_MX1	172	I/O	GPIO[109] / TV_HS / UA_RXD
VO_MX2	173	I/O	GPIO[110] / VO656_CLK / VOSRGB_D[0] / VORGB_R[0]
VO_MX3	174	I/O	GPIO[111] / VO4B656_D[0] / VO656_D[0] / VOSRGB_D[1] / VORGB_R[1]
VO_MX4	175	I/O	GPIO[112] / VO4B656_D[1] / VO656_D[1] / VOSRGB_D[2] / VORGB_R[2]

Symbol	Pin #	I/O	Description
VO_MX5	176	I/O	GPIO[113] / VO4B656_D[2] / VO656_D[2] / VOSRGB_D[3] / VORGB_R[3]
VO_MX6	177	I/O	GPIO[114] / VO4B656_D[3] / VO656_D[3] / VOSRGB_D[4] / VORGB_R[4]
VO_MX7	178	I/O	GPIO[115] / VO656_D[4] / VOSRGB_D[5] / VORGB_R[5]
VO_MX8	179	I/O	GPIO[116] / VO656_D[5] / VOSRGB_D[6] / VORGB_REXT[0]
VO_MX9	180	I/O	GPIO[117] / VO656_D[6] / VOSRGB_D[7] / VORGB_REXT[1]
VO_MX10	181	I/O	GPIO[118] / VO656_D[7] / VOSRGB_CLK / VORGB_CLK
VO_MX11	182	I/O	GPIO[119] / VOSRGB_DEN
I2C_MX0	183	I/O	GPIO[120] / VO656_D[4]
I2C_MX1	184	I/O	GPIO[121] / VO656_D[5]
OTP_VPP	185	PWR	OTP programming power
VDD_O0	186	PWR	3.3V I/O power
AGC_MX0	187	I/O	GPIO[122] / VO656_D[6]
AGC_MX1	188	I/O	GPIO[123] / VO656_D[7]
VDD_K0	189	PWR	1.8V kernel power
OSC32I	190	ANG	RTC oscillator input
OSC32O	191	ANG	RTC oscillator output
RTC_VSS33	192	GND	RTC ground
RTC_VDD33	193	PWR	RTC 3.3V power
RSSI	194	ANG	SAR ADC input
ADC_AVSS1	195	GND	ADC analog ground #1
ADC_VSS2	196	GND	ADC analog ground #2
VCM	197	ANG	ADC VCM; middle reference voltage
VRB	198	ANG	ADC VRB; minimum reference voltage
VRT	199	ANG	ADC VRT; maximum reference voltage
IFP	200	ANG	ADC analog input positive
IFN	201	ANG	ADC analog input negative
ADC_V33A	202	PWR	ADC 3.3V analog power
ADC_V33D	203	PWR	ADC 3.3V digital power
ADC_VSSD	204	GND	ADC digital ground
PLL_AVDD_D	205	PWR	PLL 3.3V power
PLL_AVDD	206	PWR	PLL 3.3V power
PLL_AVSS	207	GND	PLL ground
XOUT	208	ANG	27MHz crystal output
XIN	209	ANG	27MHz crystal input
USB_REXT	210	ANG	USB REXT; bias resistor
USB_AVDD	211	PWR	USB power
USB_AVSS	212	GND	USB ground
USB_DM	213	ANG	USB DM
USB_DP	214	ANG	USB DP
USB_AVDDTX	215	PWR	USB power for Tx
USB_AVSSTX	216	GND	USB ground for Tx

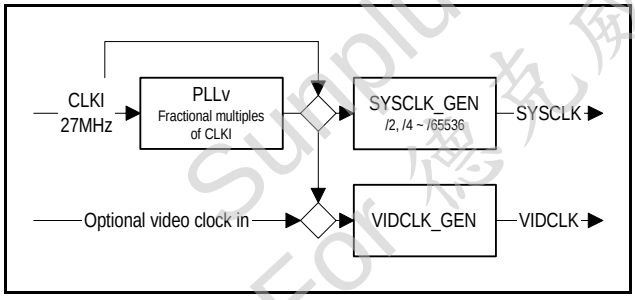
5.FUNCTIONAL DESCRIPTIONS

SPHE1003Ax integrates a MPEG-2 Transport Demultiplexer, a MPEG-1/-2/-4 A/V decoding engine, a 2-channel audio DAC and a 4-channel multi-format TV-encoder.

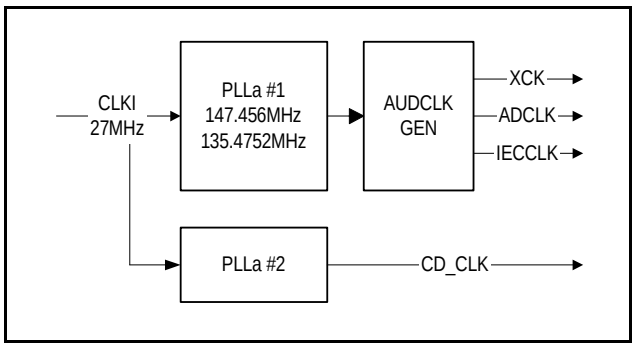
SPHE1003Ax performs real-time PID filtering, decode and playback of MPEG-1 and MPEG-2 A/V from Terrestrial Broadcasting. MPEG-1, MPEG-2, and MPEG-4 can be real time decode and playback from SD/ MMC/ Memory Stick/ Memory Stick Pro memory card or USB2.0 Mass Storage Device inputs by SPHE1003Ax. For audio it supports MPEGI/II Layer1/2/3, PCM, LPCM audio playback. The TV-encoder support CVBS, S-video, Component YCbCr.

5.1. PLL and ClockGen

SPHE1003Ax contains multiple PLLs to generate system clock and audio reference clocks. All the PLLs reference a single external 27MHz clock or crystal to generate the required clocks. System clock is then derived from division of the system PLL output.



PLLa supports two center frequencies (for both 48kHz family and 44.1kHz family) and generates required audio clocks from the audio system clock.



5.2. Power Control

SPHE1003Ax provides various levels of power-control mechanism in order to achieve minimum power consumption.

- Automatic power-save:
  Most hardware modules are automatically power-saved when not operating.
- Module-level stop-operation:
  SPHE1003Ax provides a function to turn off specific module from operating. Without explicit wake-up, the hardware module will remain static and consume little power.
- System-level doze:
  For maximum power-saving, firmware could fine-tune system performance according to system task.

5.3. Embedded 32-bit RISC Controller

SPHE1003Ax includes a powerful 32-bit RISC processor as the host controller. This host controller is utilized to parse MPEG-2 transport stream (TS), decoding tasks as well as UI tasks. It can access to all the memory and devices, cooperate between processor systems. Audio decoder and I/O processor handshake with RISC processor through the mailbox registers.

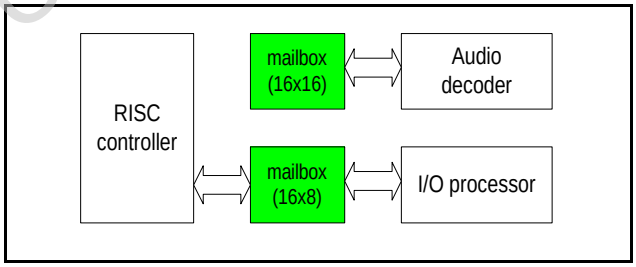


Figure 5-1: Communication between processors

The RISC processor is equipped with instruction and data caches. These caches can accelerate accesses to the SDRAM or ROM cacheable regions.

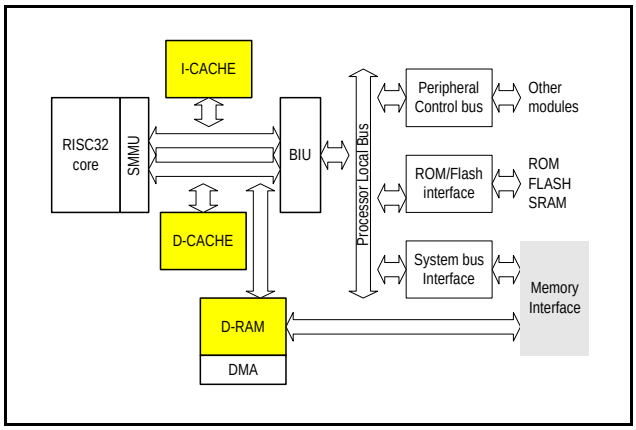


Figure 5-2: RISC subsystem

Table: RISC processor local memory configuration

Memory	Specification
I-Cache	8kbyte (2-way set associated)
D-Cache	4kbyte (2-way set associated, write back)
D-RAM/DMA	4kbyte scratch buffer

SDRAM, ROM and other devices are mapped to RISC memory spaces as in the following table:

Table: RISC memory mapping

Memory Range	Description
8000_0000~87ff_ffff	SDRAM (cached)
a000_0000~a7ff_ffff	SDRAM (uncached)
8800_0000~8fff_ffff	ROM/FLASH/SRAM (cached)
a800_0000~afff_ffff	ROM/FLASH/SRAM (uncached)
bffe_8000~bffe_ffff	Peripheral control registers
bfff_0000~bfff_0fff	DMA buffer

SPHE1003Ax includes following dedicated RISC peripherals to assist the system tasks:

- Device interrupt controller:
  Device interrupt controller takes care of interrupt sources from on-chip devices and off chip sources. For each interrupt source the firmware is able to configure the interrupt behavior between edge-trigger and level-sensitive mode.
- Watchdog:
  Watchdog keeps monitoring RISC behavior and whenever firmware is in a deadlock or ill-behaved, the watchdog would trigger system-wise reset and keep the application functioning continuously.
- Timers
  There are 4-channel timers and 2 cascade counters for timed tasks. During A/V decoding, system time counters are utilized to synchronize audio and video playback timing.

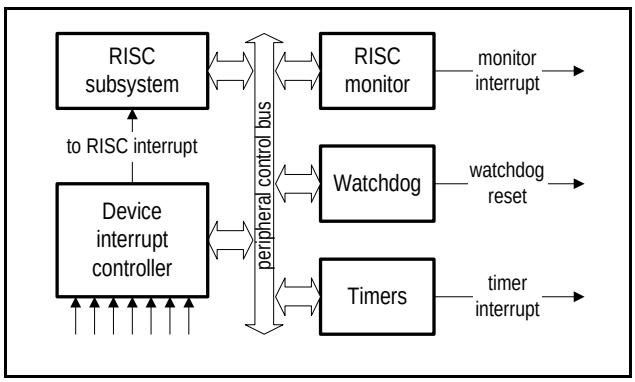


Figure 5-3: RISC dedicated hardware

Table: Device interrupt controller sources

Symbol	Description
INT_WDOG	Watchdog interrupt (if reset disabled)
INT_VSYNC	Interrupt when enter vertical resync
INT_FLD_SYNC	Interrupt when leave active region
INT_TIMER0	Timer 0 interrupt
INT_TIMER1	Timer 1 interrupt
INT_TIMER2A	Timer 2 scale interrupt
INT_TIMER2B	Timer 2 count interrupt
INT_TIMER3A	Timer 3 scale interrupt
INT_TIMER3B	Timer 3 count interrupt
INT_TIMERW	Watchdog timer interrupt
INT_UART0	UART0 interrupt
INT_VDP0	Video decoder interrupt
INT_DSP	DSP interrupt
INT_EXT0	External interrupt #0
INT_EXT1	External interrupt #1
INT_DEMUX	Demux status interrupt
INT_IOP	IOP interrupt
INT_AUD	Audio hardware interrupt

5.4. ROM/Flash/SRAM Controller

The SPHE1003Ax provides flexible connections to external ROM, Flash or SRAM (RFS). The firmware can configure RFS memory anchor registers and map these devices into locations of RISC memory space. The SPHE1003AX supports either the address/data separated 8-bit parallel ROM/FLASH interface or the address/data multiplexed SPI and 2-bit called serial flash interface. One of these modes is automatically detected after power on reset.

In parallel FLASH mode the access timing is decided by wait-state setting as in Figure 5-5.

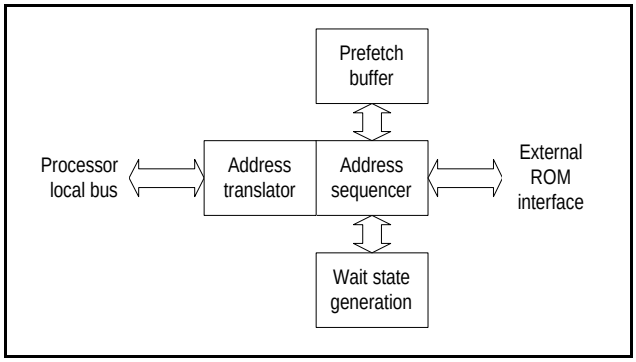


Figure 5-4: ROM/FLASH/SRAM controller

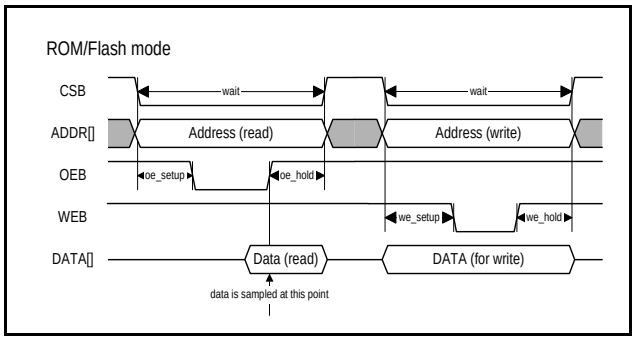


Figure 5-5: ROM/FLASH/SRAM mode timing

In serial flash modes, the pin outs and the timing diagram of the supported commodity flashes are depicted in Figure 5-5-1 through Figure 5-5-4.

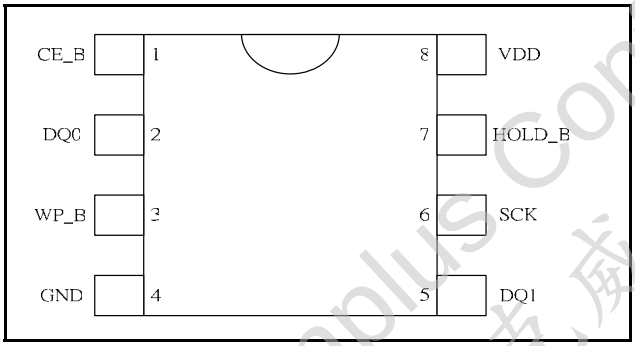


Figure 5-5-1: The pin out of SPI flash

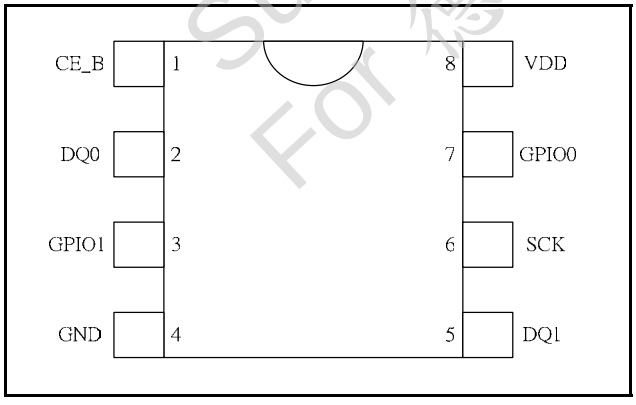


Figure 5-5-2: The pin out of 2-bit serial flash

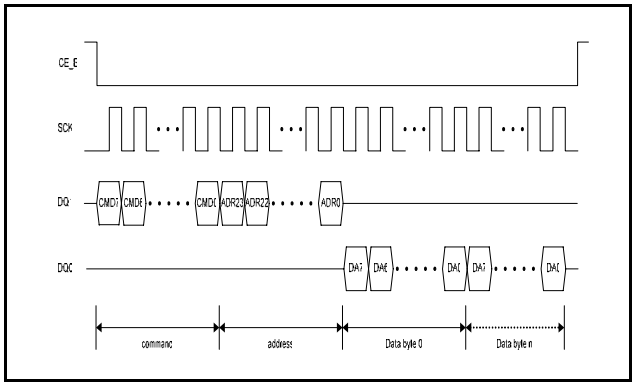


Figure 5-5-3: The timing diagram of SPI flash

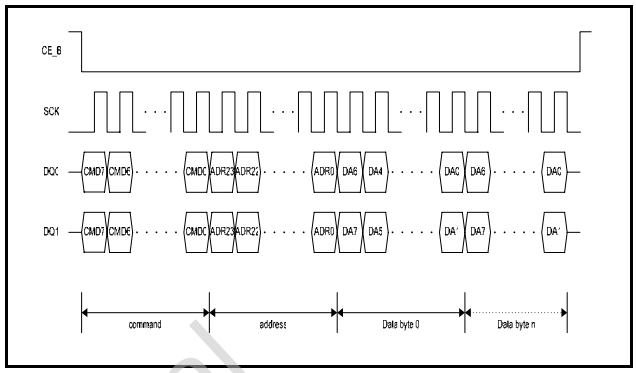


Figure 5-5-4: The timing diagram of 2-bit serial flash

5.5. DVB Demultiplexer

- Parallel or serial transport stream interface
- 32 programmable PID filters
  - One video PID
  - One audio PID
  - 30 general purpose PIDs for generic section or private PES data
- Provides PCR recovery
- MPEG-2 ISO/IEC 13818-1 compliant

5.6. MPEG Video Decoder

The system incorporates a powerful MPEG video decoding data path and provides real-time video decoding of MPEGI/II bit-stream.

The video decoder is a hardwired MPEG-1/-2/-4 decoding data path. The system architecture is as in the figure. RISC controller is in charge of pre-process and buffering source into SDRAM buffers. Upon correct timing video decoder will start to decode the bit-stream and write back reconstructed video frame for playback.

Moreover, SPHE1003Ax has the hardware JPEG accelerator to shorten the JPEG decoding time. This feature is helpful to show large photos.

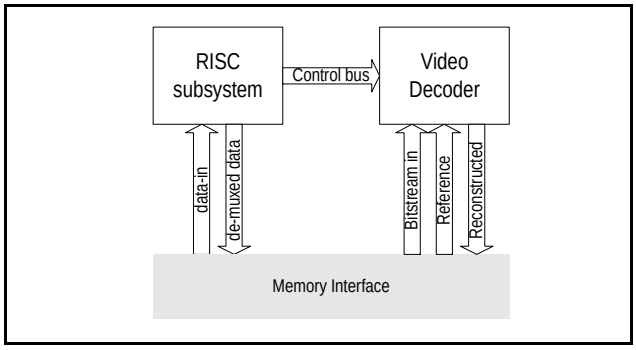


Figure 5-6: Interface between RISC and Video decoder

Advanced video decoding and display control mechanism is included to prevent tearing effect.

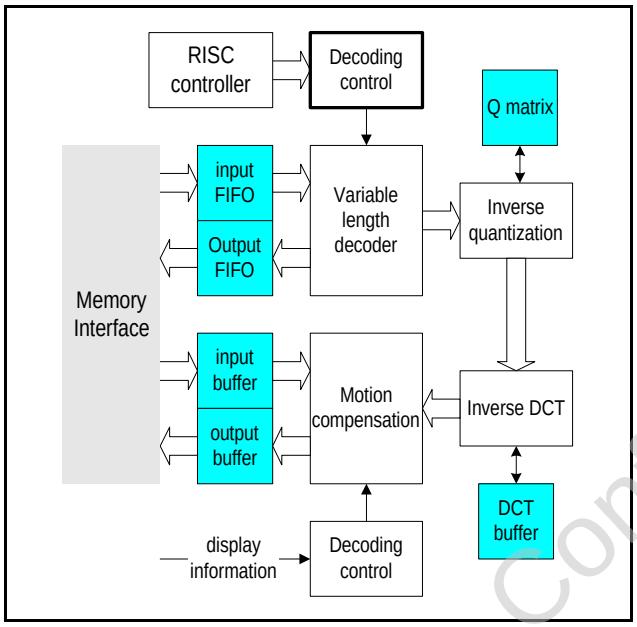


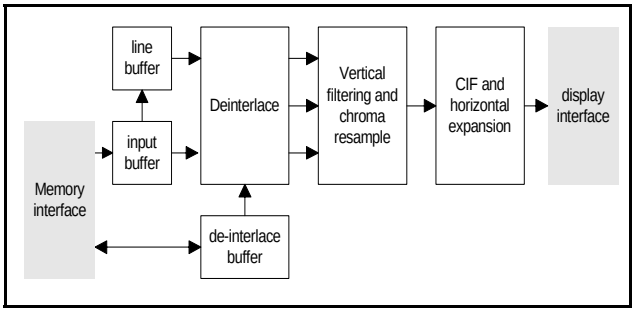
Figure 5-7: Architecture of video decoding pipeline

5.7. Video Post Processing

SPHE1003Ax includes powerful video-post-processing facilities to provide high video quality. It perform following functions:

- YUV411, YUV420, YUV422 and 8-bit indexed color
- SIF to CCIR601 interpolation
- MPEG1 CIF filter
- MPEG1/2 chroma vertical interpolation
- Up to 1/2x horizontal decimation
- Up to 1/512x vertical decimation
- Up to 1024x horizontal and vertical expansion
- Powerful de-interlacing hardware
- Pan and scan function
- De-flicker during interlaced display
- Video contrast/bright/color enhancement

During runtime video post-processing hardware will fetch video sources from frame buffer and process the data as in the following figure Figure 5-8.



5.8. Programmable Audio Decoder

The SPHE1003Ax contains a high-performance 24-bit audio DSP optimized for embedded system applications. This audio DSP processor can fetch operands from two memories and perform multiplication-and-accumulation (MAC) in one cycle. During execution the DSP fetches instruction from main-memory or IROM, at the same time the ICACHE will store the LRU instructions. Data are loaded from and to main-memory by the cycle-stealing DMA channels.

The DSP works closely with RISC processors by using mailbox registers or shared-memory protocol. When downloaded with different firmware the DSP could support multi-standard audio and act as an accelerator for RISC in some case.

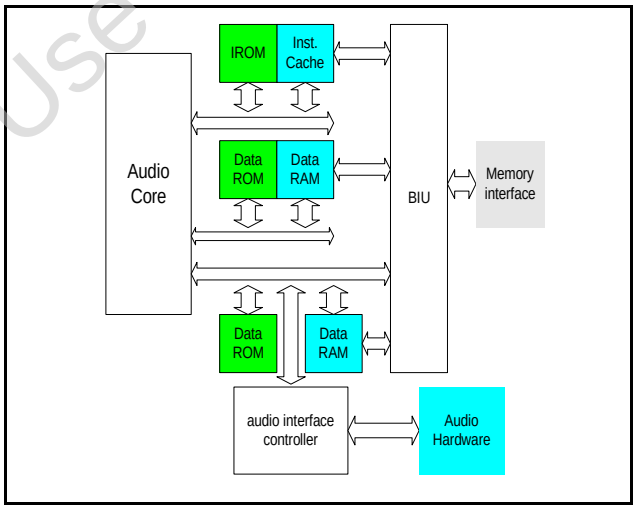


Figure 5-9: Audio DSP architecture

5.9. Audio Interface

The audio interface is in charge of servicing DSP and maintaining all audio-related tasks. It would buffer the audio PCM samples and format them to audio DAC and SPDIF formats. Up to 8 channel of digital audio are supported in I2S or normal mode.

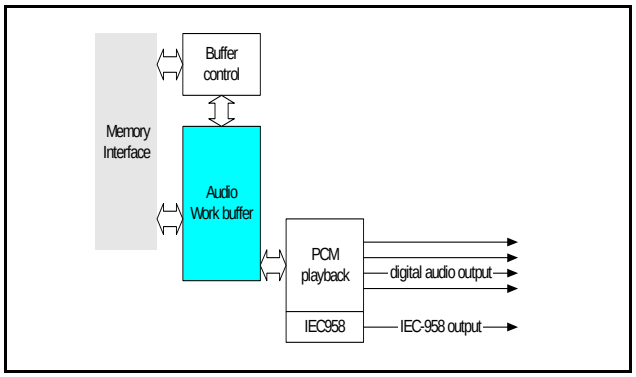


Figure 5-10: Audio Interface architecture

SPHE1003Ax support following audio DAC format combinations:

	32k	44.1k	48k	64k	88.2k	96k	192k
256fs	Ok	Ok	Ok	Ok	Ok	Ok	Ok
384fs	Ok	Ok	Ok	Ok	Ok	Ok	Ok

Data alignment	Left adjust, I2S, normal format
LRCK frame width	16b, 24b, 32b, 64b
Data bits	16b, 18b, 20b, 24b
Data sign extension	Zero-extended, sign-extended

5.10. Audio DAC

SPHE1003Ax includes a 2-channel 24-bit audio quality DAC for a minimum DVB system.

5.11. I/O Processor

The SPHE1003Ax includes an 8-bit micro-controller to help host controller handling I/O jobs. IR, VFD and other slow devices can be interfaced using this I/O processor.

5.12. SDRAM Controller

SDRAM controller in SPHE1003Ax is designed to meet both flexible and powerful requirements. It can be programmed to use 1Mx16 and 4Mx16 SDRAM chips. For different grade of memory chips it can support flexible timing select to meet different SDRAM timing requirements while achieving maximum performance. The actual speed of SDRAM interface depends on the system configuration.

SPHE1003Ax supports SDRAM power-down modes to save dynamic operating power.

5.13. On Screen Display

The on screen display (OSD) function of the SPHE1003Ax provides an overlay bitmap graphics on the final TV display. Applications can use this function to display specific information over the video display plane without operating on the video source.

The SPHE1003Ax can display multiple OSD regions on a single display frame, where every OSD regions can be in different size, location and color format. The OSD hardware supports 2, 4, 16, 256 indexed color or 16-bit direct color. OSD regions are stored in main memory before display. During display, OSD decoder would read these header and data and interpret to be a graphic data that overlay with video to be output to the display interface.

5.14. Display Interface

The display interface of SPHE1003Ax mixes the video content generated from video-post-processing, sub-picture-decoder and on-screen-display modules. It also performs content cropping, underflow and overflow correction and overall hue / brightness / contrast adjustment.

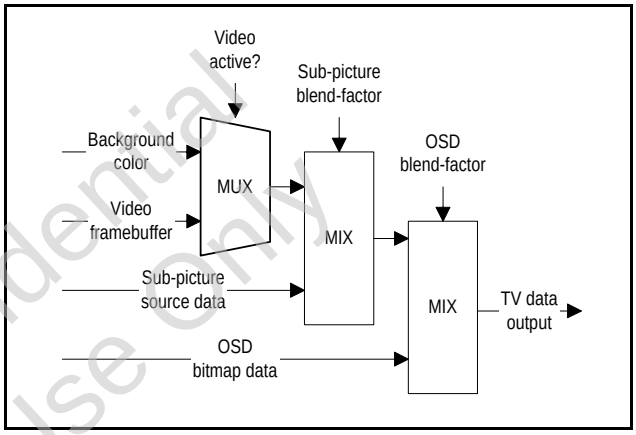


Figure 5-12: Display pipeline

The video enhancement process is show in following figure:

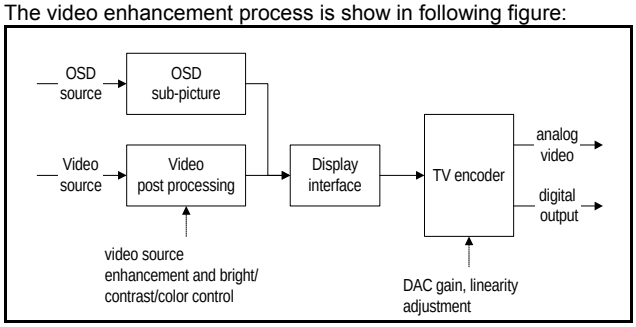


Figure 5-13: Display pipeline

5.15. Video DAC

SPHE1003Ax integrates 4-channel 10-bit high-speed current source DACs operating from 27MHz to 108MHz. These DAC outputs can drive a 37.5-Ohm load directly. Quarter current mode is provided for low power operation using external current amplifiers.

5.16. GPIO

In SPHE1003Ax almost every pin that related to selectable features can serve as general-purpose input-output (GPIO) control function. When a pin is programmed to this mode, the RISC controller or the I/O processor can take full control over the direction and output level by simple firmware programming.

5.17. UART

SPHE1003Ax provides one UART channel for debugging, firmware upgrading and other user applications. This UART can support standard serial port baud-rate and formats.

6.ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}	-0.3 to 5.5	V
Voltage on V_{DDIO} supply relative to V_{SS}	V_{DDIO}	-0.3 to 3.45	V
Voltage on V_{DDK} supply relative to V_{SS}	V_{DDK}	-0.3 to 1.90	V
Storage Temperature	T_{STG}	-55 to 150	°C
Soldering Temp. (Max. Time)	T_{SOLDER}	240 (for 5 Sec. Max.)	°C
Short circuit current	I_{OS}	50	mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6.2. DC Operating Conditions

Recommended Operating Conditions (Voltage referenced to VSS=0V, TA=-0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Units
Voltage on V_{DDK} supply relative to V_{SS}	V_{DDK}	1.70	1.80	1.90	V
Voltage on V_{DDIO} supply relative to V_{SS}	V_{DDIO}	3.15	3.30	3.45	V
Input logic high voltage	V_{IH}	2.0	-	5.5	V
Input logic low voltage	V_{IL}	-0.3	-	0.8	V
Output logic high voltage	V_{OH}	2.4	-	-	V
Output logic low voltage	V_{OL}	-	-	0.4	V
Input leakage current	I_L	-10	-	10	uA

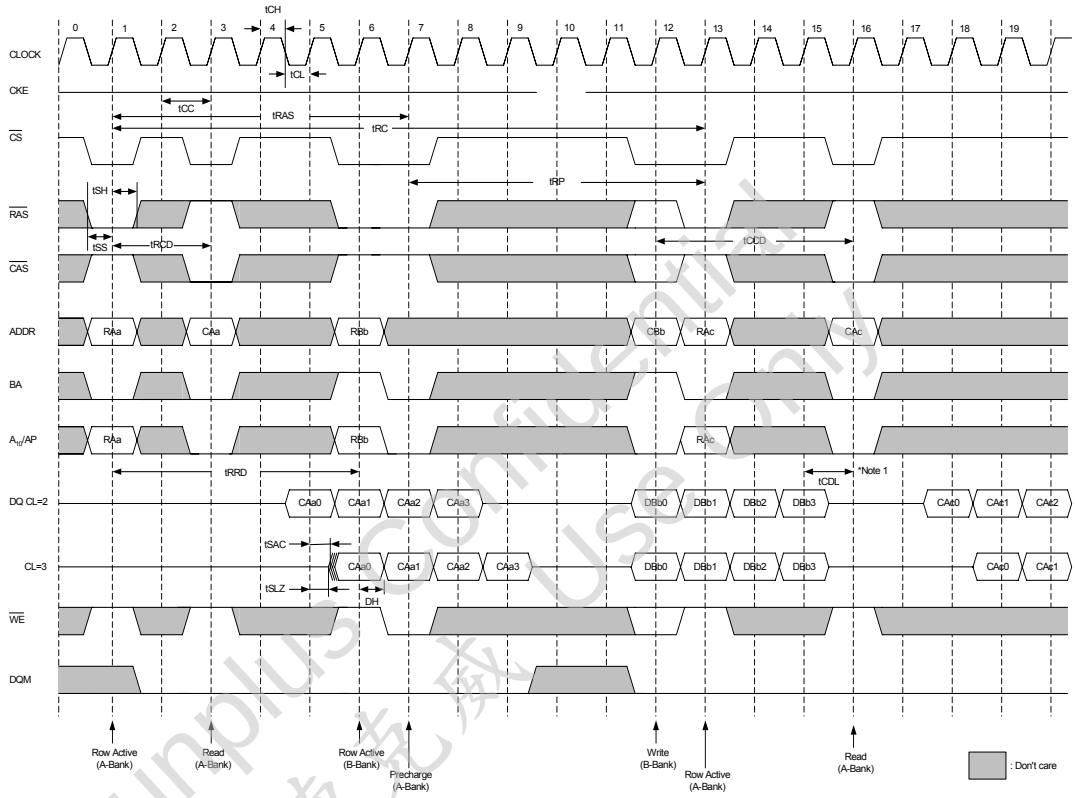
6.3. Capacitance

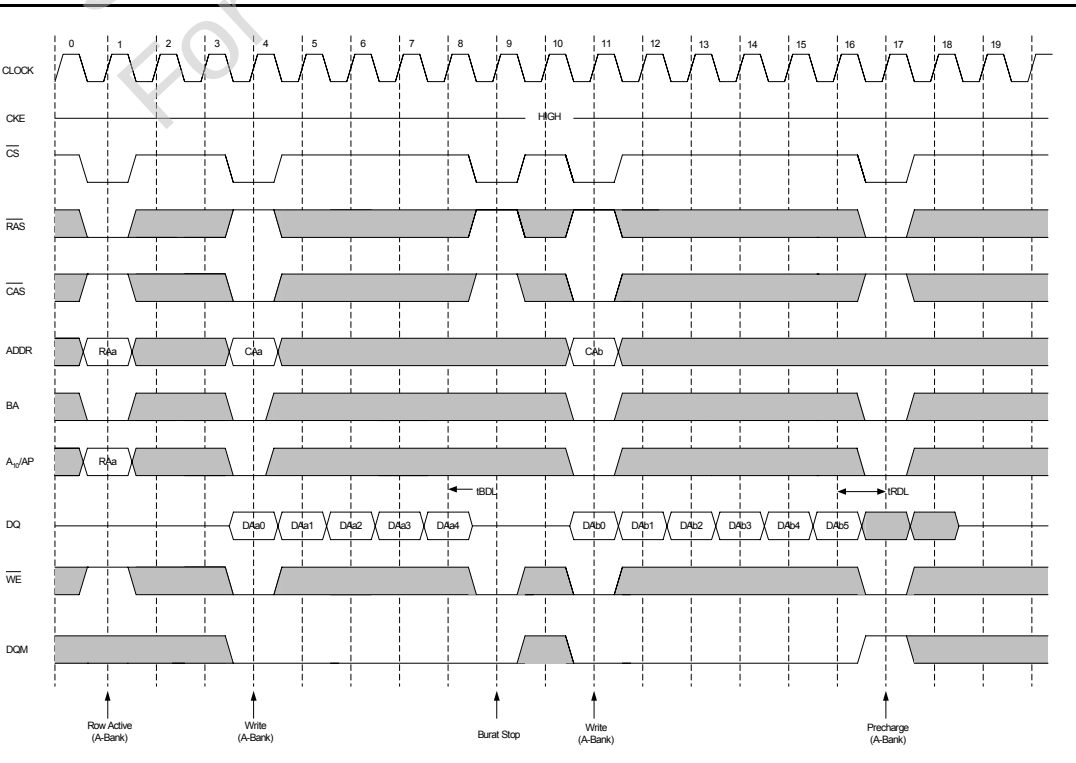
(V_{DDIO}=3.3V, TA=24°C, f=108MHz, V_{REF}=1.4V+-200mV)

Parameter	Symbol	Min.	Typ.	Max.	Units
Input pin capacitance	C_{IN}	-	3.5	-	pF
Input pin capacitance	C_{OUT}	-	3.5	-	pF
Bidirectional pin capacitance	C_{BIDIR}	-	3.5	-	pF

6.4. AC Characteristics

6.4.1. SDRAM interface timing diagrams





(Recommended condition for STB playback is listed in typical condition with f=121.5MHz)

Parameter	Symbol	Min.	Typ.	Max.	Units
Row active to row active delay	t_{RRD}	1	2	4 *1	System clock cycle
RAS to CAS delay	t_{RCD}	1	2	4 *1	System clock cycle
Row pre-charge time	t_{RP}	1	2	4 *1	System clock cycle
Row active time	t_{RAS}	1	5	8 *1	System clock cycle
Row cycle time	t_{RC}	1	8	32 *1	System clock cycle
Last data in to new column address delay	t_{CDL}	1	1	4 *1	System clock cycle
Column address to column address delay	t_{CCD}	1	1	1	System clock cycle
CLK cycle time *2	t_{CC}	6	8.2	1000	ns
CLK to valid SDRAM output delay *2	t_{SAC}	-	6.0	6.5	ns
SDRAM output data hold time *2	t_{OH}	1	2	-	ns
CLK high pulse width *3	t_{CH}	-	3	-	ns
CLK low pulse width *3	t_{CL}	-	3	-	ns
CLK to SDRAM output Low-Z	t_{SLZ}	-	1.0	(t_{CC})	ns
CLK to SDRAM output High-Z	t_{SHZ}	-	6.0	(t_{SAC})	ns

Note: 1.Using maximum values may limit system performance.

2.Width of data window can be estimated from (t_{CC}-t_{SAC}+t_{OH}).

3.Width of clock pulse depends on system clock cycle.

6.4.2. Video timing diagrams

Interlaced Modes

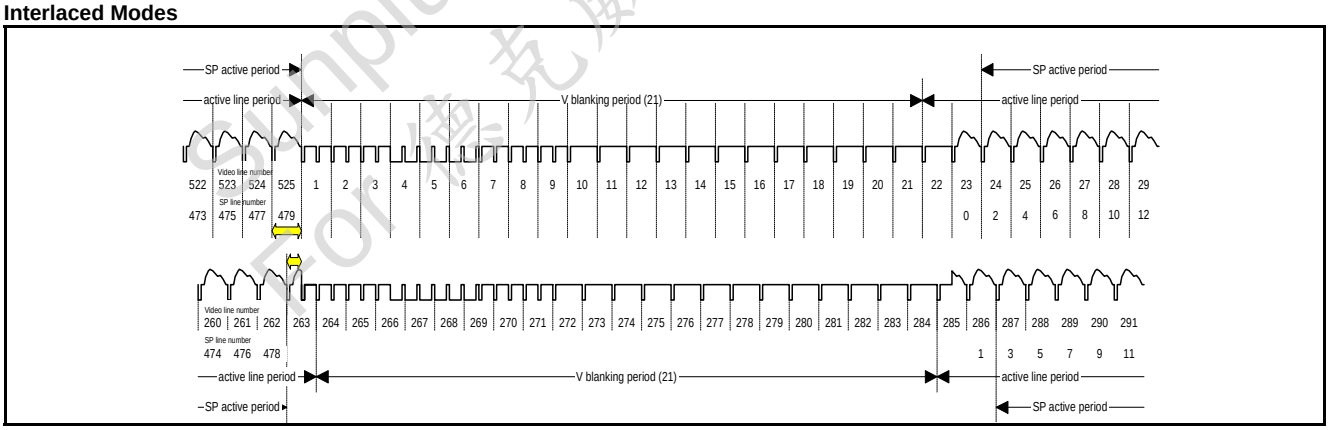


Figure 6-8: NTSC (480i) timing diagram

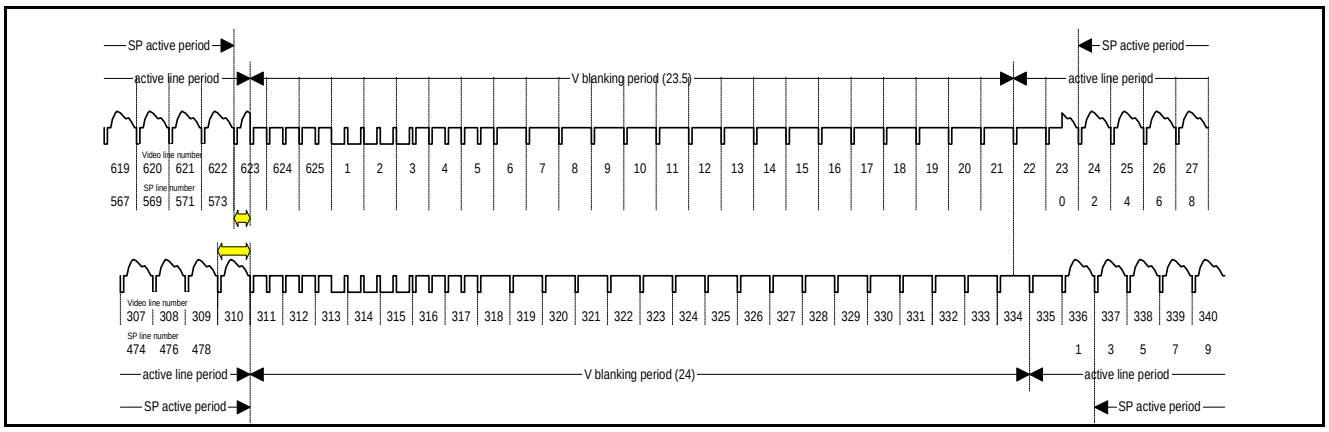


Figure 6-9: PAL (576i) timing diagram

Progressive Modes

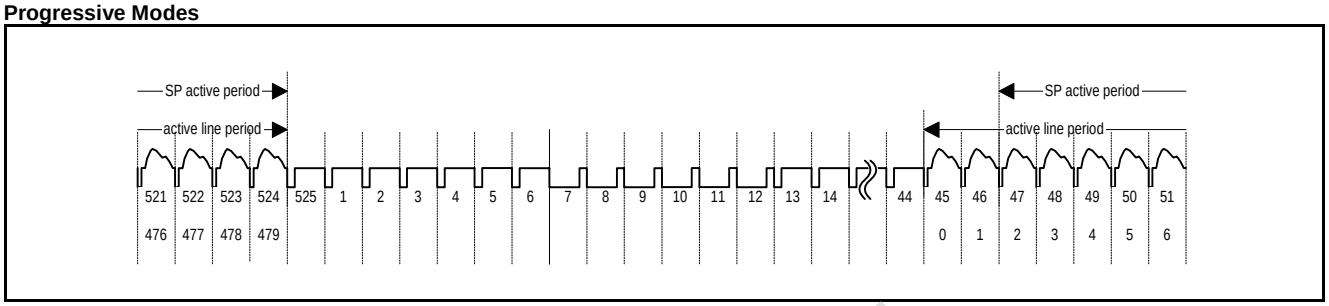


Figure 6-10: NTSC (480p) timing diagram

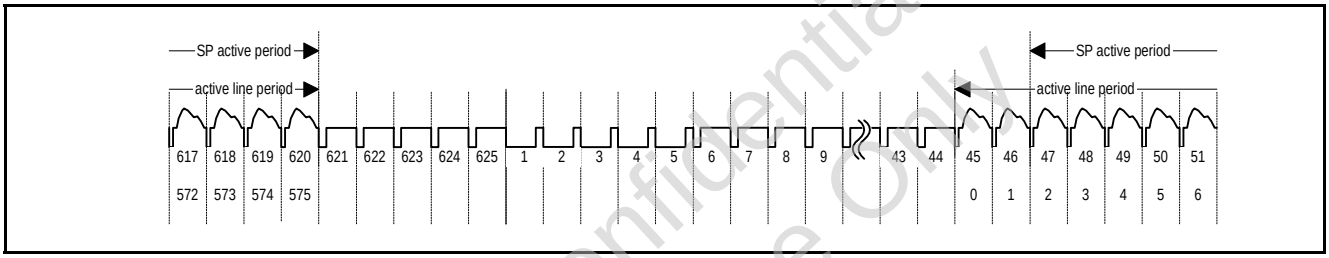


Figure 6-11: PAL (576p) timing diagram

6.4.3. Serial interface timing diagram

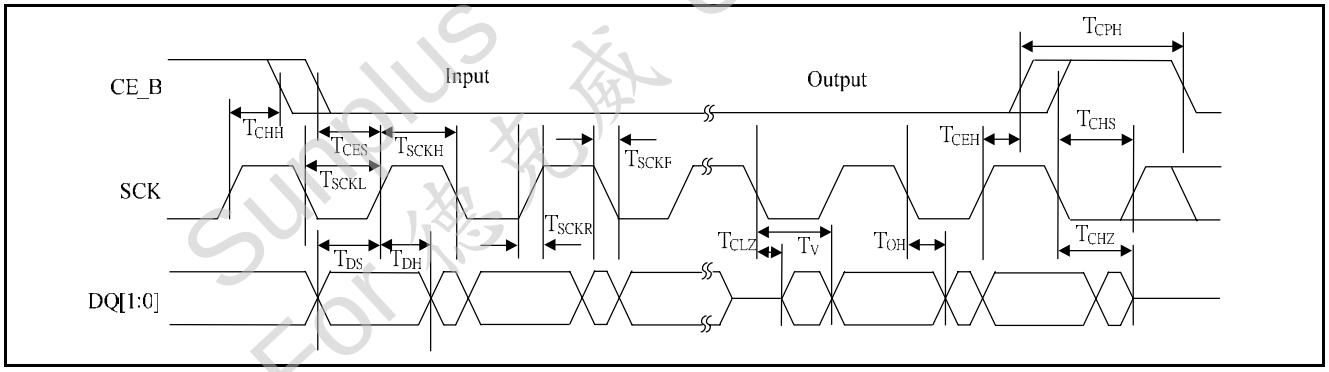


Figure 6-12: Serial interface timing diagram

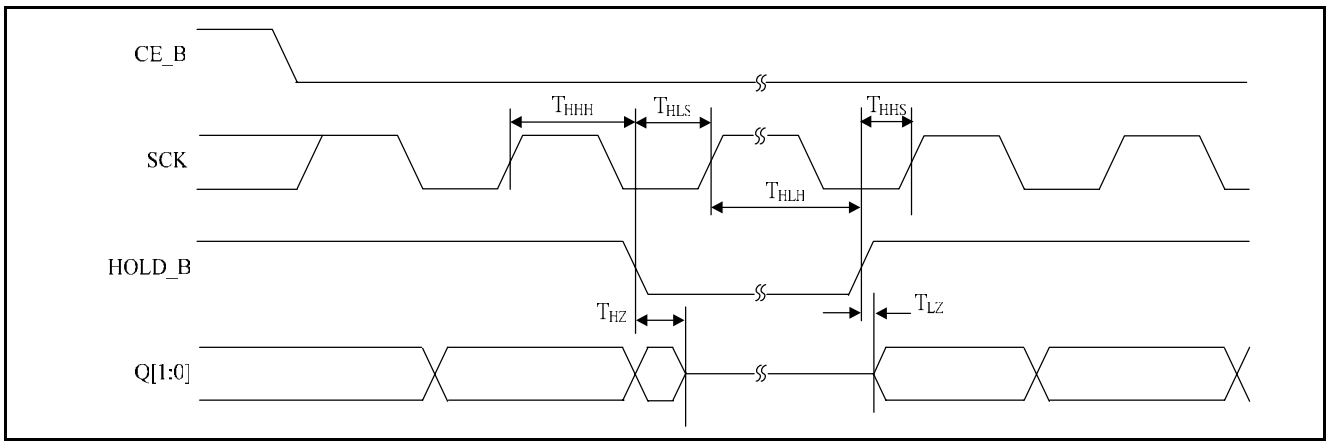


Figure 6-13: Hold timing diagram

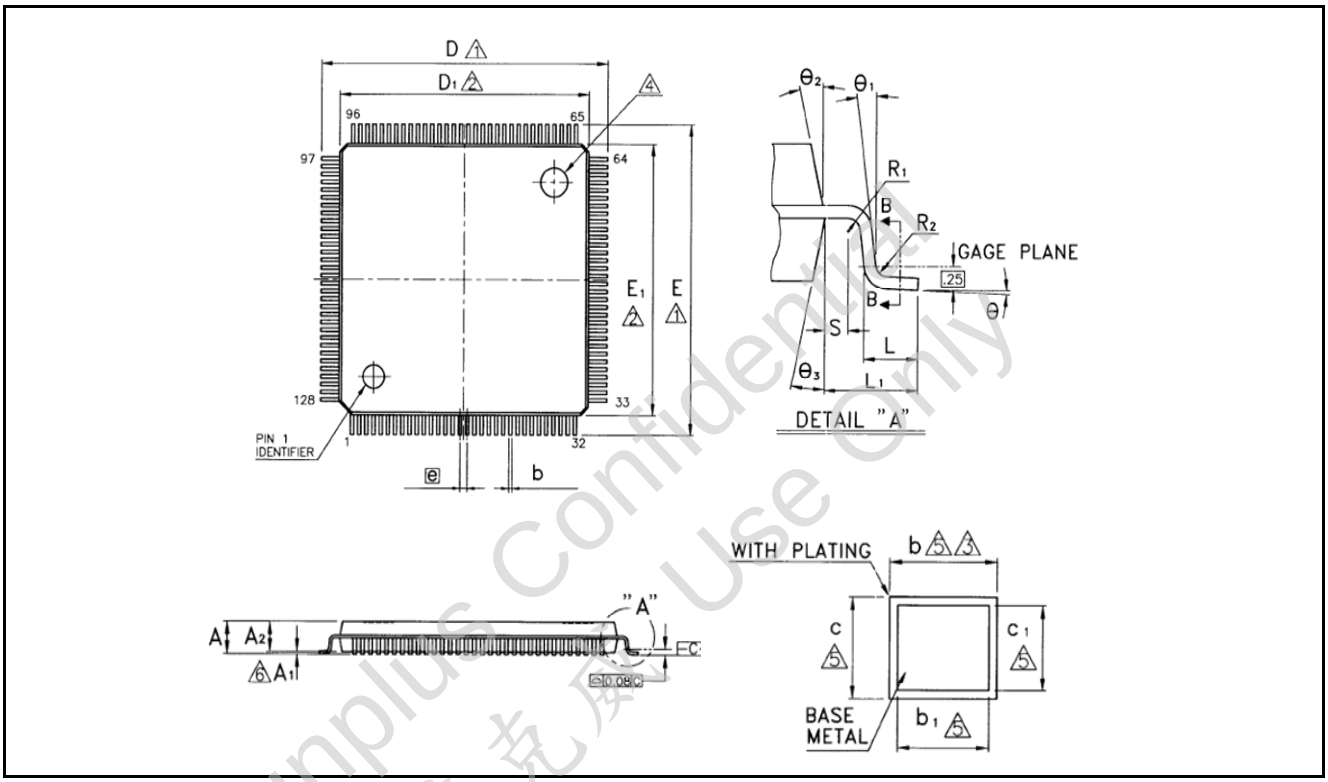
AC Operating Characteristics

Symbol	Parameter Description	Min.	Max.	Unit
F_{SCK}	Serial Clock Frequency	27	67.5	MHz
T_{SCKH}	Serial Clock High Time	7.4	18	ns
T_{SCKL}	Serial Clock Low Time	7.4	18	ns
T_{CES}	CE_B Active Setup Time	7.4		ns
T_{CEH}	CE_B Active Hold Time	7.4		ns
T_{CHS}	CE_B Not Active Setup Time	7.4		ns
T_{CHH}	CE_B Not Active Hold Time	7.4		ns
T_{CPH}	CE_B High Time	100		ns
T_{CHZ}	CE_B High to High-Z Output		10	ns
T_{CLZ}	SCK Low to Low-Z Output	8		ns
T_V	Output Valid from SCK	8		ns
T_{DS}	Data In Setup Time	3		ns
T_{DH}	Data In Hold Time	14.8		ns
T_{HLS}	HOLD_B Low Setup Time	6		ns
T_{HHS}	HOLD_B High Setup Time	6		ns
T_{HLH}	HOLD_B Low Hold Time	14.8		ns
T_{HHH}	HOLD_B High Hold Time	14.8		ns
T_{HZ}	HOLD_B Low to High-Z Output		8	ns
T_{LZ}	HOLD_B High to Low-Z Output		8	ns
T_{OH}	Output Hold from SCK Change	0		ns

7.PACKAGE/PAD LOCATION

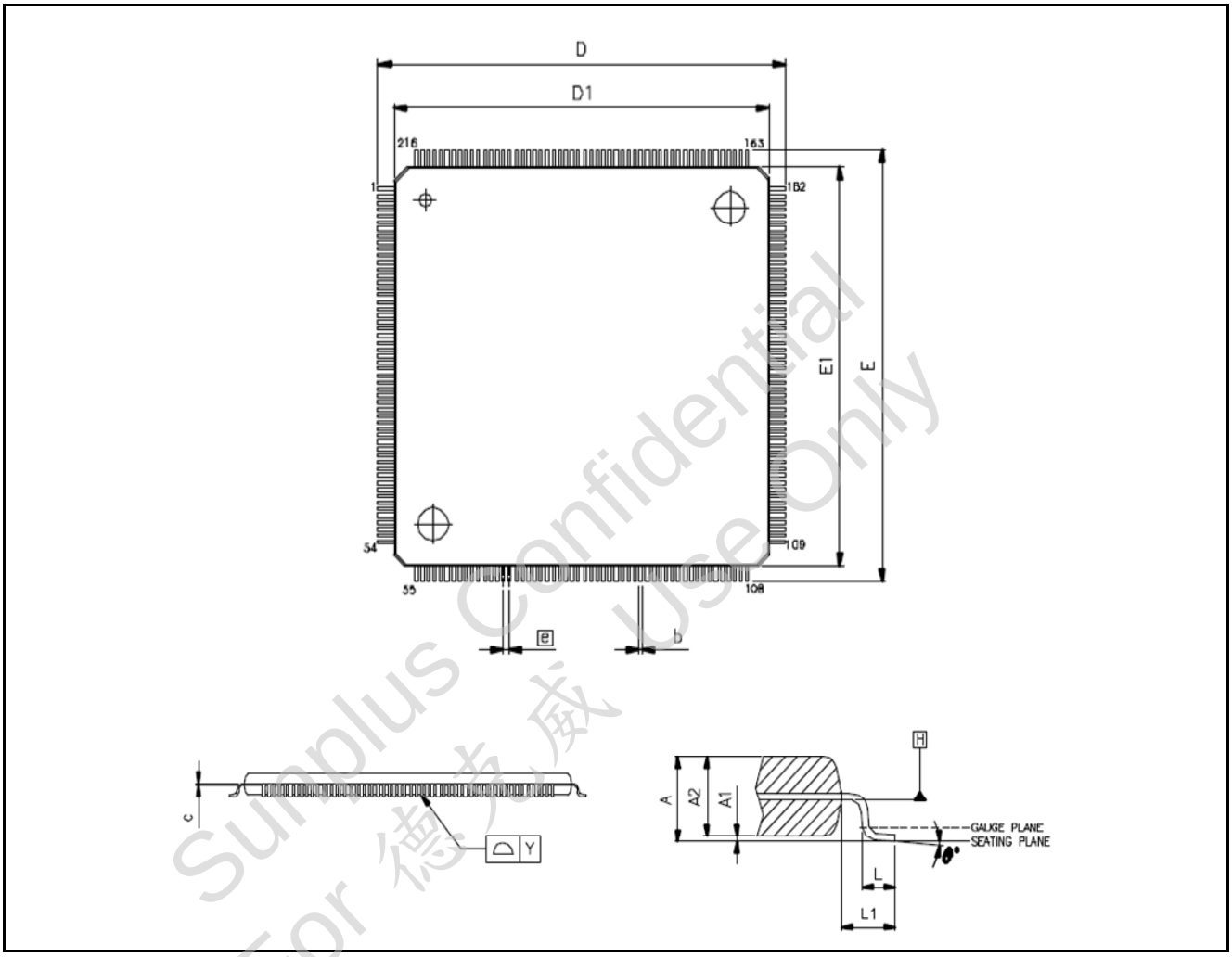
7.1. Outline Dimensions

LQFP-128 (14x14x1.4)



Symbol	Min.	Nom.	Max.	Unit
A	-	-	1.60	Millimeter
A1	0.05	-	-	Millimeter
A2	1.35	1.40	1.45	Millimeter
b	0.13	0.18	0.23	Millimeter
b1	0.13	0.16	0.19	Millimeter
c	0.09	-	0.20	Millimeter
c1	0.09	-	0.16	Millimeter
D	15.85	16.00	16.15	Millimeter
D1	13.90	14.00	14.10	Millimeter
E	15.85	16.00	16.15	Millimeter
E1	13.90	14.00	14.10	Millimeter
e	0.40 BSC			Millimeter
L	0.45	0.60	0.75	Millimeter
L1	1.00 REF			Millimeter
R1	0.08	-	-	Millimeter
R2	0.08	-	0.20	Millimeter
S	0.20	-	-	Millimeter
Θ	0^{o}	3.5^{o}	7^{o}	Millimeter
Θ1	0^{o}	-	-	Millimeter
Θ2	12^{o} TYP			Millimeter
Θ3	12^{o} TYP			Millimeter

LQFP-216 (24x24x1.4)



Symbol	Min.	Nom.	Max.	Unit
A	-	-	1.60	Millimeter
A1	0.05	-	0.15	Millimeter
A2	1.35	1.40	1.45	Millimeter
b	0.13	0.18	0.23	Millimeter
c	0.09	-	0.20	Millimeter
D1	24.00 BSC			Millimeter
E1	24.00 BSC			Millimeter
e	0.40 BSC			Millimeter
D	26.00 BSC			Millimeter
E	26.00 BSC			Millimeter
L	0.45	0.60	0.75	Millimeter
L1	1.00 REF			Millimeter
Y	0.08			Millimeter
θ^{o}	0^{o}	3.5^{o}	7^{o}	Millimeter

8.DISCLAIMER

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9.REVISION HISTORY

Date	Revision #	Description	Page
Nov. 25, 2007	0.1	Original	