DATA SHEET

SUNPLUS

SPHE8281A

DVD Single Chip MPEG A/V Processor

Preliminary

OCT. 04, 2004

Version 0.1

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DVD SINGLE CHIP MPEG A/V PROCESSOR

1.GENERAL DESCRIPTION

SPHE8281A A/V decoder is a single-chip integrated DVD A/V decoder. It performs real-time decoding and playback of ISO/IEC 11172 MPEG1, 13818 MPEG2 and MPEG4 14496-2 sources

SPHE8281A supports DVD-Video, DVD-Audio, Super Video CD, Video CD, CD-DA, HDCD, OKO, and CD-ROM disc formats.

SPHE8281A is designed to maximize system performance with minimum cost. For typical DVD application it integrates DVD/CD servo controller, multi-channel multi-format TV-encoder and audio quality ADC, with high quality 5.1ch Audio, or low cost 2-ch AC3 system.

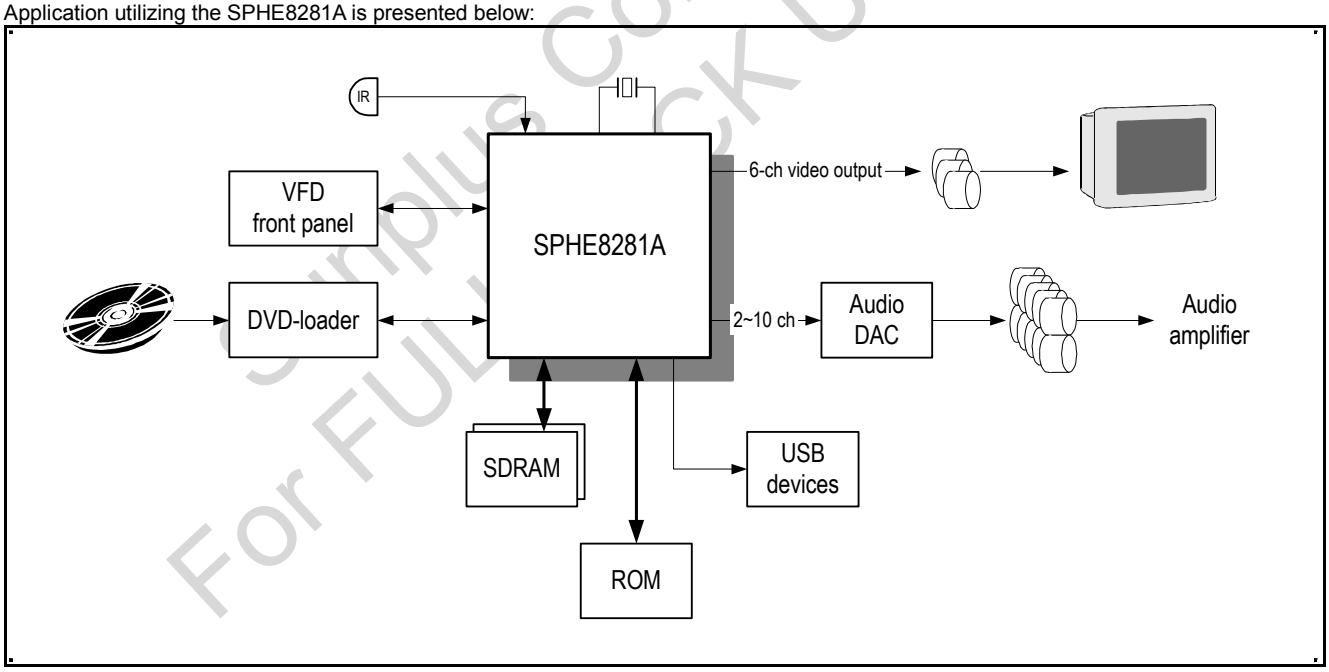
SPHE8281A supports Dolby Digital, DTS, MPEGI/II Layer1/2, PCM, LPCM, and WMA audio playback.

SPHE8281A also combines all the functions required for a high-performance progressive-scan DVD system. Built-in de-interlacing hardware allows high quality DVD playback. The embedded digital audio decoder is able to support key control and audio sound effects for Karaoke.

In additional to that SPHE8281A includes a flexible 2D graphics engine for high quality user interface and other applications. Complex application could be built using this platform easily.

Development tools of SPHE8281A include complete compiler tools, programming guide and system application libraries.

Application utilizing the SPHE8281A is presented below:



2.FEATURE

- Single Chip Integrated DVD Servo and A/V Decoder
- Integrated DVD/CD Servo Controller
  - Support 1x ~ 2x DVD format reading
  - Support 1x ~ 16x CD format reading
- Embedded 32-bit RISC Processor without external host controller
- Embedded Audio Processor supports multiple audio standards
- Embedded I/O processor supports programmable interface control
- Embedded TV encoder with multi-channel built-in high-speed video DAC supports various display standards
- Embedded audio ADC supports stereo analog audio input
- Built-in system PLL and audio PLL generate all clock sources required from single 27MHz input
- Support following disc format:
  - DVD Navigation 1.0
  - DVD audio
  - SVCD (Chaoji VCD)
  - OKO disc
  - VCD 2.0/1.1/1.0
  - CDDA / HDCD
  - CDROM (game, WMA and JPEG disc)
- CSS/CPPM hardware
  - Built-in CSS hardware
  - Built-in CPPM C2_DCBC and C2_D/C2_E function
- Video Decoder
  - Real time MPEG4 simple profile decoding
  - Real time MPEG4 Advanced Simple Profile D1 decoding
  - DivX3.11, 4.0 and 5.x version compatible (DivX home-theater profile)
  - Real time MPEG2 MP@ML decoding
  - Real time MPEG1 D1 (720x480x30 /720x576x25) decoding
  - Hardware accelerated JPEG decoding
  - Advanced decoding and display control
- Sub-picture Decoder
  - Advanced Sub-Picture Decoder for DVD SVCD and OKO
  - Support hardware vertical scaling
- Audio Decoder
  - Flexible Programmable DSP Architecture
  - Embedded high resolution audio quality ADC
  - Support CDDA, HDCD, and DVD-Audio
  - Support LPCM, PCM, and WMA playback
  - Support MPEGI/II layer 1/2 and MPEG 2.5 playback (with optional down-mixing)
  - Support Dolby Digital AC3 5.1ch / DTS 5.1ch playback (with optional down-mixing)
  - Support Key Shift of 2 channels
  - Support equalization, reverb and special sound field
- SDRAM controller
  - High Performance SDRAM controller
  - Support 16 or 32 bit operation
  - Support up to 4 SDRAM devices
  - Support 16M/64M/128M/256M SDRAM devices
- Graphics
  - Embedded 2D Graphics Accelerator
  - BitBlt, line, triangle drawing support
- Display
  - De-interlacing of interlaced video source
  - Flexible vertical interpolation
  - Flexible horizontal interpolation with optional CIF filter
  - Powerful cropping and panning effect
  - Support YUV422, 8-bit indexed color or 16-bit direct color format
- OSD
  - Multiple OSD regions with different formats
  - Support 4/16/256 indexed color
  - Support 16/24-bit direct color
  - Support x2/x3/x4 horizontal scaling
- Embedded TV encoder
  - Simultaneous multi-channel output
  - Support 480i/480p/576i/576p format
  - Support 640x480 VGA / 800x600 SVGA format
  - Support CVBS output
  - Support SVideo, Component (YUV / YPbPr) or RGB output
  - Macrovision 7.01 and Macrovision AGC v1.03 copy protection
- Interface
  - 27MHz crystal driver
  - 16/32-bit SDRAM interface
  - 8/16-bit ROM/FLASH/SRAM interface
  - UART ports
  - IR and VFD support
  - Video DAC analog output
  - Simultaneous 10-channel audio DAC output
  - IEC958/SPDIF digital input / output
  - Analog audio input
  - External ADC digital input interface (optional)
  - Optional ATAPI and I2S interface support
  - Optional Parallel Port interface support

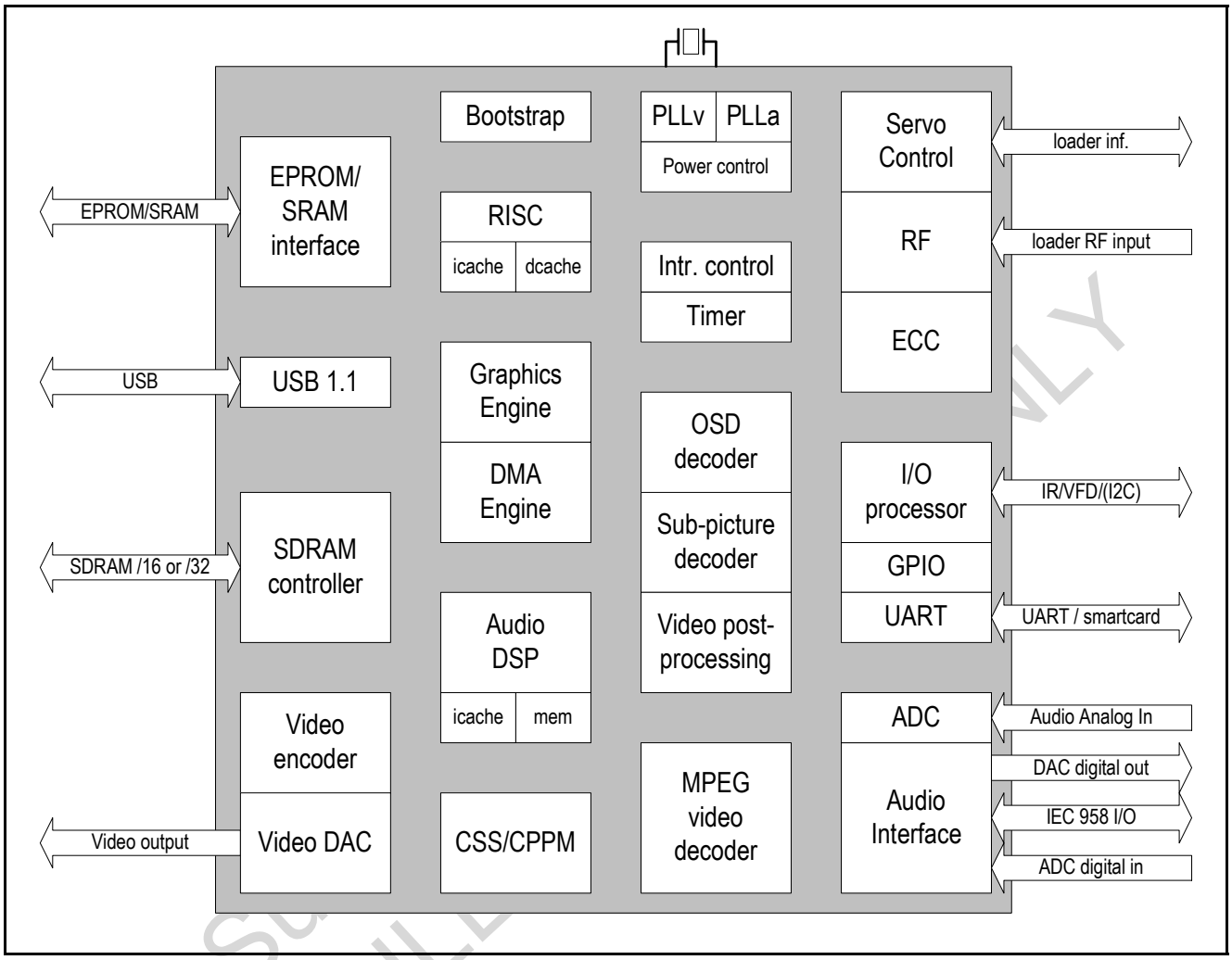
- Low power
  - Advanced low power design
  - Selective standby mode
  - Programmable low speed operation

- Technology
  - Advanced CMOS technology
  - 216-pin LQFP/ 256-pin LQFP package
  - 3v (I/O) and 1.8v (kernel) power supplies
  - 5v I/O tolerance

License Note: In order to take care of different royalties, Sunplus SPHE8281 series SPHE8281Ax have different extension character x for different combinations, such as, SPHE8281A (Dolby Digital, Macrovision, and DivX), SPHE8281AW (Dolby Digital, Macrovision, DivX, and WMA), and SPHE8281AD (Dolby Digital, Macrovision, DivX, WMA, and DTS) etc. For detail information, please contact with Sunplus Sales.

USB extension Note: SPHE8281Ax(-U) extension character -U represents with USB1.1 Host function.

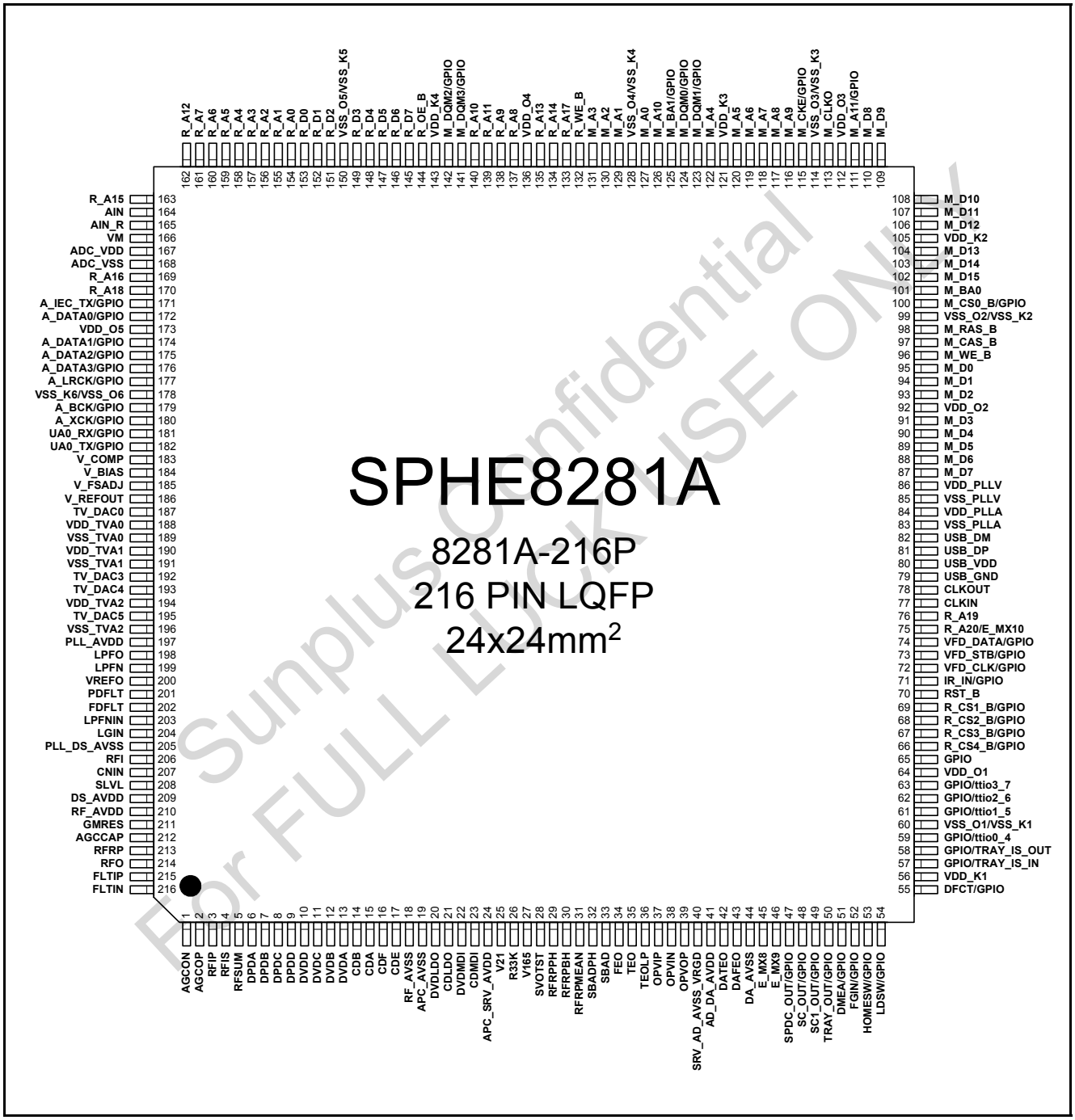
3.BLOCK DIAGRAM



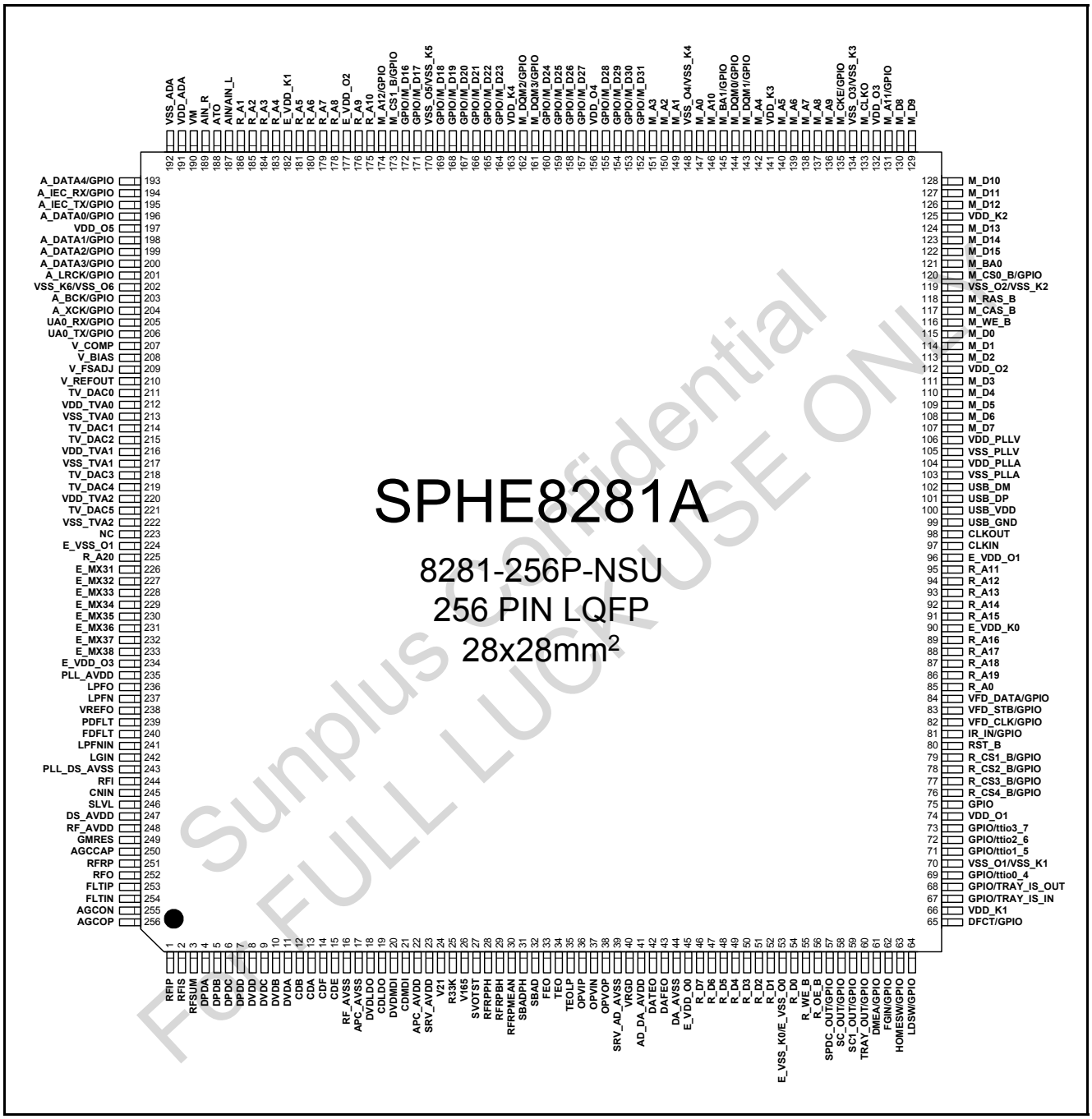
4.SIGNAL DESCRIPTION

4.1. Pin Configuration

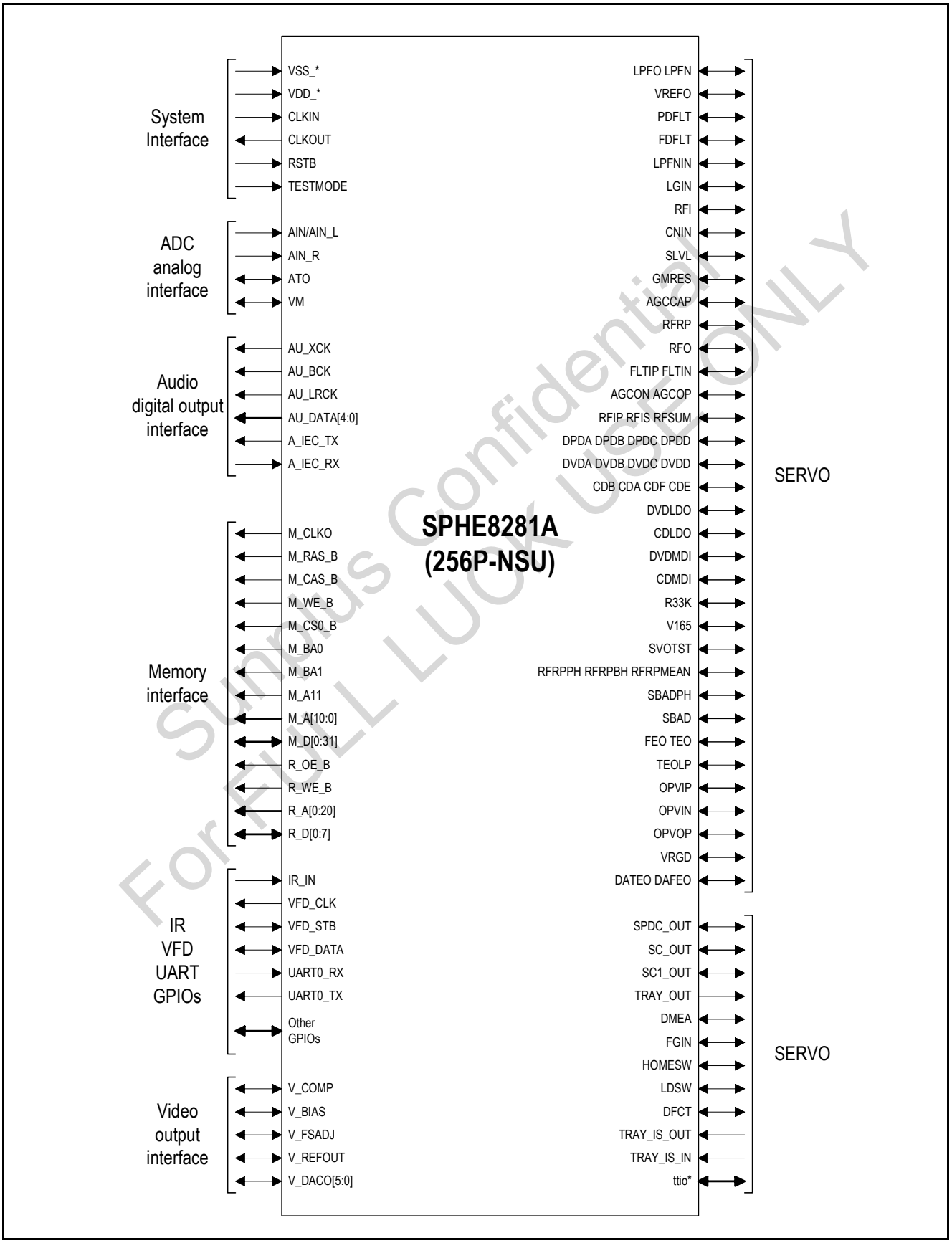
4.1.1. 216pin LQFP pin configuration



4.1.2. 256pin LQFP pin configuration



4.2. Pin Group Map



4.3. Pin Description

Symbol	256pin	216pin	I/O	Description
VSS_O0/ VSS_K0	53	n/a	S	Chip kernel logic and output shared ground pin #0
VSS_O1/ VSS_K1	70	60	S	(#1)
VSS_O2/ VSS_K2	119	99	S	(#2)
VSS_O3/ VSS_K3	134	114	S	(#3)
VSS_O4/ VSS_K4	148	128	S	(#4)
VSS_O5/ VSS_K5	170	150	S	(#5)
VSS_O6/ VSS_K6	202	178	S	(#6)
VSS_O7/ VSS_K7	224	n/a	S	(#7, not available in 216pin package)
VDD_K0	66	n/a	S	Kernel logic power supply pins for chip kernel logic and input pre-driver #0
VDD_K1	90	56	S	(#1)
VDD_K2	125	105	S	(#2)
VDD_K3	141	121	S	(#3)
VDD_K4	163	143	S	(#4)
VDD_K5	182	n/a	S	(#5)
VDD_O0	45	n/a	S	3.3V power supply pins for output pins #0
VDD_O1	74	64	S	(#1)
VDD_O2	96	92	S	(#2)
VDD_O3	112	112	S	(#3)
VDD_O4	132	136	S	(#4)
VDD_O5	156	173	S	(#5)
VDD_O6	177	n/a	S	(#6)
VDD_O7	197	n/a	S	(#7)
VDD_O8	234	n/a	S	(#8)
USB_GND	99	79	S	Ground pin for USB PLL
USB_VDD	100	80	S	3.3V power for USB PLL and USB transceiver
VSS_PLLA	103	83	S	Ground pin for USB transceiver and audio PLL
VDD_PLLA	104	84	S	3.3V power supply pin for audio PLL
VSS_PLLV	105	85	S	Ground pin for system PLL and audio PLL
VDD_PLLV	106	86	S	1.8V power supply pin for system PLL
VDD_TVA0	212	188	S	3.3V power supply pin for TV DAC
VDD_TVA1	216	190	S	(#1)
VDD_TVA2	220	194	S	(#2)
VSS_TVA0	213	89	S	Ground pin for TV DAC
VSS_TVA1	217	91	S	(#1)
VSS_TVA2	222	96	S	(#2)
VSS_ADA	192	168	S	Ground pin for on-chip audio ADC
VDD_ADA	191	167	S	3.3V power supply pin for on-chip audio ADC
R_D7	46	145	I/O	ROM / SRAM / flash data bus bit [7]
R_D6	47	146	I/O	ROM / SRAM / flash data bus bit [6]
R_D5	48	147	I/O	ROM / SRAM / flash data bus bit [5]
R_D4	49	148	I/O	ROM / SRAM / flash data bus bit [4]
R_D3	50	149	I/O	ROM / SRAM / flash data bus bit [3]
R_D2	51	151	I/O	ROM / SRAM / flash data bus bit [2]
R_D1	52	152	I/O	ROM / SRAM / flash data bus bit [1]

<table>
<tr><th>Symbol</th><th>256pin</th><th>216pin</th><th>I/O</th><th>Description</th></tr>
<tr><td>R_D0</td><td>54</td><td>153</td><td>I/O</td><td>ROM / SRAM / flash data bus bit [0]</td></tr>
<tr><td>R_WE_B</td><td>55</td><td>132</td><td>I/O</td><td>ROM / SRAM / flash write strobe</td></tr>
<tr><td>R_OE_B</td><td>56</td><td>144</td><td>I/O</td><td>ROM / SRAM / flash output enable</td></tr>
<tr><td>SPDC_OUT/GPIO</td><td>57</td><td>47</td><td>I/O</td><td>Servo SPDC_OUT<table><tr><th>Priority selection</th><th>Function</th><th>dir</th></tr><tr><td>sft_cfg2[11:10]=2’b01,2’b10</td><td>AT_RESET_B</td><td>O</td></tr><tr><td>sft_cfg4[0]=1’b1</td><td>SPDC_OUT (default)</td><td>I/O</td></tr><tr><td>Sft_cfg8[9]=1’b1</td><td>DAC_PDF</td><td>I</td></tr><tr><td>sft_cfg8[8]=1’b1</td><td>OTP_TEST_ADDR[0]</td><td>I</td></tr><tr><td>(other)</td><td>GPIO[0]</td><td>I/O</td></tr></table></td></tr>
<tr><td>SC_OUT/GPIO</td><td>58</td><td>48</td><td>I/O</td><td>Servo SC_OUT<table><tr><th>Priority selection</th><th>Function</th><th>dir</th></tr><tr><td>sft_cfg2[11:10]=2’b01,2’b10</td><td>AT_DIOR_B</td><td>O</td></tr><tr><td>sft_cfg4[1]=1’b1</td><td>SC_OUT (default)</td><td>I/O</td></tr><tr><td>Sft_cfg8[9]=1’b1</td><td>DAC_PDE</td><td>I</td></tr><tr><td>sft_cfg8[8]=1’b1</td><td>OTP_TEST_ADDR[1]</td><td>I</td></tr><tr><td>(other)</td><td>GPIO[1]</td><td>I/O</td></tr></table></td></tr>
<tr><td>SC1_OUT/GPIO</td><td>59</td><td>49</td><td>I/O</td><td>Servo SC1_OUT<table><tr><th>Priority selection</th><th>Function</th><th>dir</th></tr><tr><td>sft_cfg2[11:10]=2’b01,2’b10</td><td>AT_DIOW_B</td><td>O</td></tr><tr><td>sft_cfg4[2]=1’b1</td><td>SC1_OUT (default)</td><td>I/O</td></tr><tr><td>Sft_cfg8[9]=1’b1</td><td>DAC_PDD</td><td>I</td></tr><tr><td>sft_cfg8[8]=1’b1</td><td>OTP_TEST_ADDR[2]</td><td>I</td></tr><tr><td>(other)</td><td>GPIO[2]</td><td>I/O</td></tr></table></td></tr>
<tr><td>TRAY_OUT/GPIO</td><td>60</td><td>50</td><td>I/O</td><td>Servo TRAY_OUT<table><tr><th>Priority selection</th><th>Function</th><th>dir</th></tr><tr><td>sft_cfg2[11:10]=2’b01,2’b10</td><td>AT_IORDY</td><td>I</td></tr><tr><td>sft_cfg4[3]=1’b1</td><td>TRAY_OUT (default)</td><td>I/O</td></tr><tr><td>Sft_cfg8[9]=1’b1</td><td>DAC_PDC</td><td>I</td></tr><tr><td>sft_cfg8[8]=1’b1</td><td>OTP_TEST_ADDR[3]</td><td>I</td></tr><tr><td>(other)</td><td>GPIO[3]</td><td>I/O</td></tr></table></td></tr>
<tr><td>DMEA_OUT/GPIO</td><td>61</td><td>51</td><td>I/O</td><td>Servo DMEA<table><tr><th>Priority selection</th><th>Function</th><th>dir</th></tr><tr><td>sft_cfg2[11:10]=2’b01,2’b10</td><td>AT_DMACK</td><td>O</td></tr><tr><td>sft_cfg4[4]=1’b1</td><td>DMEA_OUT (default)</td><td>O</td></tr><tr><td>Sft_cfg8[9]=1’b1</td><td>DAC_PDB</td><td>I</td></tr><tr><td>sft_cfg8[8]=1’b1</td><td>OTP_TEST_ADDR[4]</td><td>I</td></tr><tr><td>(other)</td><td>GPIO[4]</td><td>I/O</td></tr></table></td></tr>
</table>

<table>
<tr><th>Symbol</th><th>256pin</th><th>216pin</th><th>I/O</th><th>Description</th></tr>
<tr><td>FGIN/GPIO</td><td>62</td><td>52</td><td>I/O</td><td>Servo FGIN
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg2[11:10]=2’b01,2’b10</td><td>AT_DMARQ</td><td>I</td></tr>
<tr><td>sft_cfg4[5]=1’b1</td><td>FGIN (default)</td><td>I</td></tr>
<tr><td>Sft_cfg8[9]=1’b1</td><td>DAC_PDA</td><td>I</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>OTP_TEST_PGM</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[5]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>HOMESW/GPIO</td><td>63</td><td>53</td><td>I/O</td><td>Servo HOMESW
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg2[3:2]=2’b10</td><td>UA0_RXD</td><td>I</td></tr>
<tr><td>sft_cfg1[8:6]=3’b010</td><td>R_CSALL_B</td><td>O</td></tr>
<tr><td>sft_cfg7[7:6]=2’b11</td><td>PCMCIA_IOW_B</td><td>O</td></tr>
<tr><td>Sft_cfg8[1]=1’b1</td><td>DSP_FL0</td><td>O</td></tr>
<tr><td>Sft_cfg8[9]=1’b1</td><td>DAC_DATA_F[9]</td><td>I</td></tr>
<tr><td>sft_cfg9[14:13]=2’b01</td><td>EXT_CLK48</td><td>I</td></tr>
<tr><td>sft_cfg6[4]=1’b1</td><td>DELAY_CHAIN1</td><td>O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>OTP_TEST_DATA</td><td>O</td></tr>
<tr><td>(other)</td><td>GPIO[6] (default)</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>LDSW/GPIO</td><td>64</td><td>54</td><td>I/O</td><td>Servo LDSW
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg2[3:2]=2’b10</td><td>UA0_TXD</td><td>O</td></tr>
<tr><td>sft_cfg2[5:4]=2’b10</td><td>UA1_RXD</td><td>I</td></tr>
<tr><td>sft_cfg7[7:6]=2’b11</td><td>PCMCIA_IOR_B</td><td>O</td></tr>
<tr><td>Sft_cfg8[2]=1’b1</td><td>DSP_FL1</td><td>O</td></tr>
<tr><td>Sft_cfg8[9]=1’b1</td><td>DAC_DATA_F[8]</td><td>I</td></tr>
<tr><td>sft_cfg7[15:14]=2’b11</td><td>CLK27_OUT</td><td>O</td></tr>
<tr><td>sft_cfg9[14:13]=2’b10</td><td>EXT_CLK48</td><td>I</td></tr>
<tr><td>sft_cfg6[4]=1’b1</td><td>DELAY_CHAIN2</td><td>O</td></tr>
<tr><td>(other)</td><td>GPIO[7] (default)</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>DFCT/GPIO</td><td>65</td><td>55</td><td>I/O</td><td>Servo DFCT
<table>
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<tr><td>sft_cfg2[11:10]=2’b01,2’b10</td><td>AT_INTRQ</td><td>I</td></tr>
<tr><td>sft_cfg4[6]=1’b1</td><td>DFCT (default)</td><td>O</td></tr>
<tr><td>Sft_cfg8[9]=1’b1</td><td>DAC_DATA_F[7]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[8]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>GPIO/TRAY_IS_IN</td><td>67</td><td>57</td><td>I/O</td><td>GPIO
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg2[11:10]=2’b01,2’b10</td><td>AT_ADR[1]</td><td>O</td></tr>
<tr><td>Sft_cfg8[3]=1’b1</td><td>DSP_FL2</td><td>O</td></tr>
<tr><td>fm_gpio_len[3:0] > 0</td><td>FM_GPIOB[0]</td><td>I/O</td></tr>
<tr><td>Sft_cfg8[9]=1’b1</td><td>DAC_DATA_F[6]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[9] (default)</td><td>I/O</td></tr>
</table></td></tr>
</table>

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<tr><th>Symbol</th><th>256pin</th><th>216pin</th><th>I/O</th><th>Description</th></tr>
<tr><td>GPIO/TRAY_IS_OUT</td><td>68</td><td>58</td><td>I/O</td><td>GPIO
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg2[11:10]=2’b01,2’b10</td><td>AT_ADR[2]</td><td>O</td></tr>
<tr><td>Sft_cfg8[4]=1’b1</td><td>DSP_FLAG_OUT</td><td>O</td></tr>
<tr><td>fm_gpio_len[3:0] > 0</td><td>FM_GPIOB[1]</td><td>I/O</td></tr>
<tr><td>Sft_cfg8[9]=1’b1</td><td>DAC_DATA_F[5]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[10] (default)</td><td>I/O</td></tr>
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<tr><td>GPIO/ttio0_4</td><td>69</td><td>59</td><td>I/O</td><td>GPIO
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg2[11:10]=2’b01,2’b10</td><td>AT_ADR[0]</td><td>O</td></tr>
<tr><td>sft_cfg4[9]=1’b1</td><td>ttio4/ttio0</td><td>I/O</td></tr>
<tr><td>Sft_cfg1[11:9]=3’b001</td><td>RISC_INT1_11</td><td>I</td></tr>
<tr><td>Sft_cfg3[11:10]=2’b01</td><td>ADC_BCK, digital audio input interface bit clock</td><td>I/O</td></tr>
<tr><td>fm_gpio_len[3:0] > 0</td><td>FM_GPIOB[2]</td><td>I/O</td></tr>
<tr><td>Sft_cfg8[9]=1’b1</td><td>DAC_DATA_F[4]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[11] (default)</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>GPIO/ttio1_5</td><td>71</td><td>61</td><td>I/O</td><td>GPIO
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg2[11:10]=2’b01,2’b10</td><td>AT_CS1</td><td>O</td></tr>
<tr><td>sft_cfg4[9]=1’b1</td><td>Ttio5/ttio1</td><td>I/O</td></tr>
<tr><td>sft_cfg4[15:13]=3’b001</td><td>HSYNC_PC</td><td>O</td></tr>
<tr><td>Sft_cfg1[11:9]=3’b001</td><td>RISC_INT1_12</td><td>I</td></tr>
<tr><td>Sft_cfg3[11:10]=2’b01</td><td>ADC_LRCK, digital audio input interface L/R strobe</td><td>I/O</td></tr>
<tr><td>fm_gpio_len[3:0] > 0</td><td>FM_GPIOB[3]</td><td>I/O</td></tr>
<tr><td>Sft_cfg8[9]=1’b1</td><td>DAC_DATA_F[3]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[12] (default)</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>GPIO/ttio2_6</td><td>72</td><td>62</td><td>I/O</td><td>GPIO
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg2[11:10]=2’b01,2’b10</td><td>AT_CS0</td><td>O</td></tr>
<tr><td>sft_cfg4[9]=1’b1</td><td>Ttio6/ttio2</td><td>I/O</td></tr>
<tr><td>sft_cfg4[15:13]=3’b001</td><td>VSYNC_PC</td><td>O</td></tr>
<tr><td>sft_cfg3[15:14]=2’b01</td><td>ISA_IOCHRDY</td><td>I</td></tr>
<tr><td>Sft_cfg1[11:9]=3’b001</td><td>RISC_INT1_13</td><td>I</td></tr>
<tr><td>Sft_cfg3[11:10]=2’b01</td><td>ADC_DATA, digital audio input interface data</td><td>I</td></tr>
<tr><td>fm_gpio_len[3:0] > 1</td><td>FM_GPIOB[4]</td><td>I/O</td></tr>
<tr><td>Sft_cfg8[9]=1’b1</td><td>DAC_DATA_F[2]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[13] (default)</td><td>I/O</td></tr>
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<table>
<tr><th>Symbol</th><th>256pin</th><th>216pin</th><th>I/O</th><th>Description</th></tr>
<tr><td>GPIO/ttio3_7</td><td>73</td><td>63</td><td>I/O</td><td>GPIO
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg4[9]=1’b1</td><td>Ttio7/ttio3</td><td>I/O</td></tr>
<tr><td>sft_cfg2[9:8]=2’b11</td><td>PCMCIA_WAIT_B</td><td>I</td></tr>
<tr><td>sft_cfg7[11:8]=4’b0001</td><td>EXT_CLK27</td><td>I</td></tr>
<tr><td>Sft_cfg1[11:9]=3’b001</td><td>RISC_INT1_14</td><td>I</td></tr>
<tr><td>fm_gpio_len[3:0] > 2</td><td>FM_GPIOB[5]</td><td>I/O</td></tr>
<tr><td>Sft_cfg8[9]=1’b1</td><td>DAC_DATA_F[1]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[14] (default)</td><td>I/O</td></tr>
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<tr><td>GPIO</td><td>75</td><td>65</td><td>I/O</td><td>GPIO
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg2[5:4]=2’b10</td><td>UA1_TXD</td><td>O</td></tr>
<tr><td>sft_cfg1[8:6]=3’b001</td><td>R_CSALL_B</td><td>O</td></tr>
<tr><td>sysclk_sel[4]</td><td>EXT_SYSCLK</td><td>I</td></tr>
<tr><td>sft_cfg7[11:8]=4’b0010</td><td>EXT_CLK27</td><td>I</td></tr>
<tr><td>fm_gpio_len[3:0] > 3</td><td>FM_GPIOB[6]</td><td>I/O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_F[0]</td><td>I</td></tr>
<tr><td>sft_cfg7[13:12]=2’b11</td><td>CLK54_OUT</td><td>O</td></tr>
<tr><td>sft_cfg9[14:13]=2’b11</td><td>EXT_CLK48</td><td>I</td></tr>
<tr><td>sft_cfg6[4]=1’b1</td><td>DELAY_CHAIN3</td><td>O</td></tr>
<tr><td>(other)</td><td>GPIO[15] (default)</td><td>I/O</td></tr>
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<tr><td>R_CS4_B/GPIO</td><td>76</td><td>66</td><td>I/O</td><td>ROM / SRAM / flash chip select #4 or GPIO
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<tr><td>sft_cfg1[7]=1’b1 & fm_gpio_len[3:0] = 10,11,12</td><td>FM_GPIOB[20]</td><td>I/O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_E[9]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[16]</td><td>I/O</td></tr>
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<tr><td>R_CS3_B/GPIO</td><td>77</td><td>67</td><td>I/O</td><td>ROM / SRAM / flash chip select #3 or GPIO
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<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_E[8]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[17]</td><td>I/O</td></tr>
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<tr><td>R_CS2_B/GPIO</td><td>78</td><td>68</td><td>I/O</td><td>ROM / SRAM / flash chip select #2 or GPIO
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<tr><td>(other)</td><td>GPIO[18]</td><td>I/O</td></tr>
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<tr><td>R_CS1_B/GPIO</td><td>79</td><td>69</td><td>I/O</td><td>ROM / SRAM / flash chip select #1 or GPIO
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<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_E[6]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[19]</td><td>I/O</td></tr>
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<tr><td>RST_B</td><td>80</td><td>70</td><td>I</td><td>System reset (active low reset)</td></tr>
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<tr><td>VFD_CLK/GPIO</td><td>82</td><td>72</td><td>I/O</td><td>GPIO[21] for VFD_CLK</td></tr>
<tr><td>VFD_STB/GPIO</td><td>83</td><td>73</td><td>I/O</td><td>GPIO[22] for VFD_STB<table><tr><th>Priority selection</th><th>Function</th><th>dir</th></tr><tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_E[5]</td><td>I</td></tr><tr><td>(other)</td><td>GPIO[22] (default)</td><td>I/O</td></tr></table></td></tr>
<tr><td>VFD_DATA/GPIO</td><td>84</td><td>74</td><td>I/O</td><td>GPIO[23] for VFD_DATA<table><tr><th>Priority selection</th><th>Function</th><th>dir</th></tr><tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_E[4]</td><td>I</td></tr><tr><td>(other)</td><td>GPIO[23] (default)</td><td>I/O</td></tr></table></td></tr>
<tr><td>R_A20</td><td>n/a</td><td>75</td><td>I/O</td><td>ROM / SRAM / flash address bus bit [20] (216pin package)</td></tr>
<tr><td>R_A0 (E_MX10)</td><td>85</td><td>n/a</td><td>I/O</td><td>ROM / SRAM / flash address bus bit [0] (256pin package)</td></tr>
<tr><td>R_A19 (E_MX11)</td><td>86</td><td>76</td><td>I/O</td><td>ROM / SRAM / flash address bus bit [19]</td></tr>
<tr><td>R_A18</td><td>87</td><td>170</td><td>I/O</td><td>ROM / SRAM / flash address bus bit [18]</td></tr>
<tr><td>R_A17</td><td>88</td><td>133</td><td>I/O</td><td>ROM / SRAM / flash address bus bit [17]</td></tr>
<tr><td>R_A16</td><td>89</td><td>169</td><td>I/O</td><td>ROM / SRAM / flash address bus bit [16]</td></tr>
<tr><td>R_A15</td><td>91</td><td>163</td><td>I/O</td><td>ROM / SRAM / flash address bus bit [15]</td></tr>
<tr><td>R_A14</td><td>92</td><td>134</td><td>I/O</td><td>ROM / SRAM / flash address bus bit [14]</td></tr>
<tr><td>R_A13</td><td>93</td><td>135</td><td>I/O</td><td>ROM / SRAM / flash address bus bit [13]</td></tr>
<tr><td>R_A12</td><td>94</td><td>162</td><td>I/O</td><td>ROM / SRAM / flash address bus bit [12]</td></tr>
<tr><td>R_A11</td><td>95</td><td>139</td><td>I/O</td><td>ROM / SRAM / flash address bus bit [11]</td></tr>
<tr><td>CLKIN</td><td>97</td><td>77</td><td>I</td><td>Clock input / crystal in (XTALI)</td></tr>
<tr><td>CLKOUT</td><td>98</td><td>78</td><td>O</td><td>Clock output / crystal out (XTALO)</td></tr>
<tr><td>USB_DP</td><td>101</td><td>81</td><td>I/O</td><td>USB bus D+ (only for USB versions)</td></tr>
<tr><td>USB_DM</td><td>102</td><td>82</td><td>I/O</td><td>USB bus D- (only for USB versions)</td></tr>
<tr><td>M_DD[7]</td><td>107</td><td>87</td><td>I/O</td><td>SDRAM data bus [7] or card reader GPIOA[0]<table><tr><th>Priority selection</th><th>Function</th><th>dir</th></tr><tr><td>Hardware control</td><td>SDRAM data bus [7] or card reader GPIOA[0] (default)</td><td>I/O</td></tr><tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_E[3]</td><td>I</td></tr><tr><td>sft_cfg1[12]=1’b1</td><td>USB_TEST_SUSPEND</td><td>I</td></tr></table></td></tr>
<tr><td>M_DD[6]</td><td>108</td><td>88</td><td>I/O</td><td>SDRAM data bus [6] or card reader GPIOA[1]<table><tr><th>Priority selection</th><th>Function</th><th>dir</th></tr><tr><td>Hardware control</td><td>SDRAM data bus [6] or card reader GPIOA[1] (default)</td><td>I/O</td></tr><tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_E[2]</td><td>I</td></tr><tr><td>sft_cfg1[12]=1’b1</td><td>USB_TEST_OEB</td><td>I</td></tr></table></td></tr>
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<tr><td>sft_cfg1[12]=1’b1</td><td>USB_TEST_OEA</td><td>I</td></tr>
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<tr><td>M_DD[4]</td><td>110</td><td>90</td><td>I/O</td><td>SDRAM data bus [4] or card reader GPIOA[3]
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<tr><td>Hardware control</td><td>SDRAM data bus [4] or card reader GPIOA[3] (default)</td><td>I/O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_E[0]</td><td>I</td></tr>
<tr><td>sft_cfg1[12]=1’b1</td><td>USB_TEST_DPP[0]</td><td>I</td></tr>
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<tr><td>M_DD[3]</td><td>111</td><td>91</td><td>I/O</td><td>SDRAM data bus [3] or card reader GPIOA[4]
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<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_D[9]</td><td>I</td></tr>
<tr><td>sft_cfg1[12]=1’b1</td><td>USB_TEST_DPP[1]</td><td>I</td></tr>
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<tr><td>M_DD[1]</td><td>114</td><td>94</td><td>I/O</td><td>SDRAM data bus [1] or card reader GPIOA[6]
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<tr><td>M_DD[0]</td><td>115</td><td>95</td><td>I/O</td><td>SDRAM data bus [0] or card reader GPIOA[7]
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<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_D[6]</td><td>I</td></tr>
<tr><td>sft_cfg1[12]=1’b1</td><td>USB_TEST_DPN[0]</td><td>I</td></tr>
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<tr><td>M_WE_B</td><td>116</td><td>96</td><td>I/O</td><td>SDRAM write enable / row precharge or card reader GPIOA[27]
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<tr><td>sft_cfg1[12]=1’b1</td><td>USB_TEST_DPN[3]</td><td>I</td></tr>
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<tr><td>M_CS0_B/GPIO</td><td>120</td><td>100</td><td>I/O</td><td>SDRAM chip select 0, or GPIO[24]
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<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_D[2]</td><td>I</td></tr>
<tr><td>sft_cfg1[12]=1’b1</td><td>USB_TEST_DMP[0]</td><td>I</td></tr>
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<tr><td>M_BA0</td><td>121</td><td>101</td><td>I/O</td><td>SDRAM bank select address [0] or card reader GPIOA[30]
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<tr><td>Hardware control</td><td>SDRAM data bus [8] or card reader GPIOA[15] (default)</td><td>I/O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_C[3]</td><td>I</td></tr>
<tr><td>sft_cfg1[12]=1’b1</td><td>USB_TEST_TXDM</td><td>I</td></tr>
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<tr><td>M_A[11]/ GPIO</td><td>131</td><td>111</td><td>I/O</td><td>SDRAM address bus [11] or GPIO[25]
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<tr><td>sft_cfg1[4]=1’b1</td><td>SDRAM address bus M_A[11] (default)</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_C[2]</td><td>I</td></tr>
<tr><td>sft_cfg1[12]=1’b1</td><td>USB_TEST_RXDP</td><td>O</td></tr>
<tr><td>(other)</td><td>GPIO[25]</td><td>I/O</td></tr>
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<tr><td>M_CLKO</td><td>133</td><td>113</td><td>O</td><td>SDRAM clock output</td></tr>
<tr><td>M_CKE/GPIO</td><td>135</td><td>115</td><td>I/O</td><td>SDRAM clock enable, or GPIO[26
<table>
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<tr><td>sft_cfg0[1]=1’b1</td><td>DRAM clock enable (default)</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_C[1]</td><td>I</td></tr>
<tr><td>sft_cfg1[12]=1’b1</td><td>USB_TEST_RXDM</td><td>O</td></tr>
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<tr><td>M_A[9]</td><td>136</td><td>116</td><td>I/O</td><td>SDRAM address bus [9] or card reader GPIOA[16]
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<tr><td>Hardware control</td><td>SDRAM address bus [9] or card reader GPIOA[16] (default)</td><td>I/O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_C[0]</td><td>I</td></tr>
<tr><td>sft_cfg1[12]=1’b1</td><td>USB_TEST_RXD</td><td>O</td></tr>
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<tr><td>M_A[8]</td><td>137</td><td>117</td><td>I/O</td><td>SDRAM address bus [8] or card reader GPIOA[17]
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<tr><td>M_A[7]</td><td>138</td><td>118</td><td>I/O</td><td>SDRAM address bus [7] or card reader GPIOA[18]
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<tr><td>Hardware control</td><td>SDRAM address bus [7] or card reader GPIOA[18] (default)</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_D_R[0]</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_B[8]</td><td>I</td></tr>
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<tr><td>M_A[6]</td><td>139</td><td>119</td><td>I/O</td><td>SDRAM address bus [6] or card reader GPIOA[19]
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<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_B[7]</td><td>I</td></tr>
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<tr><td>M_A[5]</td><td>140</td><td>120</td><td>I/O</td><td>SDRAM address bus [5] or card reader GPIOA[20]
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<tr><td>M_A[4]</td><td>142</td><td>122</td><td>I/O</td><td>SDRAM address bus [4] or card reader GPIOA[21]
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<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_D_R[3]</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_B[5]</td><td>I</td></tr>
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<tr><td>M_DQM1/GPIO</td><td>143</td><td>123</td><td>I/O</td><td>SDRAM data input/output mask for M_DD[15:8], or GPIOA[27]
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg0[3]=1’b1</td><td>SDRAM data input/output mask for M_DD[15:8] (default)</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_D_R[4]</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_B[4]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[27]</td><td>I/O</td></tr>
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<tr><td>M_DQM0/GPIO</td><td>144</td><td>124</td><td>I/O</td><td>SDRAM data input/output mask for M_DD[7:0] or GPIOA[28]
<table>
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<tr><td>sft_cfg0[2]=1’b1</td><td>SDRAM data input/output mask for M_DD[7:0] (default)</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_D_R[5]</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_B[3]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[28]</td><td>I/O</td></tr>
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<tr><td>M_BA1/GPIO</td><td>145</td><td>125</td><td>I/O</td><td>SDRAM bank select address [1] or GPIOA[29]
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<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_D_R[6]</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_B[2]</td><td>I</td></tr>
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<tr><td>M_A[10]</td><td>146</td><td>126</td><td>O</td><td>SDRAM address bus [10] or card reader GPIOA[22]
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<tr><td>Hardware control</td><td>SDRAM address bus [10] or card reader GPIOA[22](default)</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_D_R[7]</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_B[1]</td><td>I</td></tr>
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<tr><td>M_A[0]</td><td>147</td><td>127</td><td>O</td><td>SDRAM address bus [0] or card reader GPIOA[23]
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<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_D_R[8]</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_B[0]</td><td>I</td></tr>
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<tr><td>M_A[1]</td><td>149</td><td>129</td><td>O</td><td>SDRAM address bus [1] or card reader GPIOA[24]
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<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_D_R[9]</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_A[9]</td><td>I</td></tr>
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<tr><td>M_A[2]</td><td>150</td><td>130</td><td>O</td><td>SDRAM address bus [2] or card reader GPIOA[25]
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<tr><td>Hardware control</td><td>SDRAM address bus [2] or card reader GPIOA[25](default)</td><td>I/O</td></tr>
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<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_A[8]</td><td>I</td></tr>
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<tr><td>M_A[3]</td><td>151</td><td>131</td><td>O</td><td>SDRAM address bus [3] or card reader GPIOA[26]
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<tr><td>Hardware control</td><td>SDRAM address bus [3] or card reader GPIOA[26](default)</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_D_R[11]</td><td>O</td></tr>
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<tr><td>GPIO/M_DD[31]</td><td>152</td><td>n/a</td><td>I/O</td><td>SDRAM data bus bit 31 or GPIO[30]
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<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>hw_cfg_chg[5]=1’b1 or
hw_cfg_chg[4]=1’b0</td><td>SDRAM data bus [31]</td><td>I/O</td></tr>
<tr><td>sft_cfg2[5:4]=2’b11</td><td>UA1_RXD</td><td>I</td></tr>
<tr><td>sft_cfg2[11:10]=2’b01</td><td>AT_D[15]</td><td>I/O</td></tr>
<tr><td>sft_cfg1[11:9]=3’b010</td><td>RISC_INT1_11</td><td>I</td></tr>
<tr><td>sft_cfg0[13:12]=2’b01</td><td>TV_LCD_R[0]</td><td>O</td></tr>
<tr><td>sft_cfg8[7]=1’b1</td><td>MO_STAMP[0]</td><td>O</td></tr>
<tr><td>sft_cfg8[6]=1’b1</td><td>HB_GPIO_I[0]</td><td>O</td></tr>
<tr><td>sft_cfg7[1]=1’b0,
fm_gpio_len[3:0]=4'b1100</td><td>FM_GPIOB[27]</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_D_R[12]</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_A[6]</td><td>I</td></tr>
<tr><td>sft_cfg8[10]=1’b1</td><td>USB_BIST_FAIL</td><td>O</td></tr>
<tr><td>(other)</td><td>GPIO[30] (default)</td><td>I/O</td></tr>
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<tr><td>GPIO/M_DD[30]</td><td>153</td><td>n/a</td><td>I/O</td><td>SDRAM data bus bit 30 or GPIO[31]
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<tr><td>hw_cfg_chg[5]=1’b1 or
hw_cfg_chg[4]=1’b0</td><td>SDRAM data bus [30]</td><td>I/O</td></tr>
<tr><td>sft_cfg2[5:4]=2’b11</td><td>UA1_TXD</td><td>O</td></tr>
<tr><td>sft_cfg2[11:10]=2’b01</td><td>AT_D[0]</td><td>I/O</td></tr>
<tr><td>sft_cfg1[11:9]=3’b010</td><td>RISC_INT1_12</td><td>I</td></tr>
<tr><td>sft_cfg0[13:12]=2’b01</td><td>TV_LCD_R[1]</td><td>O</td></tr>
<tr><td>sft_cfg8[7]=1’b1</td><td>MO_STAMP[1]</td><td>O</td></tr>
<tr><td>sft_cfg8[6]=1’b1</td><td>HB_GPIO_I[1]</td><td>O</td></tr>
<tr><td>sft_cfg7[1]= 1’b 0
fm_gpio_len[3:0]>10</td><td>FM_GPIOB[26]</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_D_R[13]</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_A[5]</td><td>I</td></tr>
<tr><td>sft_cfg8[10]=1’b1</td><td>HOST_BIST_FAIL</td><td>O</td></tr>
<tr><td>(other)</td><td>GPIO[31] (default)</td><td>I/O</td></tr>
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hw_cfg_chg[4]=1’b0</td><td>SDRAM data bus [29]</td><td>I/O</td></tr>
<tr><td>sft_cfg2[7:6]=2’b01</td><td>UA1_CTS_B</td><td>I</td></tr>
<tr><td>sft_cfg2[11:10]=2’b01</td><td>AT_D[14]</td><td>I/O</td></tr>
<tr><td>sft_cfg7[11:8]=4’b0100</td><td>EXT_CLK27</td><td>I</td></tr>
<tr><td>sft_cfg1[11:9]=3’b010</td><td>RISC_INT1_13</td><td>I</td></tr>
<tr><td>sft_cfg0[13:12]=2’b01</td><td>TV_LCD_R[2]</td><td>O</td></tr>
<tr><td>sft_cfg8[7]=1’b1</td><td>MO_STAMP[2]</td><td>O</td></tr>
<tr><td>sft_cfg8[6]=1’b1</td><td>HB_GPIO_I[2]</td><td>O</td></tr>
<tr><td>sft_cfg7[1]= 1’b 0
fm_gpio_len[3:0]>10</td><td>FM_GPIOB[25]</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_D_R[14]</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_A[4]</td><td>I</td></tr>
<tr><td>sft_cfg8[10]=1’b1</td><td>CSS_BIST_FAIL</td><td>O</td></tr>
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hw_cfg_chg[4]=1’b0</td><td>SDRAM data bus [28]</td><td>I/O</td></tr>
<tr><td>sft_cfg2[7:6]=2’b01</td><td>UA1_RTS_B</td><td>O</td></tr>
<tr><td>sft_cfg2[11:10]=2’b01</td><td>AT_D[1]</td><td>I/O</td></tr>
<tr><td>sft_cfg1[11:9]=3’b010</td><td>RISC_INT1_14</td><td>I</td></tr>
<tr><td>sft_cfg0[13:12]=2’b01</td><td>TV_LCD_R[3]</td><td>O</td></tr>
<tr><td>sft_cfg8[7]=1’b1</td><td>MO_STAMP[3]</td><td>O</td></tr>
<tr><td>sft_cfg8[6]=1’b1</td><td>HB_GPIO_I[3]</td><td>O</td></tr>
<tr><td>sft_cfg7[1]= 1’b 0
fm_gpio_len[3:0]>10</td><td>FM_GPIOB[24]</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_D_L[0]</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_A[3]</td><td>I</td></tr>
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<tr><td>sft_cfg2[11:10]=2’b01</td><td>AT_D[13]</td><td>I/O</td></tr>
<tr><td>sft_cfg1[11:9]=3’b011</td><td>RISC_INT1_11</td><td>I</td></tr>
<tr><td>sft_cfg0[13:12]=2’b01</td><td>TV_LCD_R[4]</td><td>O</td></tr>
<tr><td>sft_cfg8[7]=1’b1</td><td>MO_STAMP[4]</td><td>O</td></tr>
<tr><td>sft_cfg8[6]=1’b1</td><td>HB_GPIO_I[4]</td><td>O</td></tr>
<tr><td>sft_cfg7[1]= 1’b 0
fm_gpio_len[3:0]>10</td><td>FM_GPIOB[23]</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_D_L[1]</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_A[2]</td><td>I</td></tr>
<tr><td>sft_cfg8[10]=1’b1</td><td>IOP_BIST_FAIL</td><td>O</td></tr>
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<tr><td>GPIO/M_DD[26]</td><td>158</td><td>n/a</td><td>I/O</td><td>SDRAM data bus bit 26 or GPIO[35]
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<tr><td>sft_cfg2[11:10]=2’b01</td><td>AT_D[2]</td><td>I/O</td></tr>
<tr><td>sft_cfg1[11:9]=3’b011</td><td>RISC_INT1_12</td><td>I</td></tr>
<tr><td>sft_cfg0[13:12]=2’b01</td><td>TV_LCD_R[5]</td><td>O</td></tr>
<tr><td>sft_cfg8[7]=1’b1</td><td>MO_STAMP[5]</td><td>O</td></tr>
<tr><td>sft_cfg8[6]=1’b1</td><td>HB_GPIO_I[5]</td><td>O</td></tr>
<tr><td>sft_cfg7[1]= 1’b 0,
fm_gpio_len[3:0]>10</td><td>FM_GPIOB[22]</td><td>I/O</td></tr>
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<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_A[1]</td><td>I</td></tr>
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<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>hw_cfg_chg[5]=1’b1 or hw_cfg_chg[4]=1’b0</td><td>SDRAM data bus [25]</td><td>I/O</td></tr>
<tr><td>sft_cfg2[7:6]=2’b01</td><td>UA1_RI_B</td><td>I</td></tr>
<tr><td>sft_cfg2[11:10]=2’b01</td><td>AT_D[12]</td><td>I/O</td></tr>
<tr><td>sft_cfg1[11:9]=3’b011</td><td>RISC_INT1_13</td><td>I</td></tr>
<tr><td>sft_cfg0[13:12]=2’b01</td><td>TV_LCD_G[0]</td><td>O</td></tr>
<tr><td>sft_cfg8[7]=1’b1</td><td>MO_STAMP[6]</td><td>O</td></tr>
<tr><td>sft_cfg8[6]=1’b1</td><td>HB_GPIO_I[6]</td><td>O</td></tr>
<tr><td>sft_cfg7[1]= 1’b 0, fm_gpio_len[3:0]>10</td><td>FM_GPIOB[21]</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_D_L[3]</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_DATA_A[0]</td><td>I</td></tr>
<tr><td>sft_cfg8[10]=1’b1</td><td>OSD_BIST_FAIL</td><td>O</td></tr>
<tr><td>(other)</td><td>GPIO[36] (default)</td><td>I/O</td></tr>
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<tr><td>GPIO/M_DD[24]</td><td>160</td><td>n/a</td><td>I/O</td><td>SDRAM data bus bit 24 or GPIO[37]
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>hw_cfg_chg[5]=1’b1 or hw_cfg_chg[4]=1’b0</td><td>SDRAM data bus [24]</td><td>I/O</td></tr>
<tr><td>sft_cfg2[7:6]=2’b01</td><td>UA1_DCD_B</td><td>I</td></tr>
<tr><td>sft_cfg2[11:10]=2’b01</td><td>AT_D[3]</td><td>I/O</td></tr>
<tr><td>sft_cfg7[3:2]=2’b01</td><td>VDIN_CK27</td><td>I</td></tr>
<tr><td>sft_cfg1[11:9]=3’b011</td><td>RISC_INT1_14</td><td>I</td></tr>
<tr><td>sft_cfg0[13:12]=2’b01</td><td>TV_LCD_G[1]</td><td>O</td></tr>
<tr><td>sft_cfg8[7]=1’b1</td><td>MO_STAMP[7]</td><td>O</td></tr>
<tr><td>sft_cfg8[6]=1’b1</td><td>HB_GPIO_I[7]</td><td>O</td></tr>
<tr><td>sft_cfg7[1]= 1’b 0,sft_cfg0[11]= 1’b 0, fm_gpio_len[3:0]>9</td><td>FM_GPIOB[20]</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_D_L[4]</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_OPA[0]</td><td>I</td></tr>
<tr><td>sft_cfg8[10]=1’b1</td><td>VPP_BIST_FAIL</td><td>O</td></tr>
<tr><td>(other)</td><td>GPIO[37] (default)</td><td>I/O</td></tr>
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<table>
<tr><th>Symbol</th><th>256pin</th><th>216pin</th><th>I/O</th><th>Description</th></tr>
<tr><td>M_DQM3/GPIO</td><td>161</td><td>141</td><td>I/O</td><td>SDRAM data input/output mask for M_DD[31:24] , or GPIO[38]
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg0[5]=1’b1</td><td>SDRAM data input/output mask for M_DD[31:24] (default)</td><td>O</td></tr>
<tr><td>sft_cfg2[3:2]=2’b11</td><td>UA0_RXD</td><td>I</td></tr>
<tr><td>sft_cfg1[8:6]=3’b011</td><td>R_CSALL_B</td><td>O</td></tr>
<tr><td>sft_cfg3[13:12]=2’b10</td><td>TV_HSYNC</td><td>I/O</td></tr>
<tr><td>sft_cfg4[15:13]=3’b010</td><td>TV_HSYNC_PC</td><td>O</td></tr>
<tr><td>sft_cfg7[7:6]=2’b01</td><td>PCMCIA_IOW_B</td><td>O</td></tr>
<tr><td>sft_cfg0[13:12]=2’b01</td><td>TV_LCD_G[2]</td><td>O</td></tr>
<tr><td>sft_cfg7[1]= 1’b0,
sft_cfg0[11]= 1’b 0,
fm_gpio_len[3:0]>9</td><td>FM_GPIOB[19]</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_D_L[5]</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_OPA[1]</td><td>I</td></tr>
<tr><td>sft_cfg8[10]=1’b1</td><td>OGT_BIST_FAIL</td><td>O</td></tr>
<tr><td>(other)</td><td>GPIO[38]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>M_DQM2/GPIO</td><td>162</td><td>142</td><td>I/O</td><td>SDRAM data input/output mask for M_DD[23:16] , or GPIO[39]
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg0[4]=1’b1</td><td>SDRAM data input/output mask for M_DD[23:16] (default)</td><td>O</td></tr>
<tr><td>sft_cfg2[3:2]=2’b11</td><td>UA0_TXD</td><td>O</td></tr>
<tr><td>sft_cfg3[13:12]=2’b10</td><td>TV_VSYNC</td><td>I/O</td></tr>
<tr><td>sft_cfg4[15:13]=3’b010</td><td>TV_VSYNC_PC</td><td>O</td></tr>
<tr><td>sft_cfg7[7:6]=2’b01</td><td>PCMCIA_IOR_B</td><td>O</td></tr>
<tr><td>sft_cfg0[13:12]=2’b01</td><td>TV_LCD_G[3]</td><td>O</td></tr>
<tr><td>sft_cfg7[1]= 1’b 0,
sft_cfg0[11]= 1’b 0,
fm_gpio_len[3:0]>9</td><td>FM_GPIOB[18]</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_D_L[6]</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_OPA[2]</td><td>I</td></tr>
<tr><td>sft_cfg8[10]=1’b1</td><td>BUF_CTRL_BIST_FAIL</td><td>O</td></tr>
<tr><td>(other)</td><td>GPIO[39]</td><td>I/O</td></tr>
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<tr><td>GPIO/M_DD[23]</td><td>164</td><td>n/a</td><td>I/O</td><td>GPIO[40] or SDRAM data bus bit 23
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>hw_cfg_chg[5]=1’b1</td><td>SDRAM data bus [23]</td><td>I/O</td></tr>
<tr><td>sft_cfg2[11:10]=2’b01</td><td>AT_D[11]</td><td>I/O</td></tr>
<tr><td>sft_cfg7[3:2]=2’b01</td><td>VDIN_DATA[0]</td><td>I</td></tr>
<tr><td>sft_cfg7[5:4]=2’b01</td><td>CCIR656_DATA[0]</td><td>O</td></tr>
<tr><td>sft_cfg0[13:12]=2’b01</td><td>TV_LCD_G[4]</td><td>O</td></tr>
<tr><td>sft_cfg8[7]=1’b1</td><td>MO_STAMP[8]</td><td>O</td></tr>
<tr><td>sft_cfg8[6]=1’b1</td><td>HB_GPIO_I[8]</td><td>O</td></tr>
<tr><td>sft_cfg7[1]= 1’b 0,
sft_cfg0[11]= 1’b 0,
fm_gpio_len[3:0]>9</td><td>FM_GPIOB[17]</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_D_L[7]</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_OPB[0]</td><td>I</td></tr>
<tr><td>sft_cfg8[10]=1’b1</td><td>MC_BIST_FAIL</td><td>O</td></tr>
<tr><td>(other)</td><td>GPIO[40] (default)</td><td>I/O</td></tr>
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<tr><td>GPIO/M_DD[22]</td><td>165</td><td>n/a</td><td>I/O</td><td>GPIO[41] or SDRAM data bus bit 22
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>hw_cfg_chg[5]=1’b1</td><td>SDRAM data bus [22]</td><td>I/O</td></tr>
<tr><td>sft_cfg2[11:10]=2’b01</td><td>AT_D[4]</td><td>I/O</td></tr>
<tr><td>sft_cfg7[3:2]=2’b01</td><td>VDIN_DATA[1]</td><td>I</td></tr>
<tr><td>sft_cfg7[5:4]=2’b01</td><td>CCIR656_DATA[1]</td><td>O</td></tr>
<tr><td>sft_cfg7[11:8]=4’b0101</td><td>EXT_CLK27</td><td>I</td></tr>
<tr><td>sft_cfg0[13:12]=2’b01</td><td>TV_LCD_G[5]</td><td>O</td></tr>
<tr><td>sft_cfg8[7]=1’b1</td><td>MO_STAMP[9]</td><td>O</td></tr>
<tr><td>sft_cfg8[6]=1’b1</td><td>HB_GPIO_I[9]</td><td>O</td></tr>
<tr><td>sft_cfg7[1]= 1’b 0,
sft_cfg0[11]= 1’b 0,
fm_gpio_len[3:0]>8</td><td>FM_GPIOB[16]</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_D_L[8]</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_OPB[1]</td><td>I</td></tr>
<tr><td>sft_cfg8[10]=1’b1</td><td>VLD_BIST_FAIL</td><td>O</td></tr>
<tr><td>(other)</td><td>GPIO[41] (default)</td><td>I/O</td></tr>
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<tr><td>GPIO/M_DD[21]</td><td>166</td><td>n/a</td><td>I/O</td><td>GPIO[42] or SDRAM data bus bit 21
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>hw_cfg_chg[5]=1’b1</td><td>SDRAM data bus [21]</td><td>I/O</td></tr>
<tr><td>sft_cfg2[11:10]=2’b01</td><td>AT_D[10]</td><td>I/O</td></tr>
<tr><td>sft_cfg7[3:2]=2’b01</td><td>VDIN_DATA[2]</td><td>I</td></tr>
<tr><td>sft_cfg7[5:4]=2’b01</td><td>CCIR656_DATA[2]</td><td>O</td></tr>
<tr><td>sft_cfg0[13:12]=2’b01</td><td>TV_LCD_B[0]</td><td>O</td></tr>
<tr><td>sft_cfg8[7]=1’b1</td><td>MO_STAMP[10]</td><td>O</td></tr>
<tr><td>sft_cfg8[6]=1’b1</td><td>HB_GPIO_I[10]</td><td>O</td></tr>
<tr><td>sft_cfg7[1]= 1’b 0,
sft_cfg0[11]= 1’b 0,
fm_gpio_len[3:0]>8</td><td>FM_GPIOB[15]</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_D_L[9]</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_OPB[2]</td><td>I</td></tr>
<tr><td>sft_cfg8[10]=1’b1</td><td>INVQ_BIST_FAIL</td><td>O</td></tr>
<tr><td>(other)</td><td>GPIO[42] (default)</td><td>I/O</td></tr>
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<tr><td>GPIO/M_DD[20]</td><td>167</td><td>n/a</td><td>I/O</td><td>GPIO[43] or SDRAM data bus bit 20
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>hw_cfg_chg[5]=1’b1</td><td>SDRAM data bus [20]</td><td>I/O</td></tr>
<tr><td>sft_cfg2[11:10]=2’b01</td><td>AT_D[5]</td><td>I/O</td></tr>
<tr><td>sft_cfg7[3:2]=2’b01</td><td>VDIN_DATA[3]</td><td>I</td></tr>
<tr><td>sft_cfg7[5:4]=2’b01</td><td>CCIR656_DATA[3]</td><td>O</td></tr>
<tr><td>sft_cfg1[11:9]=3’b100</td><td>RISC_INT1_11</td><td>I</td></tr>
<tr><td>sft_cfg0[13:12]=2’b01</td><td>TV_LCD_B[1]</td><td>O</td></tr>
<tr><td>sft_cfg8[7]=1’b1</td><td>MO_STAMP[11]</td><td>O</td></tr>
<tr><td>sft_cfg8[6]=1’b1</td><td>HB_GPIO_I[11]</td><td>O</td></tr>
<tr><td>sft_cfg7[1]= 1’b 0,
sft_cfg0[11]= 1’b 0,
fm_gpio_len[3:0]>8</td><td>FM_GPIOB[14]</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_D_L[10]</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_OPC[0]</td><td>I</td></tr>
<tr><td>sft_cfg8[10]=1’b1</td><td>IDCT_BIST_FAIL</td><td>O</td></tr>
<tr><td>(other)</td><td>GPIO[43] (default)</td><td>I/O</td></tr>
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<tr><th>Symbol</th><th>256pin</th><th>216pin</th><th>I/O</th><th>Description</th></tr>
<tr><td>GPIO/M_DD[19]</td><td>168</td><td>n/a</td><td>I/O</td><td>GPIO[44] or SDRAM data bus bit 19
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<tr><td>hw_cfg_chg[5]=1’b1</td><td>SDRAM data bus [19]</td><td>I/O</td></tr>
<tr><td>sft_cfg2[11:10]=2’b01</td><td>AT_D[9]</td><td>I/O</td></tr>
<tr><td>sft_cfg7[3:2]=2’b01</td><td>VDIN_DATA[4]</td><td>I</td></tr>
<tr><td>sft_cfg7[5:4]=2’b01</td><td>CCIR656_DATA[4]</td><td>O</td></tr>
<tr><td>sft_cfg1[11:9]=3’b100</td><td>RISC_INT1_12</td><td>I</td></tr>
<tr><td>sft_cfg0[13:12]=2’b01</td><td>TV_LCD_B[2]</td><td>O</td></tr>
<tr><td>sft_cfg8[7]=1’b1</td><td>MO_STAMP[12]</td><td>O</td></tr>
<tr><td>sft_cfg8[6]=1’b1</td><td>HB_GPIO_I[12]</td><td>O</td></tr>
<tr><td>sft_cfg7[1]= 1’b 0,
sft_cfg0[11]= 1’b 0,
fm_gpio_len[3:0]>8</td><td>FM_GPIOB[13]</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_D_L[11]</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_OPC[1]</td><td>I</td></tr>
<tr><td>sft_cfg8[10]=1’b1</td><td>AGDC_BIST_FAIL</td><td>O</td></tr>
<tr><td>(other)</td><td>GPIO[44] (default)</td><td>I/O</td></tr>
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<tr><td>GPIO/M_DD[18]</td><td>169</td><td>n/a</td><td>I/O</td><td>GPIO[45] or SDRAM data bus bit 18
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>hw_cfg_chg[5]=1’b1</td><td>SDRAM data bus [18]</td><td>I/O</td></tr>
<tr><td>sft_cfg2[11:10]=2’b01</td><td>AT_D[6]</td><td>I/O</td></tr>
<tr><td>sft_cfg7[3:2]=2’b01</td><td>VDIN_DATA[5]</td><td>I</td></tr>
<tr><td>sft_cfg7[5:4]=2’b01</td><td>CCIR656_DATA[5]</td><td>O</td></tr>
<tr><td>sft_cfg1[11:9]=3’b100</td><td>RISC_INT1_13</td><td>I</td></tr>
<tr><td>sft_cfg3[11:10]=2’b10</td><td>ADC_BCK, digital audio input interface bit clock</td><td>I/O</td></tr>
<tr><td>sft_cfg0[13:12]=2’b01</td><td>TV_LCD_B[3]</td><td>O</td></tr>
<tr><td>sft_cfg8[7]=1’b1</td><td>MO_STAMP[13]</td><td>O</td></tr>
<tr><td>sft_cfg8[6]=1’b1</td><td>HB_GPIO_I[13]</td><td>O</td></tr>
<tr><td>sft_cfg7[1]= 1’b 0,
sft_cfg0[11]= 1’b 0,
fm_gpio_len[3:0]>8</td><td>FM_GPIOB[12]</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_D_L[12]</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_OPC[2]</td><td>I</td></tr>
<tr><td>sft_cfg8[10]=1’b1</td><td>RI_BIST_FAIL</td><td>O</td></tr>
<tr><td>(other)</td><td>GPIO[45] (default)</td><td>I/O</td></tr>
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<tr><th>Symbol</th><th>256pin</th><th>216pin</th><th>I/O</th><th>Description</th></tr>
<tr><td>GPIO/M_DD[17]</td><td>171</td><td>n/a</td><td>I/O</td><td>GPIO[46] or SDRAM data bus bit 17
<table>
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<tr><td>sft_cfg2[11:10]=2’b01</td><td>AT_D[8]</td><td>I/O</td></tr>
<tr><td>sft_cfg7[3:2]=2’b01</td><td>VDIN_DATA[6]</td><td>I</td></tr>
<tr><td>sft_cfg7[5:4]=2’b01</td><td>CCIR656_DATA[6]</td><td>O</td></tr>
<tr><td>sft_cfg1[11:9]=3’b100</td><td>RISC_INT1_14</td><td>I</td></tr>
<tr><td>sft_cfg3[11:10]=2’b10</td><td>ADC_LRCK, digital audio input interface L/R strobe</td><td>I/O</td></tr>
<tr><td>sft_cfg0[13:12]=2’b01</td><td>TV_LCD_B[4]</td><td>O</td></tr>
<tr><td>sft_cfg8[7]=1’b1</td><td>MO_STAMP[14]</td><td>O</td></tr>
<tr><td>sft_cfg8[6]=1’b1</td><td>HB_GPIO_I[14]</td><td>O</td></tr>
<tr><td>sft_cfg7[1]= 1’b 0,
sft_cfg0[11]= 1’b 0,
fm_gpio_len[3:0]>7</td><td>FM_GPIOB[11]</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_D_L[13]</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_OPD[0]</td><td>I</td></tr>
<tr><td>sft_cfg8[10]=1’b1</td><td>BOOTROM_BIST_FAIL</td><td>O</td></tr>
<tr><td>(other)</td><td>GPIO[46] (default)</td><td>I/O</td></tr>
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<tr><td>GPIO/M_DD[16]</td><td>172</td><td>n/a</td><td>I/O</td><td>GPIO[47] or SDRAM data bus bit 16
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>hw_cfg_chg[5]=1’b1</td><td>SDRAM data bus [16]</td><td>I/O</td></tr>
<tr><td>sft_cfg2[11:10]=2’b01</td><td>AT_D[7]</td><td>I/O</td></tr>
<tr><td>sft_cfg7[3:2]=2’b01</td><td>VDIN_DATA[7]</td><td>I</td></tr>
<tr><td>sft_cfg7[5:4]=2’b01</td><td>CCIR656_DATA[7]</td><td>O</td></tr>
<tr><td>sft_cfg7[11:8]=4’b0110</td><td>EXT_CLK27</td><td>I</td></tr>
<tr><td>sft_cfg3[11:10]=2’b10</td><td>ADC_DATA, digital audio input interface data</td><td>I</td></tr>
<tr><td>sft_cfg0[13:12]=2’b01</td><td>TV_LCD_B[5]</td><td>O</td></tr>
<tr><td>sft_cfg8[7]=1’b1</td><td>MO_STAMP[15]</td><td>O</td></tr>
<tr><td>sft_cfg8[6]=1’b1</td><td>HB_GPIO_I[15]</td><td>O</td></tr>
<tr><td>sft_cfg7[1]= 1’b 0,
sft_cfg0[11]= 1’b 0,
fm_gpio_len[3:0]>7</td><td>FM_GPIOB[10]</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_D_L[14]</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_OPD[1]</td><td>I</td></tr>
<tr><td>sft_cfg8[10]=1’b1</td><td>DMA_BIST_FAIL</td><td>O</td></tr>
<tr><td>(other)</td><td>GPIO[47] (default)</td><td>I/O</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Symbol</th><th>256pin</th><th>216pin</th><th>I/O</th><th>Description</th></tr>
<tr><td>M_CS1_B/GPIO</td><td>173</td><td>n/a</td><td>I/O</td><td>SDRAM chip select 1, or GPIO[48]
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg0[7]=1’b1</td><td>SDRAM chip select 1 (default)</td><td>I/O</td></tr>
<tr><td>sft_cfg1[8:6]=3’b100</td><td>R_CSALL_B</td><td>O</td></tr>
<tr><td>sft_cfg7[11:8]=4’b0111</td><td>EXT_CLK27</td><td>I</td></tr>
<tr><td>sft_cfg0[13:12]=2’b01</td><td>TV_LCD_DVAL</td><td>O</td></tr>
<tr><td>sft_cfg7[1]= 1’b 0, fm_gpio_len[3:0]>6</td><td>FM_GPIOB[9]</td><td>I/O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_OPD[2]</td><td>I</td></tr>
<tr><td>sft_cfg8[10]=1’b1</td><td>RISC_BIST_FAIL</td><td>O</td></tr>
<tr><td>(other)</td><td>GPIO[48]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>M_A[12]/GPIO</td><td>174</td><td>n/a</td><td>I/O</td><td>SDRAM address bus [12] or GPIO[49]
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg1[5]=1’b1</td><td>SDRAM address bus [12] (default)</td><td>I/O</td></tr>
<tr><td>sft_cfg1[15]=1’b1</td><td>PWM_OUT</td><td>O</td></tr>
<tr><td>sft_cfg3[15:14]=2’b10</td><td>ISA_ IOCHRDY</td><td>I</td></tr>
<tr><td>sft_cfg7[11:8]=4’b1000</td><td>EXT_CLK27</td><td>I</td></tr>
<tr><td>sft_cfg0[13:12]=2’b01</td><td>TV_LCD_DCLK</td><td>O</td></tr>
<tr><td>sft_cfg7[1]= 1’b 0, fm_gpio_len[3:0]>5</td><td>FM_GPIOB[8]</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_Q64</td><td>O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_OPE[0]</td><td>I</td></tr>
<tr><td>sft_cfg7[13:12]=2’b01</td><td>CLK54_OUT</td><td>O</td></tr>
<tr><td>sft_cfg7[15:14]=2’b01</td><td>CLK27_OUT</td><td>O</td></tr>
<tr><td>sft_cfg8[10]=1’b1</td><td>SRV_MPEG_BIST_FAIL</td><td>O</td></tr>
<tr><td>(other)</td><td>GPIO[49]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>R_A10</td><td>175</td><td>140</td><td>O</td><td>ROM / SRAM / flash address bus bit [10]</td></tr>
<tr><td>R_A9</td><td>176</td><td>138</td><td>O</td><td>ROM / SRAM / flash address bus bit [9]</td></tr>
<tr><td>R_A8</td><td>178</td><td>137</td><td>O</td><td>ROM / SRAM / flash address bus bit [8]</td></tr>
<tr><td>R_A7</td><td>179</td><td>161</td><td>O</td><td>ROM / SRAM / flash address bus bit [7]</td></tr>
<tr><td>R_A6</td><td>180</td><td>160</td><td>O</td><td>ROM / SRAM / flash address bus bit [6]</td></tr>
<tr><td>R_A5</td><td>181</td><td>159</td><td>O</td><td>ROM / SRAM / flash address bus bit [5]</td></tr>
<tr><td>R_A4</td><td>183</td><td>158</td><td>O</td><td>ROM / SRAM / flash address bus bit [4]</td></tr>
<tr><td>R_A3</td><td>184</td><td>157</td><td>O</td><td>ROM / SRAM / flash address bus bit [3]</td></tr>
<tr><td>R_A2</td><td>185</td><td>156</td><td>O</td><td>ROM / SRAM / flash address bus bit [2]</td></tr>
<tr><td>R_A1</td><td>186</td><td>155</td><td>O</td><td>ROM / SRAM / flash address bus bit [1]</td></tr>
<tr><td>R_A0</td><td></td><td>154</td><td>O</td><td>ROM / SRAM / flash address bus bit [0]</td></tr>
<tr><td>AIN/AIN_L</td><td>187</td><td>164</td><td>A</td><td>ADC input (left channel, with OP)</td></tr>
<tr><td>ATO</td><td>188</td><td>n/a</td><td>A</td><td>ADC OP output. When not used, connect a 0.1uF to ground.</td></tr>
<tr><td>AIN_R</td><td>189</td><td>165</td><td>A</td><td>ADC input (right channel)</td></tr>
<tr><td>VM</td><td>190</td><td>166</td><td>A</td><td>ADC input voltage reference. When not used, connect a 0.1uF to ground.</td></tr>
</table>

<table>
<tr><th>Symbol</th><th>256pin</th><th>216pin</th><th>I/O</th><th>Description</th></tr>
<tr><td>A_DATA[4] / GPIO</td><td>193</td><td>n/a</td><td>I/O</td><td>Serial audio data output for channel 9/8 or GPIO
<table>
<tr><th>Priority selection</th><th>Function</th><th>Dir</th></tr>
<tr><td>sft_cfg3[5]=1’b1</td><td>A_DATA[4] (default)</td><td>O</td></tr>
<tr><td>sft_cfg7[5:4]=2’b01,2’b11</td><td>VDOUT_CLK</td><td>O</td></tr>
<tr><td>sft_cfg2[9:8]=2’b01</td><td>PCMCIA_WAIT_B</td><td>I</td></tr>
<tr><td>sft_cfg7[11:8]=4’b0011</td><td>EXT_CLK27</td><td>I</td></tr>
<tr><td>sft_cfg7[1]=1’b0, fm_gpio_len[3:0]>4</td><td>FM_GPIOB [7]</td><td>I/O</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_OPE[1]</td><td>I</td></tr>
<tr><td>sft_cfg7[13:12]=2’b10</td><td>CLK54_OUT</td><td>O</td></tr>
<tr><td>sft_cfg7[15:14]=2’b10</td><td>CLK27_OUT</td><td>O</td></tr>
<tr><td>(other)</td><td>GPIO[50]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>A_IEC_RX/GPIO</td><td>194</td><td>n/a</td><td>I/O</td><td>IEC-958 receive data
<table>
<tr><th>Priority selection</th><th>Function</th><th>Dir</th></tr>
<tr><td>sft_cfg3[7]=1’b1</td><td>A_IEC_RX (default)</td><td>I</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MCLK</td><td>I</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_OPE[2]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[51]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>A_IEC_TX/GPIO</td><td>195</td><td>171</td><td>I/O</td><td>IEC-958 transmit data
<table>
<tr><th>Priority selection</th><th>Function</th><th>Dir</th></tr>
<tr><td>sft_cfg3[8]=1’b1</td><td>A_IEC_TX (default)</td><td>O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_C[0]</td><td>I</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_OPF[0]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[52]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>A_DATA[0] / GPIO</td><td>196</td><td>172</td><td>I/O</td><td>Serial audio data output for channel 1/0 or GPIO
<table>
<tr><th>Priority selection</th><th>Function</th><th>Dir</th></tr>
<tr><td>sft_cfg3[1]=1’b1</td><td>A_DATA[0] (default)</td><td>O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_C[1]</td><td>I</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_OPF[1]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[53]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>A_DATA[1] / GPIO</td><td>198</td><td>174</td><td>I/O</td><td>Serial audio data output for channel 3/2 or GPIO
<table>
<tr><th>Priority selection</th><th>Function</th><th>Dir</th></tr>
<tr><td>sft_cfg3[2]=1’b1</td><td>A_DATA[1] (default)</td><td>O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_C[2]</td><td>I</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_OPF[2]</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[54]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>A_DATA[2] / GPIO</td><td>199</td><td>175</td><td>I/O</td><td>Serial audio data output for channel 5/4 or GPIO
<table>
<tr><th>Priority selection</th><th>Function</th><th>Dir</th></tr>
<tr><td>sft_cfg3[3]=1’b1</td><td>A_DATA[2] (default)</td><td>O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_PWAD</td><td>I</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_PDALL</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[55]</td><td>I/O</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Symbol</th><th>256pin</th><th>216pin</th><th>I/O</th><th>Description</th></tr>
<tr><td>A_DATA[3] / GPIO</td><td>200</td><td>176</td><td>I/O</td><td>Serial audio data output for channel 7/6 or GPIO
<table>
<tr><th>Priority selection</th><th>Function</th><th>Dir</th></tr>
<tr><td>sft_cfg3[4]=1’b1</td><td>A_DATA[3] (default)</td><td>O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_SPGA</td><td>I</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_TEST</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[56]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>A_LRCK/GPIO</td><td>201</td><td>177</td><td>I/O</td><td>PCM data output L/R strobe
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>sft_cfg3[6]=1’b1</td><td>A_LRCK (default)</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_MODE1</td><td>I</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_UD</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[57]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>A_BCK/GPIO</td><td>203</td><td>179</td><td>I/O</td><td>PCM bit clock
<table>
<tr><th>Priority selection</th><th>Function</th><th>Dir</th></tr>
<tr><td>sft_cfg3[0]=1’b1</td><td>A_BCK (default)</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_MODE1_1</td><td>I</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_BGPD</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[58]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>A_XCK/GPIO</td><td>204</td><td>180</td><td>I/O</td><td>Audio over-sampling clock
<table>
<tr><th>Priority selection</th><th>Function</th><th>Dir</th></tr>
<tr><td>sft_cfg3[9]=1’b1</td><td>A_XCK (default)</td><td>I/O</td></tr>
<tr><td>sft_cfg8[8]=1’b1</td><td>ADC_MONO_MODE2</td><td>I</td></tr>
<tr><td>sft_cfg8[9]=1’b1</td><td>DAC_CLK</td><td>I</td></tr>
<tr><td>(other)</td><td>GPIO[59]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>UA0_RX/GPIO</td><td>205</td><td>181</td><td>I/O</td><td>UART #0 data receive or GPIO
<table>
<tr><th>Priority selection</th><th>Function</th><th>Dir</th></tr>
<tr><td>sft_cfg2[3:2] =2’b01</td><td>UART0_RX (default)</td><td>I</td></tr>
<tr><td>sft_cfg3[13:12]=2’b01</td><td>TV_HSYNC</td><td>I/O</td></tr>
<tr><td>sft_cfg4[15:13]=3’b011</td><td>HSYNC_PC</td><td>O</td></tr>
<tr><td>(other)</td><td>GPIO[60]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>UA0_TX/GPIO</td><td>206</td><td>182</td><td>I/O</td><td>UART #0 data transmit or GPIO
<table>
<tr><th>Priority selection</th><th>Function</th><th>Dir</th></tr>
<tr><td>sft_cfg2[3:2] =2’b01</td><td>UART0_TX (default)</td><td>O</td></tr>
<tr><td>sft_cfg3[13:12]=2’b01</td><td>TV_VSYNC</td><td>I/O</td></tr>
<tr><td>sft_cfg4[15:13]=3’b011</td><td>VSYNC_PC</td><td>O</td></tr>
<tr><td>(other)</td><td>GPIO[61]</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>V_COMP</td><td>207</td><td>183</td><td>A</td><td>Compensation pin. A 0.1pF ceramic capacitor must be used to bypass this pin to VSSA. The lead length must be kept as short as possible to avoid noise.</td></tr>
<tr><td>V_BIAS</td><td>208</td><td>184</td><td></td><td></td></tr>
<tr><td>V_FSADJ</td><td>209</td><td>185</td><td>A</td><td>Full-Scale adjustment control pin. The full-scale current of D/A converters can be adjusted by connecting a resistor (R_{SET}) between this pin and ground.</td></tr>
<tr><td>V_REFOUT</td><td>210</td><td>186</td><td>A</td><td>Voltage reference output. It generates typical 1.2V voltage reference and may be used to drive V_REFIN pin directly.</td></tr>
<tr><td>V_DAC[0]</td><td>211</td><td>187</td><td>A</td><td>Video DAC output #0. This is a high-impedance current source output. These outputs can drive a 37.5 Ω load directly.</td></tr>
</table>

<table>
<tr><th>Symbol</th><th>256pin</th><th>216pin</th><th>I/O</th><th>Description</th></tr>
<tr><td>V_DAC[1]</td><td>214</td><td>n/a</td><td>A</td><td>Video DAC output #1. This is a high-impedance current source output. These outputs can drive a 37.5 Ω load directly.</td></tr>
<tr><td>V_DAC[2]</td><td>215</td><td>n/a</td><td>A</td><td>Video DAC output #2. This is a high-impedance current source output. These outputs can drive a 37.5 Ω load directly.</td></tr>
<tr><td>V_DAC[3]</td><td>218</td><td>192</td><td>A</td><td>Video DAC output #3. This is a high-impedance current source output. These outputs can drive a 37.5 Ω load directly.</td></tr>
<tr><td>V_DAC[4]</td><td>219</td><td>193</td><td>A</td><td>Video DAC output #4. This is a high-impedance current source output. These outputs can drive a 37.5 Ω load directly.</td></tr>
<tr><td>V_DAC[5]</td><td>221</td><td>195</td><td>A</td><td>Video DAC output #5. This is a high-impedance current source output. These outputs can drive a 37.5 Ω load directly.</td></tr>
<tr><td>NC</td><td>223</td><td>n/a</td><td>-</td><td>No connection</td></tr>
<tr><td>R_A20 (E_MX30)</td><td>225</td><td>n/a</td><td>I/O</td><td>ROM / SRAM / flash address bus bit [20], or GPIO[92]
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>Hardware control</td><td>ROM / SRAM / flash address bus bit [20]</td><td>O</td></tr>
<tr><td>pad_ctrl[4]=1’b1</td><td>656_DATA[7]</td><td>O</td></tr>
<tr><td>sft_cfg7[3:2]=2’b11</td><td>VDIN_DATA[0]</td><td>I</td></tr>
<tr><td>sft_cfg7[5:4]=2’b10</td><td>656_DATA[4]</td><td>O</td></tr>
<tr><td>sft_cfg7[1]=1’b1,
sft_cfg0[11]=1’b0,
fm_gpio_len[3:0]>8</td><td>FM_GPIOB [14]</td><td>I/O</td></tr>
<tr><td>(other)</td><td>GPIO[92](default)</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>E_MX31</td><td>226</td><td>n/a</td><td>I/O</td><td>ROM / SRAM / flash address bus bit [21], or GPIO[93]
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>pad_ctrl[4]=1’b1</td><td>656_DATA[6]</td><td>O</td></tr>
<tr><td>sft_cfg1[4]=1’b1,ROM/SD RAM non share</td><td>ROM / SRAM / flash address bus bit [21]</td><td>O</td></tr>
<tr><td>sft_cfg7[3:2]=2’b11</td><td>VDIN_DATA[1]</td><td>I</td></tr>
<tr><td>sft_cfg7[5:4]=2’b10</td><td>656_DATA[5]</td><td>O</td></tr>
<tr><td>sft_cfg7[1]=1’b1,
sft_cfg0[11]=1’b0,
fm_gpio_len[3:0]>8</td><td>FM_GPIOB [15]</td><td>I/O</td></tr>
<tr><td>(other)</td><td>GPIO[93](default)</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>E_MX32</td><td>227</td><td>n/a</td><td>I/O</td><td>ROM / SRAM / flash address bus bit [22], or GPIO[94]
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>pad_ctrl[4]=1’b1</td><td>656_DATA[5]</td><td>O</td></tr>
<tr><td>sft_cfg1[5]=1’b1,ROM/SD RAM non share</td><td>ROM / SRAM / flash address bus bit [22]</td><td>O</td></tr>
<tr><td>sft_cfg7[3:2]=2’b11</td><td>VDIN_DATA[2]</td><td>I</td></tr>
<tr><td>sft_cfg7[5:4]=2’b10</td><td>656_DATA[6]</td><td>O</td></tr>
<tr><td>sft_cfg0[14]=1’b1</td><td>TV_LCD_R_EXT[0]</td><td>O</td></tr>
<tr><td>sft_cfg7[1]=1’b1,
sft_cfg0[11]=1’b0,
fm_gpio_len[3:0]>8</td><td>FM_GPIOB [16]</td><td>I/O</td></tr>
<tr><td>(other)</td><td>GPIO[94](default)</td><td>I/O</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Symbol</th><th>256pin</th><th>216pin</th><th>I/O</th><th>Description</th></tr>
<tr><td>E_MX33</td><td>228</td><td>n/a</td><td>I/O</td><td>GPIO[95]
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>pad_ctrl[4]=1’b1</td><td>656_DATA[4]</td><td>O</td></tr>
<tr><td>sft_cfg7[3:2]=2’b11</td><td>VDIN_DATA[3]</td><td>I</td></tr>
<tr><td>sft_cfg7[5:4]=2’b10</td><td>656_DATA[7]</td><td>O</td></tr>
<tr><td>sft_cfg0[14]=1’b1</td><td>TV_LCD_R_EXT[1]</td><td>O</td></tr>
<tr><td>sft_cfg7[1]=1’b1,
sft_cfg0[11]=1’b0,
fm_gpio_len[3:0]>9</td><td>FM_GPIOB [17]</td><td>I/O</td></tr>
<tr><td>(other)</td><td>GPIO[95](default)</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>E_MX34</td><td>229</td><td>n/a</td><td>I/O</td><td>GPIO[96]
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>pad_ctrl[4]=1’b1</td><td>656_DATA[3]</td><td>O</td></tr>
<tr><td>sft_cfg7[3:2]=2’b11</td><td>VDIN_DATA[4]</td><td>I</td></tr>
<tr><td>sft_cfg7[5:4]=2’b11</td><td>656_DATA[6]</td><td>O</td></tr>
<tr><td>sft_cfg0[14]=1’b1</td><td>TV_LCD_G_EXT[0]</td><td>O</td></tr>
<tr><td>sft_cfg7[1]=1’b1,
sft_cfg0[11]=1’b0,
fm_gpio_len[3:0]>9</td><td>FM_GPIOB [18]</td><td>I/O</td></tr>
<tr><td>(other)</td><td>GPIO[96](default)</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>E_MX35</td><td>230</td><td>n/a</td><td>I/O</td><td>GPIO[97]
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>pad_ctrl[4]=1’b1</td><td>656_DATA[2]</td><td>O</td></tr>
<tr><td>sft_cfg7[3:2]=2’b11</td><td>VDIN_DATA[5]</td><td>I</td></tr>
<tr><td>sft_cfg7[5:4]=2’b11</td><td>656_DATA[7]</td><td>O</td></tr>
<tr><td>sft_cfg0[14]=1’b1</td><td>TV_LCD_G_EXT[1]</td><td>O</td></tr>
<tr><td>sft_cfg7[1]=1’b1,
sft_cfg0[11]=1’b0,
fm_gpio_len[3:0]>9</td><td>FM_GPIOB [19]</td><td>I/O</td></tr>
<tr><td>(other)</td><td>GPIO[97](default)</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>E_MX36</td><td>231</td><td>n/a</td><td>I/O</td><td>GPIO[98]
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>pad_ctrl[4]=1’b1</td><td>656_CLK</td><td>O</td></tr>
<tr><td>sft_cfg7[3:2]=2’b11</td><td>VDIN_DATA[6]</td><td>I</td></tr>
<tr><td>sft_cfg7[5:4]=2’b10</td><td>656_OUTCLK</td><td>O</td></tr>
<tr><td>sft_cfg0[14]=1’b1</td><td>TV_LCD_B_EXT[0]</td><td>O</td></tr>
<tr><td>sft_cfg7[1]=1’b1,
sft_cfg0[11]=1’b0,
fm_gpio_len[3:0]>9</td><td>FM_GPIOB [20]</td><td>I/O</td></tr>
<tr><td>(other)</td><td>GPIO[98](default)</td><td>I/O</td></tr>
</table></td></tr>
<tr><td>E_MX37</td><td>232</td><td>n/a</td><td>I/O</td><td>GPIO[99]
<table>
<tr><th>Priority selection</th><th>Function</th><th>dir</th></tr>
<tr><td>pad_ctrl[4]=1’b1</td><td>656_DATA[1]</td><td>O</td></tr>
<tr><td>sft_cfg7[3:2]=2’b11</td><td>VDIN_DATA[7]</td><td>I</td></tr>
<tr><td>sft_cfg0[14]=1’b1</td><td>TV_LCD_B_EXT[1]</td><td>O</td></tr>
<tr><td>(other)</td><td>GPIO[99](default)</td><td>I/O</td></tr>
</table></td></tr>
</table>

Symbol	256pin	216pin	I/O	Description
E_MX38	233	n/a	I/O	GPIO[100] Priority selection / Function / dir pad_ctrl[4]=1'b1 / 656_DATA[0] / O sft_cfg7[3:2]=2'b11 / VDIN_CLK / I sft_cfg7[11:8]=4'b1001 / VGA_CLK / O (other) / GPIO[99](default) / I/O
PLL_AVDD	235	197	S	Servo PLL 3.3V power
LPFO	236	198		NC pin
LPFN	237	199		NC pin
VREFO	238	200	A	
PDFLT	239	201	A	
FDFLT	240	202	A	
LPFNIN	241	203	A	
LGIN	242	204	A	
PLL_DS_AVSS	243	205	S	Servo PLL/Data-slicer ground
RFI	244	206	A	
CNIN	245	207	A	
SLVL	246	208	A	
DS_AVDD	247	209	S	Servo Data slicer 3.3V power
RF_AVDD	248	210	S	Servo RF 3.3V power
GMRES	249	211	-	External reference resistor input.
AGCCAP	250	212	-	External AGC capacitor connected to ground.
RFRP	251	213	O	RFRP signal output.
RFO	252	214	O	RF signal output.
FLTIP	253	215	I	Differential RF equalizer input #P
FLTIN	254	216	I	Differential RF equalizer input #N
AGCON	255	1	O	Differential AGC output #N
AGCOP	256	2	O	Differential AGC output #P
RFIP	1	3	I	Differential RF signal input.
RFIS	2	4	I	Single-ended RF equalizer input.
RFSUM	3	5	O	RF summing amplified output.
DPDA	4	6	I	AC coupled RF inputs for the DPD, from the main beam photo detector.
DPDB	5	7	I	
DPDC	6	8	I	
DPDD	7	9	I	
DVDD	8	10	I	DVD RF inputs, from the main beam photo detector.
DVDC	9	11	I	
DVDB	10	12	I	
DVDA	11	13	I	
CDB	12	14	I	CD RF inputs, from the main beam photo detector.
CDA	13	15	I	
CDF	14	16	I	CD tracking error inputs, from the sub-beam photo detector.
CDE	15	17	I	
RF_AVSS	16	18	S	Servo RF ground
APC_AVSS	17	19	S	Servo APC ground

Symbol	256pin	216pin	I/O	Description
DVDLDO	18	20	O	DVD APC output.
CDLDO	19	21	O	CD APC output.
DVDMDI	20	22	I	DVD APC input from monitor photo diode.
CDMDI	21	23	I	CD APC input from monitor photo diode.
APC_AVDD	22	n/a	S	Servo APC 3.3V power
SRV_AVDD	23	n/a	S	Servo analog 3.3V power
APC_SRV_AVDD	n/a	24	S	Servo APC and analog 3.3V power (216pin only)
V21	24	25	-	Reference DC bias voltage.
R33K	25	26	-	External reference resistor input.
V165	26	27	-	Reference DC bias voltage.
SVOTST	27	28	O	RF peak hold external capacitor
RFRPPH	28	29	O	RFRP peak hold signal output.
RFRPBH	29	30	O	RFRP bottom hold signal output.
RFRPMEAN	30	31	O	RFRP mean signal output.
SBADPH	31	32	O	Sub-beam adds peak hold signal output.
SBAD	32	33	O	Sub-beam adds signal output.
FEO	33	34	O	Focus error signal output.
TEO	34	35	O	Tracking error signal output.
TEOLP	35	36	A	
OPVIP	36	37	I	Op-amp 1 positive input.
OPVIN	37	38	I	Op-amp 1 negative input.
OPVOP	38	39	O	Op-amp output.
SRV_AD_AVSS	39	n/a	S	Servo/ADC analog ground
VRGD	40	n/a	A	
SRV_AD_AVSS_VRGD	n/a	40	S	Servo/ADC analog ground (216pin only)
AD_DA_AVDD	41	41	S	Servo ADC/DAC 3.3V power
DATEO	42	42	A	
DAFEO	43	43	A	
DA_AVSS	44	44	S	Servo DAC ground

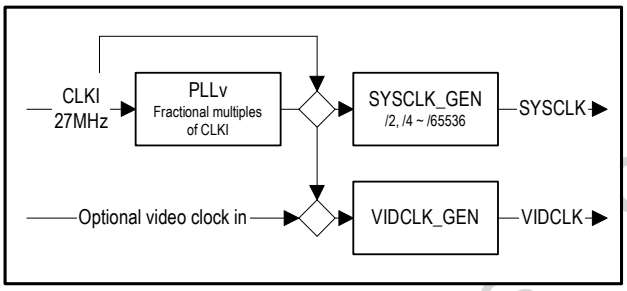
Note: Please reference SPHE8281A servo datasheet for servo related information.

5.FUNCTIONAL DESCRIPTIONS

SPHE8281A is a highly integrated system-on-chip DVD player ASIC design. It includes DVD/CD servo controller, host controller, MPEG1/2/4 video decoder, programmable audio decoder, programmable peripheral controller, audio ADC and multi-format TV-encoder on a single chip.

5.1. PLL and ClockGen

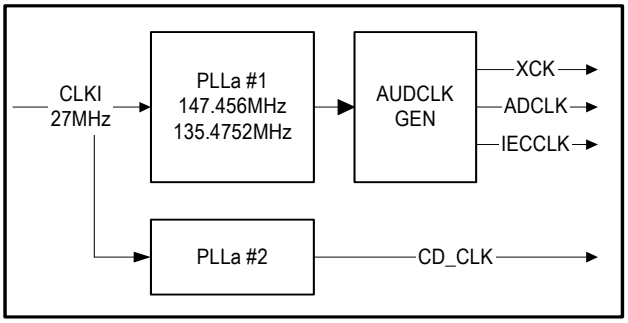
SPHE8281A contains multiple PLLs to generate system clock (PLLv) and audio reference clocks (PLLa). All the PLLs reference a single external 27MHz clock or crystal to generate all the required clocks. System clock is then derived from division of the PLLv output.



Some pre-defined PLLv/SYSCLK frequencies are listed below:

SYSCLK Frequency	PLLV Frequency
81MHz	324MHz
87.75MHz	351MHz
94.5MHz	378MHz
101.25MHz	405MHz
108MHz	216MHz
114.75MHz	459MHz
121.5MHz	486MHz
128.25MHz	256.5MHz
135MHz	270MHz

PLLa supports two center frequencies (for both 48kHz family and 44.1kHz family) and generates required audio clocks from the audio system clock.



5.2. Power Control

SPHE8281A provides various levels of power-control mechanism in order to achieve minimum power consumption.

- Automatic power-save:
  Most hardware modules are automatically power-saved when not operating.
- Module-level stop-operation:
  SPHE8281A provides a function to turn off specific module from operating. Without explicit wake-up, the hardware module will remain static and consume very little power.
- System-level doze:
  For maximum power-saving, firmware could fine-tune system performance according to system task.

5.3. Embedded 32-bit RISC Controller

SPHE8281A includes a powerful 32-bit RISC processor. This RISC processor is utilized to manage decoding tasks as well as UI tasks. It can access to all the memory and devices, cooperate between processor systems. Audio decoder and I/O processor handshake with RISC processor through the mailbox registers.

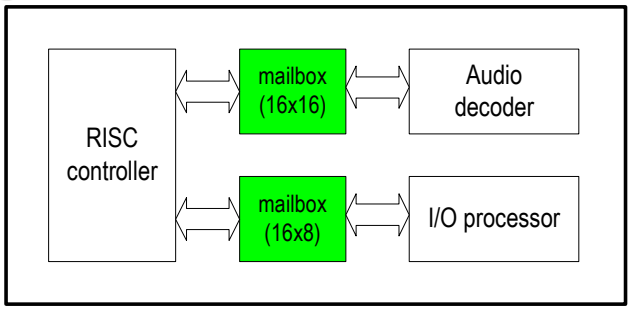


Figure 5-1: Communication between processors

The RISC processor is equipped with instruction and data caches. These caches can accelerate accesses to the SDRAM or ROM cacheable regions.

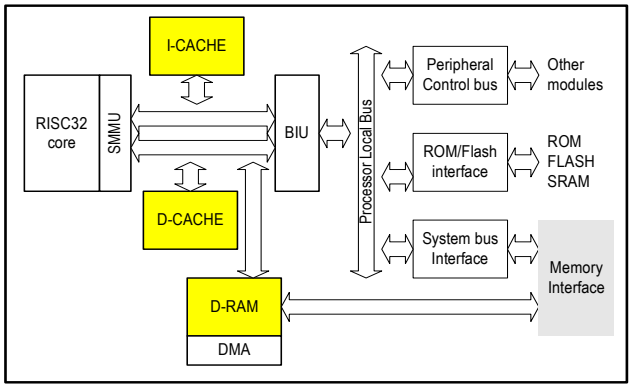


Figure 5-2: RISC subsystem

Table: RISC processor local memory configuration

Memory	Specification
I-Cache	8kbyte (2-way set associated)
D-Cache	4kbyte (direct-mapped)
D-RAM/DMA	1kbyte scratch buffer

The RISC sub-system is able to bootstrap from multiple sources. In typical application the RISC processor boots from external ROM device #1. Besides that, it also supports standalone booting without pre-loaded firmware.

5.4. RISC Interface

RISC controllers interface to system via various interface control modules. These interface modules are mapped to the processor memory map and firmware could operate on them via typical memory accesses. These controllers include:

- ROM/FLASH/SRAM (RFS) controller
- RISC Memory Interface controller (SDRAM)
- Peripheral control interface

The RISC memory mapping of these controllers is shown in following table:

Table: RISC memory mapping

Memory Range	Description
8000_0000~87ff_ffff	SDRAM (cached)
a000_0000~a7ff_ffff	SDRAM (uncached)
8800_0000~8fff_ffff	ROM/FLASH/SRAM (cached)
a800_0000~afff_ffff	ROM/FLASH/SRAM (uncached)
bffe_8000~bffe_ffff	Peripheral control registers
bfff_0000~bfff_03ff	DMA buffer

In additional to that, SPHE8281A includes dedicated RISC peripherals to assist the system tasks:

- Device interrupt controller:
  Device interrupt controller takes care of interrupt sources from on-chip devices and off chip sources. For each interrupt source the firmware is able to configure the interrupt behavior between edge-trigger and level-sensitive mode.
- Watchdog:
  Watchdog keeps monitoring RISC behavior and whenever firmware is in a deadlock or ill-behaved, the watchdog would trigger system-wise reset and keep the application functioning continuously.
- Timers
  There are 4-channel timers and 2 cascade counters for timed tasks. During A/V decoding, system time counters are utilized to synchronize audio and video playback timing.

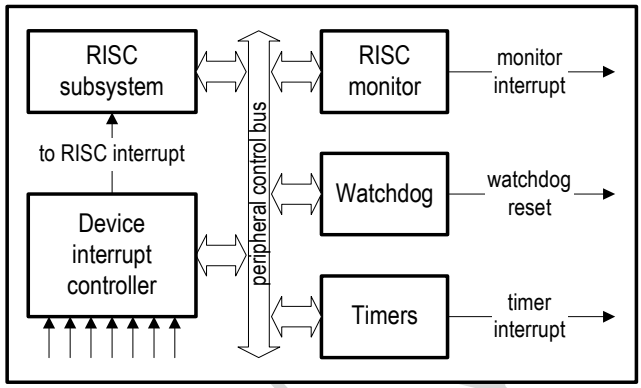


Figure 5-3: RISC dedicated hardware

Table: Device interrupt controller sources

Symbol	Description
INT_WDOG	Watchdog interrupt (if reset disabled)
INT_HSYNC	Interrupt when horizontal resync
INT_VSYNC	Interrupt when enter vertical resync
INT_FLD_ACT	Interrupt when enter active region
INT_FLD_SYNC	Interrupt when leave active region
INT_HOST	Host device interrupt
INT_TIMER0	Timer 0 interrupt
INT_TIMER1	Timer 1 interrupt
INT_TIMER2A	Timer 2 scale interrupt
INT_TIMER2B	Timer 2 count interrupt
INT_TIMER3A	Timer 3 scale interrupt
INT_TIMER3B	Timer 3 count interrupt
INT_TIMERW	Watchdog timer interrupt
INT_UART0	UART0 interrupt
INT_UART1	UART1 interrupt
INT_VDP0	Video decoder interrupt
INT_DSP	DSP interrupt
INT_EXT0	External interrupt #0
INT_EXT1	External interrupt #1
INT_EXT2	External interrupt #2
INT_EXT3	External interrupt #3
INT_IOP	IOP interrupt
INT_AUD	Audio hardware interrupt

5.5. ROM/Flash/SRAM Controller

The SPHE8281A provides flexible connections to external ROM, Flash or SRAM (RFS). It can support up to 4 external RFS devices by using different chip-selects (R_CS_B[3:0]). The firmware can configure RFS memory anchor registers and map these devices into locations of RISC memory space. For each memory space it can be in flash mode or in ISA mode. In FLASH mode the access timing is decided by wait-state setting, while in ISA mode the controller will reference external IO_CHRDY input.

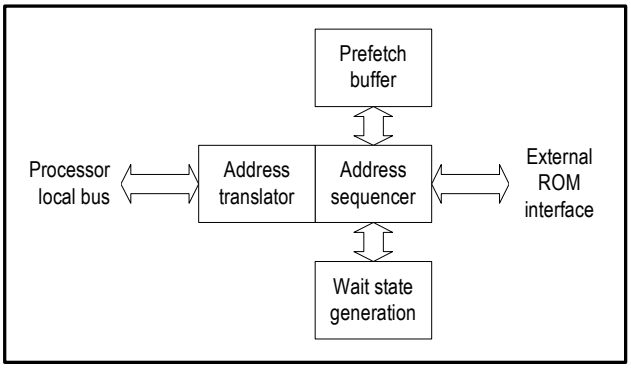


Figure 5-4: ROM/FLASH/SRAM controller

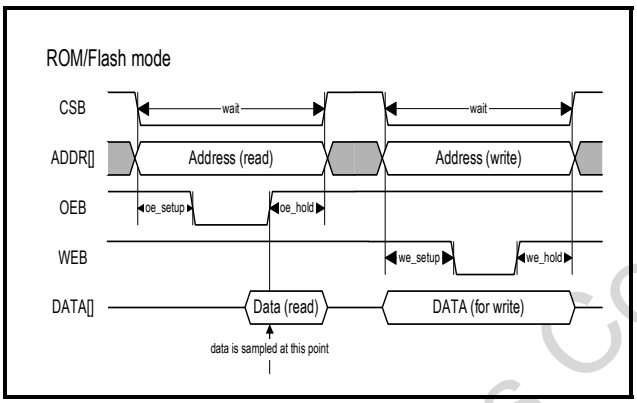


Figure 5-5: ROM/FLASH/SRAM mode timing

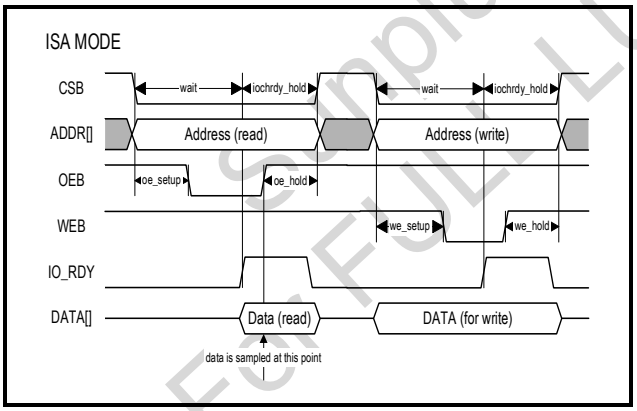


Figure 5-6: ISA mode timing

5.6. RISC Memory Interface

RISC memory interface provides a fast-path between processor local bus and system memory bus. Local bus transactions are mapped to system memory bus tasks.

5.7. Peripheral Control Interface

RISC firmware controls on-chip devices (such as video decoder, audio decoder..) by a dedicated peripheral control interface. Firmware controls the hardware behavior by writing to specific hardware registers using this interface.

5.8. CSS/CPPM

SPHE8281A have built-in CSS and CPPM hardware support. For CSS the system supports accelerated DMA. For CPPM the system supports C2_D/C2_E and C2_DCBC functions.

5.9. MPEG Video Decoder

The system incorporates a powerful MPEG video decoding datapath and provides real-time video decoding of MPEGI/II bitstream. The bitstream can come from Servo hardware, ATAPI devices and other interfaces. This enables various applications to be built over SPHE8281A such as real-time broadcasting over Ethernet.

The video decoder is a hardwired MPEG1/2/4 datapath. The system architecture is as in the figure. RISC subsystem is in charge of de-multiplexing the data and buffering formatted video data into video bitstream buffer resided in external SDRAM. Upon correct timing video decoder will decode the bitstream and write back reconstructed video frame for playback.

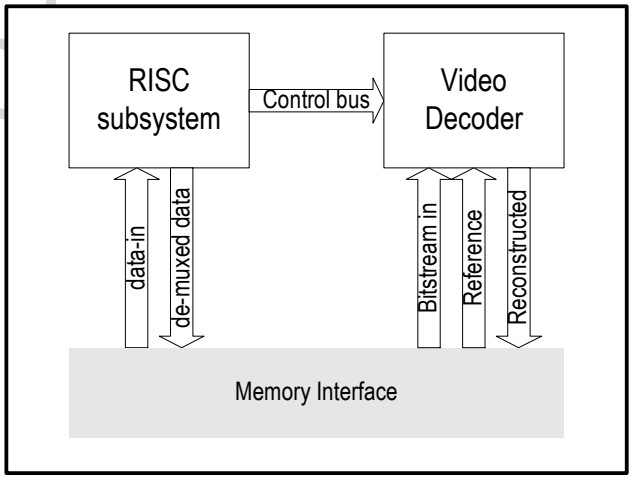


Figure 5-7: Interface between RISC and Video decoder

Advanced video decoding and display control mechanism is included to prevent tearing effect.

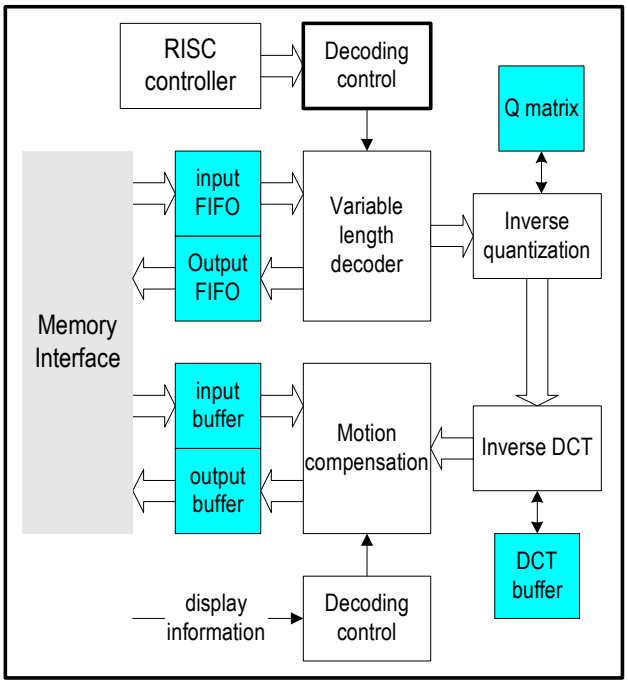


Figure 5-8: Architecture of video decoding pipeline

5.10. Graphics Engine BondyPro®

For thin-client or set-top box applications, 2D graphics capabilities are key to system performance. This graphics engine is able to perform fast BitBlt and 2D drawing functions. The graphics engine is combined with 2 parts: graphics command interpreter and graphics datapath. Upon receiving command from RISC, interpreter will send micro-commands to graphics datapath, where raster operations are executed.

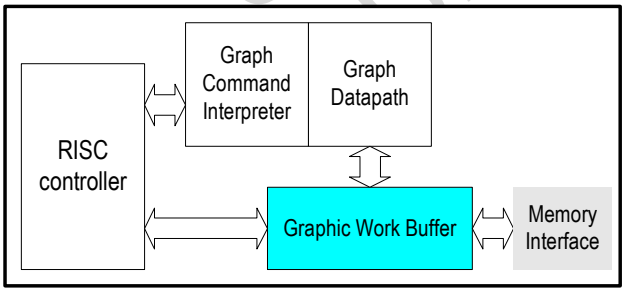


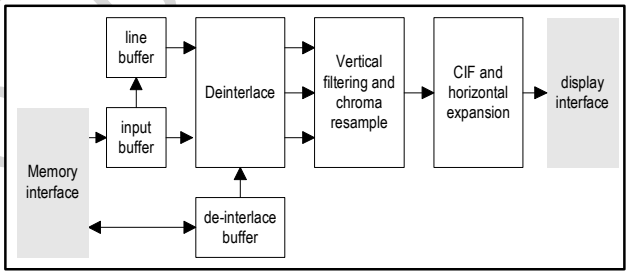
Figure 5-9: BondyPro® architecture

5.11. Video Post Processing

SPHE8281A includes powerful video-post-processing facilities to provide high video quality. It perform following functions:

- YUV411, YUV420, YUV422 and 8-bit indexed color
- SIF to CCIR601 interpolation
- MPEG1 CIF filter
- MPEG1/2 chroma vertical interpolation
- Up to 1/2x horizontal decimation
- Up to 1/512x vertical decimation
- Up to 1024x horizontal expansion
- Up to 1024x vertical expansion
- Powerful de-interlacing hardware
- Pan and scan function
- De-flicker during interlaced display
- Video contrast/bright/color enhancement

During runtime video post-processing hardware will fetch video sources from framebuffer and process the data as in the following figure.



5.12. Audio Digital Signal Processor

The SPHE8281A contains a high-performance 24-bit audio DSP optimized for embedded system applications. The DSP processor can fetch operands from two memories and perform multiplication-and-accumulation (MAC) in one cycle. During execution the DSP fetches instruction from main-memory or IROM, at the same time the ICACHE will store the LRU instructions. Data are loaded from and to main-memory by using the cycle-stealing DMA channels. There are 3 independent cycle-stealing DMA channels that allow DSP run without stalled by memory access.

The DSP works closely with RISC processors by using mailbox registers or shared-memory protocol. When downloaded with different firmware the DSP could support multi-standard audio and act as an accelerator for RISC in some case.

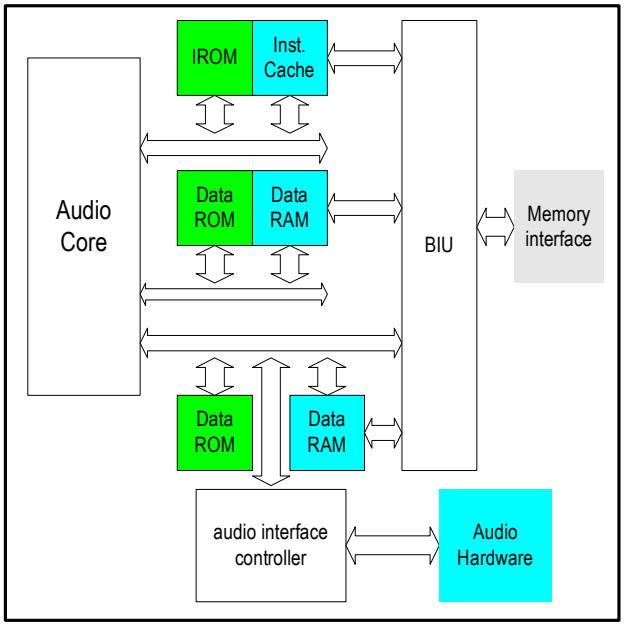


Figure 5-10: Audio DSP architecture

5.13. Audio Interface

The audio interface is in charge of servicing DSP and maintaining all audio-related tasks. It will buffer the DSP processed audio playback data and format them to audio DAC required format. Up to 10 channel of digital audio are supported in I2S or normal mode.

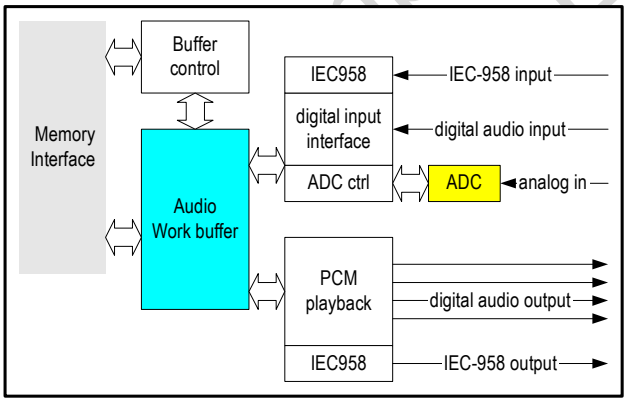


Figure 5-11: Audio Interface architecture

SPHE8281A support following audio DAC format combinations:

	32k	44.1k	48k	64k	88.2k	96k	192k
256fs	Ok	Ok	Ok	Ok	Ok	Ok	Ok
384fs	Ok	Ok	Ok	Ok	Ok	Ok	Ok

Data Alignment	Left adjust, I2S, normal format
LRCK frame width	16b, 24b, 32b, 64b
Data bits	16b, 18b, 20b, 24b
Data sign extension	Zero-extended, sign-extended

5.14. Audio ADC

The embedded ADC is a 2-channel 64fs over-sampling ADC of 12-bit audio quality. The audio ADC supports both MIC (mono) and line-in (stereo) modes.

5.15. I/O Processor

The SPHE8281A includes an 8-bit micro-controller to help RISC controller handling I/O jobs. IR, VFD and other slow devices can be interfaced using this I/O processor.

5.16. SDRAM Controller

SDRAM controller in SPHE8281A is designed to meet both flexible and powerful requirements. It can meet different SDRAM timing requirement while achieving maximum performance. SDRAM tasks are optimized for maximum system performance.

For power-constrained applications SPHE8281A also implements SDRAM power-down modes to save dynamic operating power.

5.17. Sub-picture Decoder

For DVD and SVCD sub-picture content SPHE8281A includes an advanced multi-format sub-picture decoder. It supports vertical interpolation for PAL/NTSC translation or special effect.

5.18. On Screen Display

The on screen display (OSD) function of the SPHE8281A provides an overlay bitmap graphics on the final TV display. Applications can use this function to display specific information over the video display plane without operating on the video source.

The SPHE8281A can display multiple OSD regions on a single display frame, where every OSD regions can be in different size, location and color format. The OSD hardware supports 4, 16, 256 indexed color or 16-bit direct color. OSD regions are stored in main memory before display. During display, OSD decoder would read these header and data and interpret to be a graphic data that overlay with video to be output to the display interface.

5.19. Display Interface

The display interface of SPHE8281A mixs the video content generated from video-post-processing, sub-picture-decoder and on-screen-display modules. It also performs content cropping, underflow and overflow correction and overall hue / brightness / contrast adjustment.

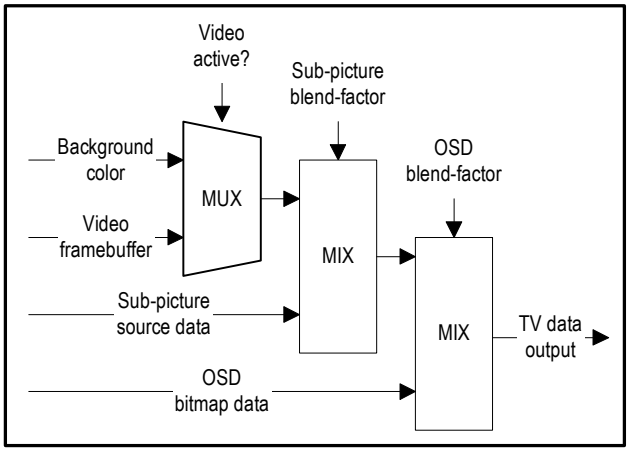


Figure 5-12: Display pipeline

The video enhancement process is show in following figure:

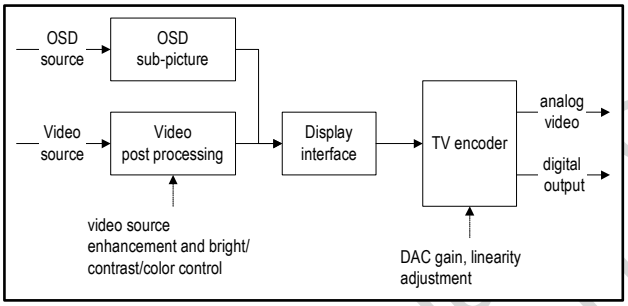


Figure 5-13: Display pipeline

5.20. Video DAC

SPHE8281A contains 6-channel (4-channel for 216pin package) 10-bit high-speed current-source DACs operating from 27MHz to 60MHz (for 480p/576p or SVGA display). The DAC outputs can drive a 37.5Ohm load directly.

5.21. USB Host Controller

SPHE8281A integrated an USB v1.1 UHCI compliant host controller. By utilizing this host controller, SPHE8281A can access to USB based flash discs and keyboard/mouse devices.

5.22. ATAPI Interface

SPHE8281A also supports ATAPI host interface directly without glue logic. Although the SPHE8281A has integrated DVD/CD servo logics, with this interface the application could support other ATA/ATAPI compliant devices directly. The ATAPI/IDE interface is a standard ATA-5 host interface capable of PIO mode 2 to PIO mode 4 to external devices.

5.23. GPIO

In SPHE8281A almost every pin that related to selectable features can serve as general-purpose input-output (GPIO) control function. When a pin is programmed to this mode, the RISC controller or the I/O processor can take full control over the direction and output level.

6.ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}	-0.3 to 5.5	V
Voltage on V_{DDIO} supply relative to V_{SS}	V_{DDIO}	-0.3 to 3.45	V
Voltage on V_{DDK} supply relative to V_{SS}	V_{DDK}	-0.3 to 1.90	V
Storage Temperature	T_{STG}	-55 to 150	°C
Soldering Temp. (Max. Time)	T_{SOLDER}	240 (for 5 Sec. Max.)	°C
Short circuit current	I_{OS}	50	mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6.2. DC Operating Conditions

Recommended Operating Conditions (Voltage referenced to VSS=0V, TA=-0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Units
Voltage on V_{DDK} supply relative to V_{SS}	V_{DDK}	1.70	1.80	1.90	V
Voltage on V_{DDIO} supply relative to V_{SS}	V_{DDIO}	3.15	3.30	3.45	V
Input logic high voltage	V_{IH}	2.0	-	5.5	V
Input logic low voltage	V_{IL}	-0.3	-	0.8	V
Output logic high voltage	V_{OH}	2.4	-	-	V
Output logic low voltage	V_{OL}	-	-	0.4	V
Input leakage current	I_L	-10	-	10	uA

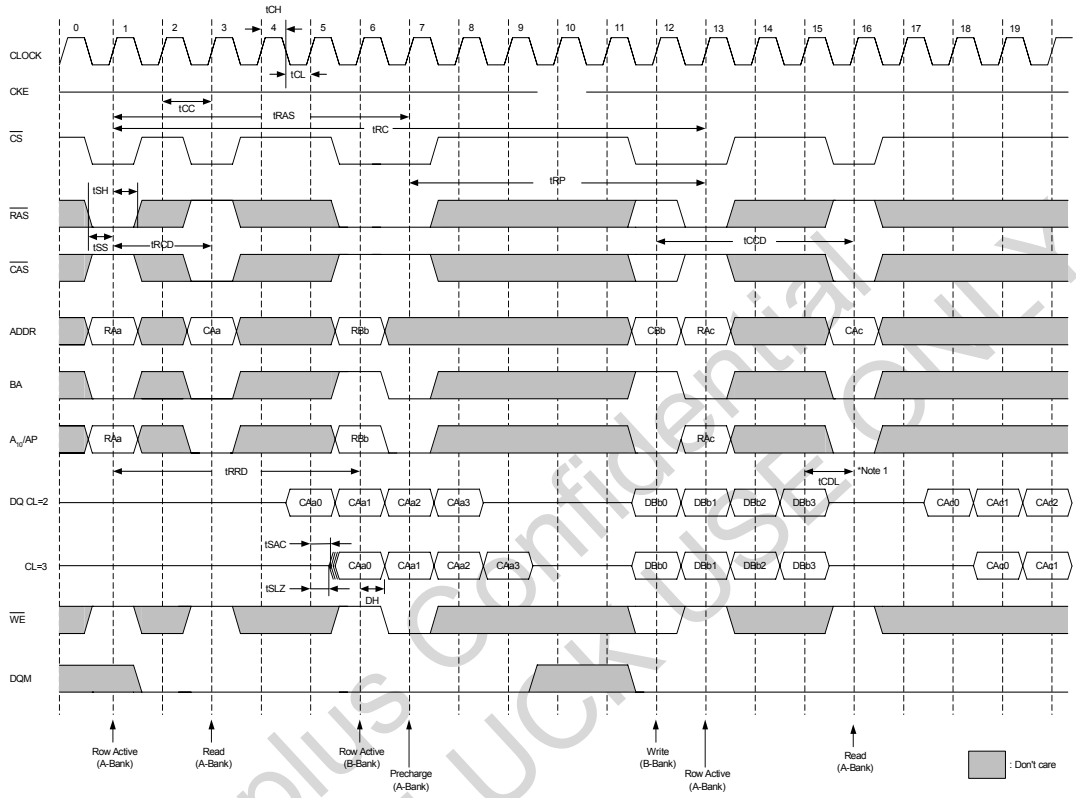
6.3. Capacitance

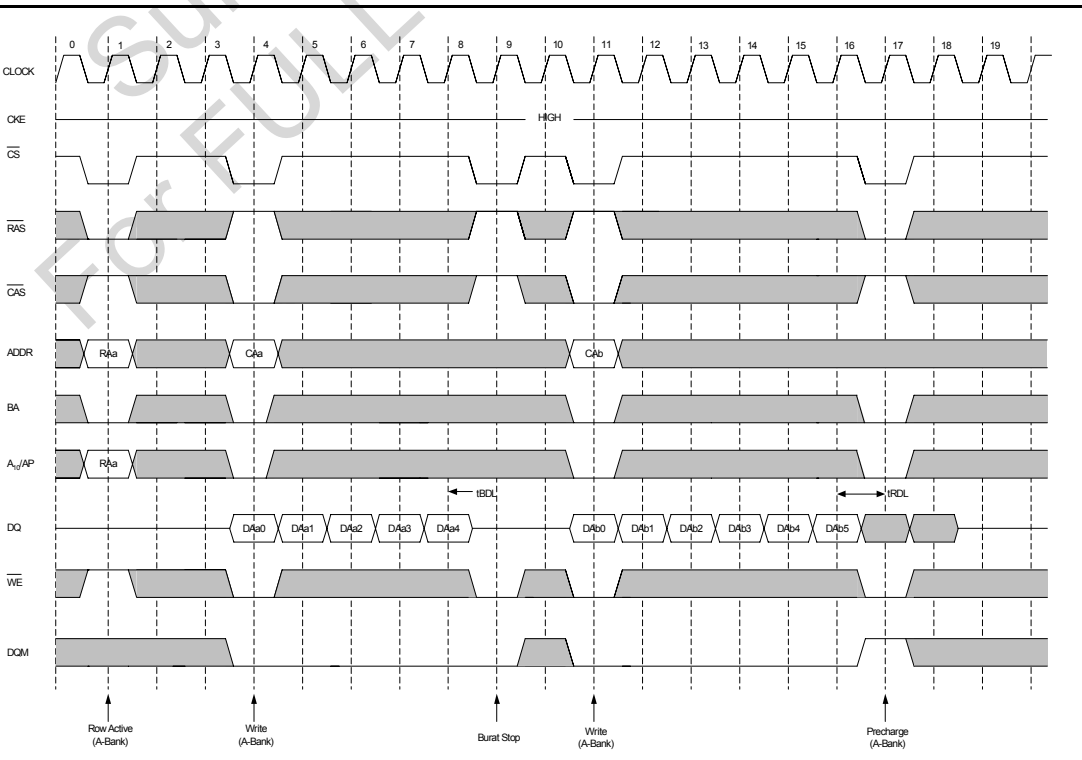
(V_{DDIO}=3.3V, TA=24°C, f=108MHz, V_{REF}=1.4V+-200mV)

Parameter	Symbol	Min.	Typ.	Max.	Units
Input pin capacitance	C_{IN}	-	3.5	-	pF
Input pin capacitance	C_{OUT}	-	3.5	-	pF
Bidirectional pin capacitance	C_{BIDIR}	-	3.5	-	pF

6.4. AC Characteristics

6.4.1. SDRAM interface timing diagrams





(Recommended condition for DVD playback is listed in typical condition with f=121.5MHz)

Parameter	Symbol	Min.	Typ.	Max.	Units
Row active to row active delay	t_{RRD}	1	2	4 *1	System clock cycle
RAS to CAS delay	t_{RCD}	1	2	4 *1	System clock cycle
Row precharge time	t_{RP}	1	2	4 *1	System clock cycle
Row active time	t_{RAS}	1	5	8 *1	System clock cycle
Row cycle time	t_{RC}	1	8	32 *1	System clock cycle
Last data in to new column address delay	t_{CDL}	1	1	4 *1	System clock cycle
Column address to column address delay	t_{CCD}	1	1	1	System clock cycle
CLK cycle time *2	t_{CC}	6	8.2	1000	ns
CLK to valid SDRAM output delay *2	t_{SAC}	-	6.0	6.5	ns
SDRAM output data hold time *2	t_{OH}	1	2	-	ns
CLK high pulse width *3	t_{CH}	-	3	-	ns
CLK low pulse width *3	t_{CL}	-	3	-	ns
CLK to SDRAM output Low-Z	t_{SLZ}	-	1.0	(t_{CC})	ns
CLK to SDRAM output High-Z	t_{SHZ}	-	6.0	(t_{SAC})	ns

Note: 1.Using maximum values may limit system performance.
2.Width of data window can be estimated from (t_{CC}-t_{SAC}+t_{OH}).
3.Width of clock pulse depends on system clock cycle.

6.4.2. ROM / flash interface timing diagrams

ROM Compatible Mode

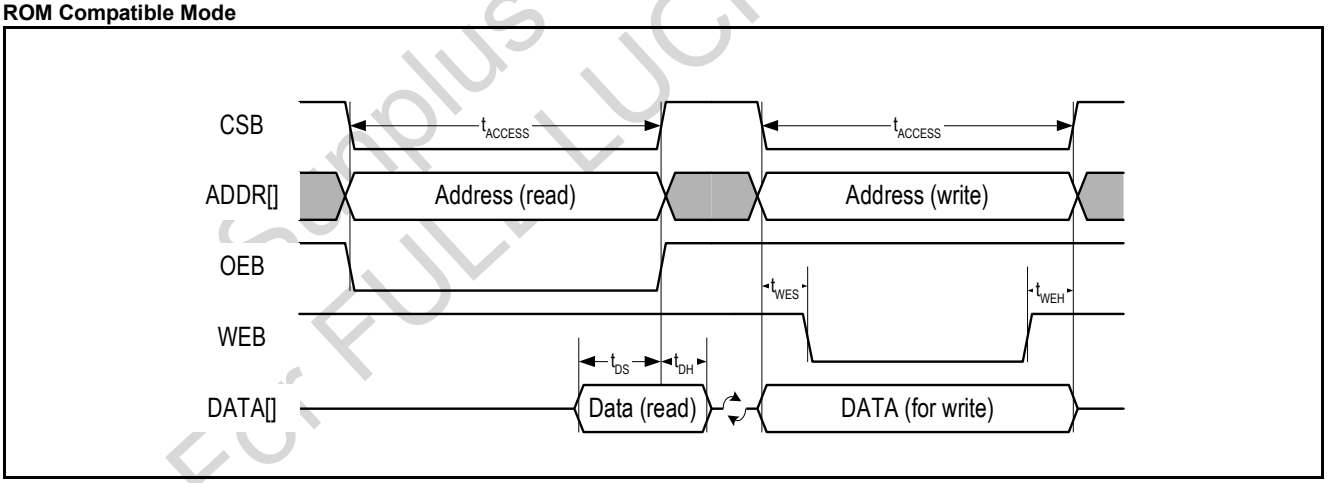


Figure 6-1: ROM / flash interface ROM mode access timing

Parameter	Symbol	Min.	Typ.	Max.	Units
ROM / SRAM / flash access time	t_{ACCESS}	2	8 *1	31	System clock cycle
Data setup time for read	t_{DS}	5	-	-	ns
Data hold time for read	t_{DH}	0	-	-	ns
Address/data setup time before write strobe	t_{WS}	0	1	31	System clock cycle
Address/data setup time after write strobe	t_{WH}	0	1	31	System clock cycle

Note: Recommended value when f=121.5MHz

ISA Compatible Mode

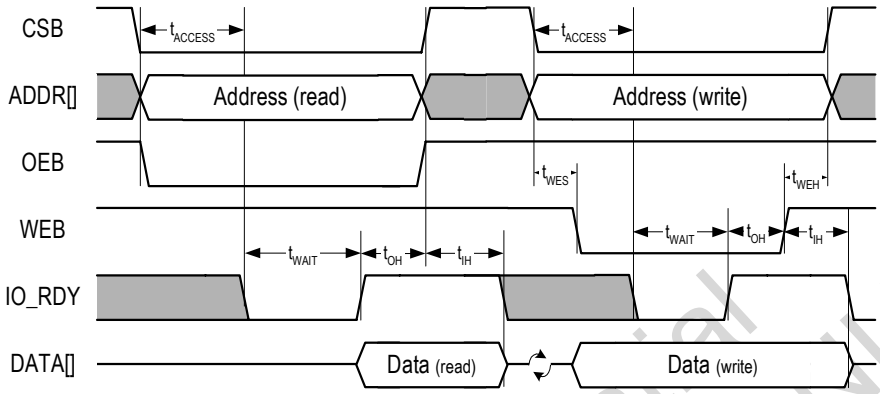


Figure 6-2: ROM / flash interface ISA mode access timing

Parameter	Symbol	Min.	Typ.	Max.	Units
ISA access time *1	t_{ACCESS}	2	-	31	System clock cycle
IO_RDY wait time	t_{WAIT}	0	-	1000	ns
Output hold time	t_{OH}	1	-	-	System clock cycle
Input hold time	t_{IH}	0	-	-	ns
Address/data setup time before write strobe	t_{WS}	0	1	31	System clock cycle
Address/data setup time after write strobe	t_{WH}	0	1	31	System clock cycle

Note: After this period of time IO_RDY_B must be stable and indicates correct status of target device.

6.4.3. Audio interface timing diagrams

Some audio interface configuration timing diagrams are shown below.

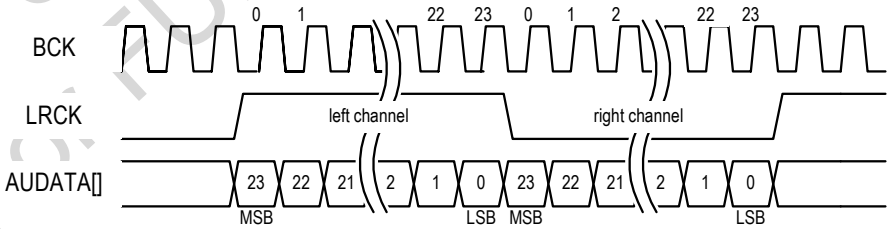


Figure 6-3: Normal mode / 24bit data / 24bit frame / MSB first

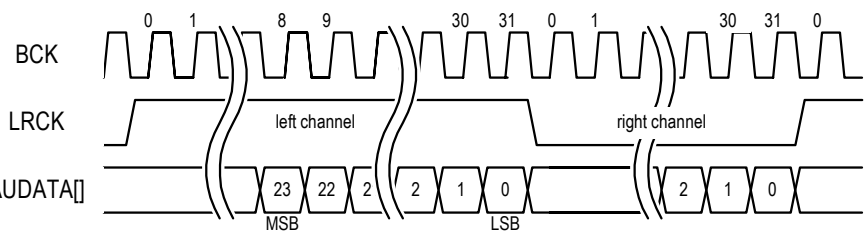


Figure 6-4: Right justified (normal) mode / 24bit data / 32bit frame / MSB first

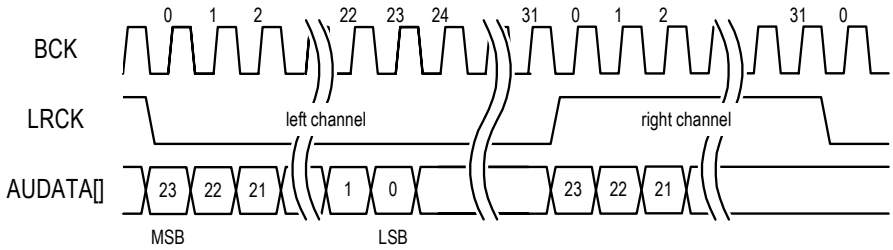


Figure 6-5: Left justified mode / 24bit data / 32bit frame / MSB first

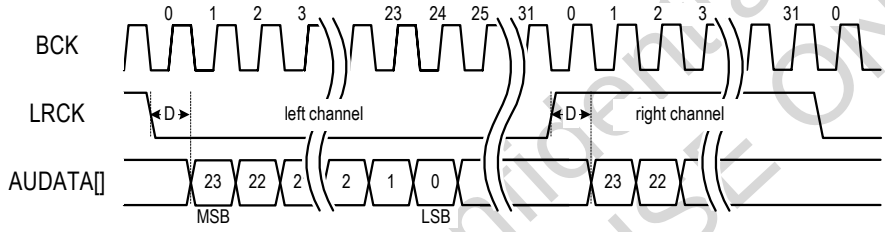


Figure 6-6: I²S mode / 24bit data / 32bit frame

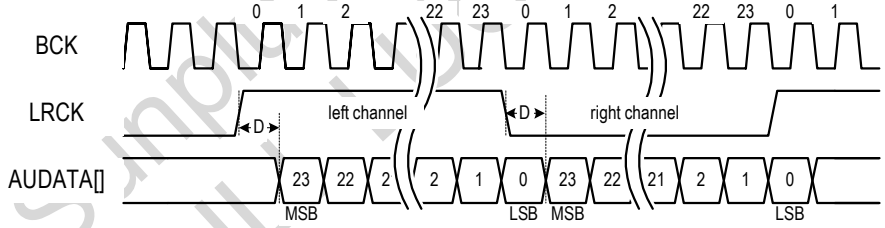


Figure 6-7: I²S mode / 24bit data / 24bit frame

Parameter	Symbol	Min.	Typ.	Max.	Units
BCK rising to LRCK / AUDATA transition	t_S	-	0.5	-	System clock cycle

6.4.4. Video timing diagrams

Interlaced Modes

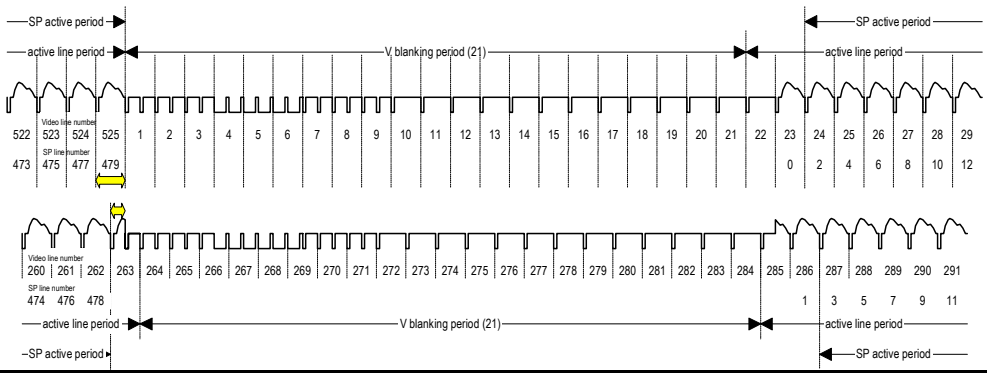


Figure 6-8: NTSC (480i) timing diagram

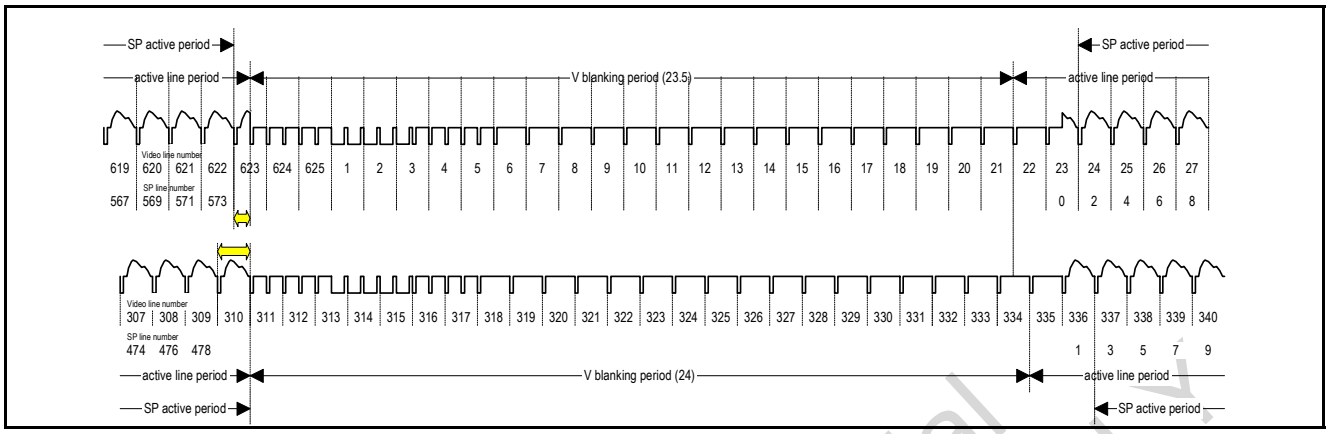


Figure 6-9: PAL (576i) timing diagram

Progressive Modes

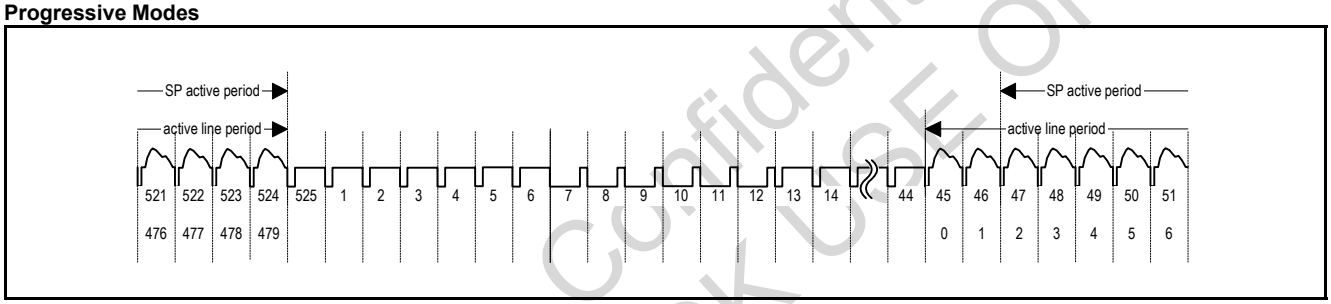


Figure 6-10: NTSC (480p) timing diagram

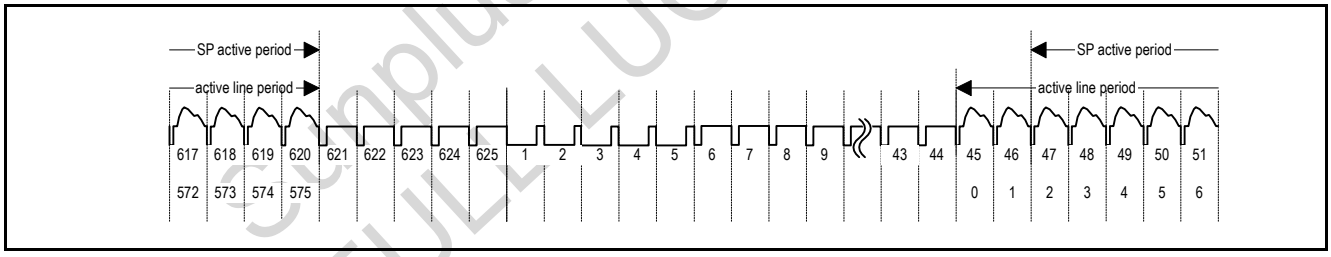
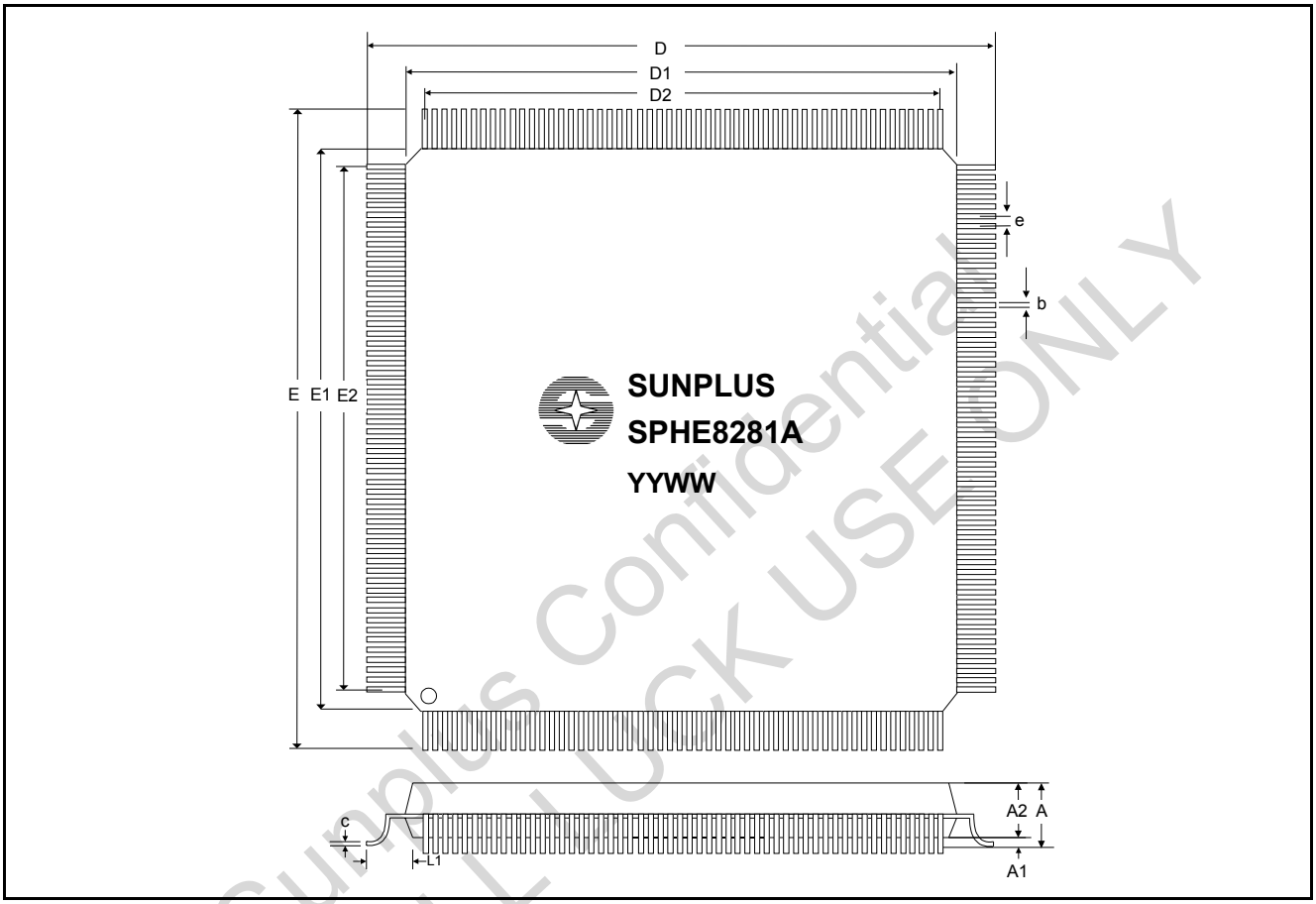


Figure 6-11: PAL (576p) timing diagram

7.PACKAGE/PAD LOCATION

7.1. Outline Dimensions

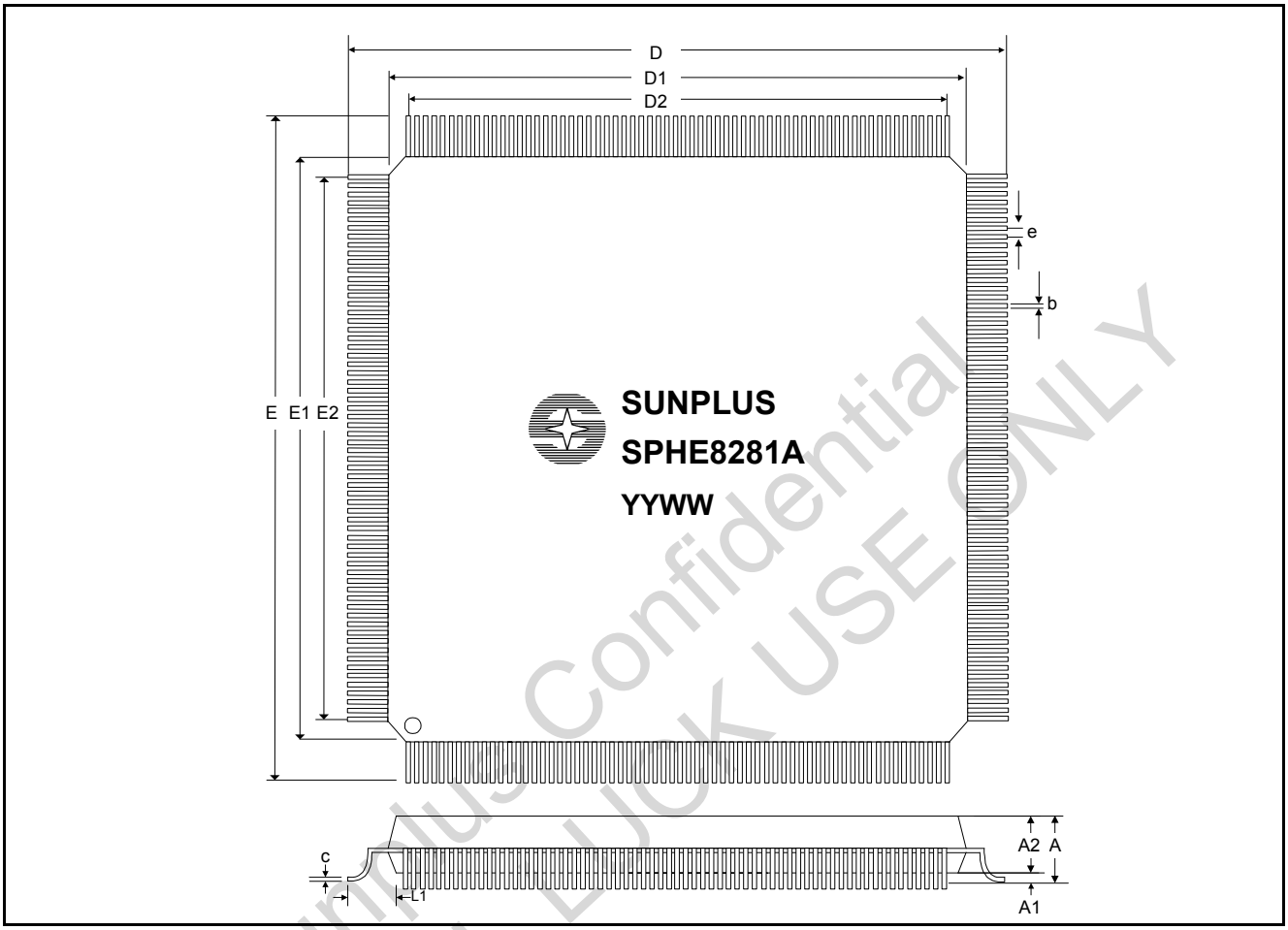
7.1.1. 216-pin LQFP



Symbol	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
D	26.00 BSC.	26.00 BSC.	26.00 BSC.
D1	24.00 BSC.	24.00 BSC.	24.00 BSC.
E	26.00 BSC.	26.00 BSC.	26.00 BSC.
E1	24.00 BSC.	24.00 BSC.	24.00 BSC.
R2	0.08	-	0.20
R1	0.08	-	-
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ3	11°	12°	13°
c	0.09	-	0.20
L	0.45	0.60	0.75
L1	1.00 REF	1.00 REF	1.00 REF
S	0.20	-	-

Unit: Millimeter

7.1.2. 256-pin LQFP



Symbol	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
D	30.00 BSC.	30.00 BSC.	30.00 BSC.
D1	28.00 BSC.	28.00 BSC.	28.00 BSC.
E	30.00 BSC.	30.00 BSC.	30.00 BSC.
E1	28.00 BSC.	28.00 BSC.	28.00 BSC.
R2	0.08	-	0.20
R1	0.08	-	-
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ3	11°	12°	13°
c	0.09	-	0.20
L	0.45	0.60	0.75
L1	1.00 REF	1.00 REF	1.00 REF
S	0.20	-	-

Unit: Millimeter

7.2. Feature Comparison Between Packages

Feature	SPHE8281A 216 LQFP	SPHE8281A-U 216 LQFP	SPHE8281A 256 LQFP	SPHE8281A-U 256 LQFP
USB	×	✓	×	✓
SDRAM bus width	16b	16b	16b or 32b	16b or 32b
SDRAM component	1Mx16 or 4Mx16	1Mx16 or 4Mx16	1Mx16 ~ 8Mx16	1Mx16 ~ 8Mx16
Audio DAC channels	Up to 8 channels	Up to 8 channels	Up to 10 channels	Up to 10 channels
Video DAC channels	4 channels	4 channels	6 channels	6 channels
De-interlace	×	×	✓ (with 32b SDRAM)	✓ (with 32b SDRAM)
Card-reader function	minimum	minimum		
On-chip ADC	no OP	no OP	with built-in OP	with built-in OP

8.DISCLAIMER

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9.REVISION HISTORY

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