DATA SHEET

凌陽科技
SUNPLUS

SPL081A

Low Voltage 7KB LCD Controller

AUG. 27, 2001

Version 1.1

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LOW VOLTAGE 7KB LCD CONTROLLER

1. GENERAL DESCRIPTION

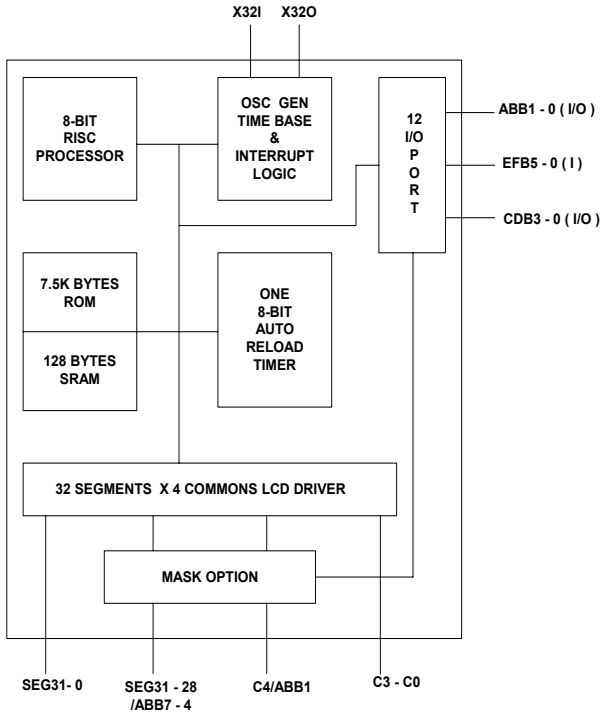
SPL081A, a special designed CMOS 8-bit microprocessor by Sunplus, offers the best cost/performance ratio in the industry. It combines RAM, ROM, I/Os, an interrupt controller, and an automatic display controller/driver in a small package. One of its extraordinary features is the capability of operating in low voltage range, from 1.2V - 1.7V. The Power Down Mode keeps LCD being displayed when CPU is in standby mode, but consumes only less than 3.5μA. Not only SPL081A is capable of displaying LCD, but it also can process complex instructions and functions as well. The development team has designed SPL081A to cover many application fields such as calculator, watch and other LCD related products required only one battery supply.

2. FEATURES

- Built-in 8-bit RISC processor
- 128-byte SRAM
- 7.5K-byte ROM
- CPU frequency: 150KHz, 300KHz or 500KHz (mask option) @ 1.5V (dependent VDD)
- Built-in RC oscillator
- Built-in 32.768KHz oscillator circuit for real clock function
- Watch dog mode (1Hz or 0.5Hz)
- Low operating voltage: 1.2V - 1.7V
- Low standby current, I_{STBY} < 1μA
- LCD matrix: 28 - 32 segments, 4(or 5) commons defined as I/O;
- 12 general I/O pins (segment 29, 30, 31, 32 can be ABB1 can be optioned to 5th common)
- LCD 1/2, 1/3 bias, 1/2, 1/3, 1/4, 1/5 (mask option) duty
- One 8-bit timer
- 6 interrupt sources (Timer, T16Hz, T2Hz, 128Hz, 2KHz, external interrupt)
- Power down mode (Wake-up source: key input, T2Hz, T16Hz, timer)

Note1: T16Hz: 32Hz, 16Hz, 8Hz or 4Hz
Note2: T2Hz: 2Hz or 1Hz

3. BLOCK DIAGRAM



Note1: By mask option, SEG31 - 28 can be defined as either segment output or I/O. (SEG31 - 28 or ABB7 - 4)
Note2: By mask option, ABB1 can be defined as either I/O or common output (ABB1 or common4)

4. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
SEG26 - 0 SEG31 - 27	30 - 4 36 - 32	O	LCD driver segment output. SEG31 - 28 can be mask option for ABB7 - 4.
C3 - 0	54 - 57	O	LCD driver common output
ABB1 - 0	37 - 38	I/O	I/O port (ABB1 can be mask option for C4)
EFB5 - 0	44 - 49	I	Input port (also for key wake up input)
CDB3 - 0	42 - 39	I/O	I/O port is applicable for sensor
RESET	50	I	System reset input
X32I	51	I	32.768KHz crystal input (provide LCD frequency)
X32O	52	O	32.768KHz crystal output
TEST	53	I	Test input
VDD	43	I	Power input
VSS	31	I	Ground input
V3 V45	58 1	I	Inputs for setting LCD bias
CUP1 CUP2	2 3	I	Inputs for setting LCD bias

5. FUNCTIONAL DESCRIPTIONS

5.1. ROM Area

The SPL081A provides 7.5K-byte ROM with a LCD driver that is capable of controlling 4(or 5) commons and 32 segments. (Basically, 7K bytes of ROM is available for application program and data, 0.5K bytes is allocated for test program.)

5.2. Stop Clock Mode

The SPL081A provides a power saving mode for those applications required very low stand-by current. Users can simply enable the wake-up sources to stop the CPU clock by writing the STOP CLOCK Register ($09). By doing that, CPU will go to standby mode and the RAM and I/Os remain in their previous states until being woken up. There are three wake-up sources in the SPL081A, Port EFB wake-up, TIMER wake-up and T2Hz or T16Hz wake-up. After the SPL081A is woken up, CPU will go to the next state of Sleep. Wake-up action will not affect both RAM and I/Os.

Note1: T16Hz: 32Hz, 16Hz, 8Hz or 4Hz
Note2: T2Hz: 2Hz or 1Hz

5.3. Timer/Counter

The SPL081A contains an 8-bit timer. In the timer mode, TMA is a re-loadable up-counter. It will automatically be reloaded with the user's preset value and up-count again.

The clock source is selected as the following:

Timer/Counter		Addr.	Clock Source
TMA	8-BIT TIMER	$0025	CPU CLOCK (T) or CLK32K (32768Hz or CPU clock / 8)

5.4. LCD Controller

SPL081A contains a LCD controller/driver that provides the capability of driving 5 commons and 32 segments LCD. To light the overhead of CPU, a display buffer is designed for mapping to LCD. A LCD dot/pattern is set ON or OFF by programming the corresponding bit of the display buffer. To make the chip more flexible, the pin SEG31, 30, 29, 28, can be selected as I/O pins by mask option. In addition, the LCD bias can be programmed as 1/2 or 1/3. The duty can be selected as 1/2, 1/3, 1/4 or 1/5.

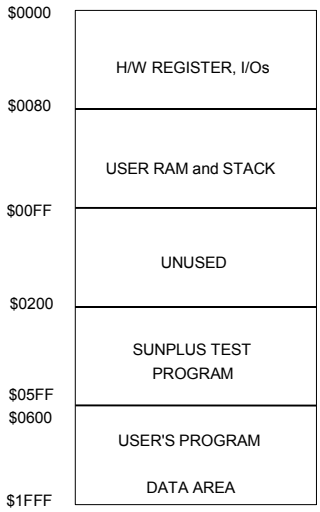
5.5. Map of Memory and I/Os

* I/O PORT:
  - PORT ABB $0002
    EFB $0003
    CDB $0005
  - I/O CONFIG $0000
    $0001
    $0006

* NMI SOURCE:
  - INT1 (from TIMER)

*INT SOURCE
  - INT0 (from TIMER)
  - 128 Hz
  - 2 KHz
  - TYHz (32Hz, 16Hz, 8Hz, 4Hz)
  - TXHz (2 Hz or 1Hz)
  - EXTERNAL (CDB1)

*MEMORY MAP



6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

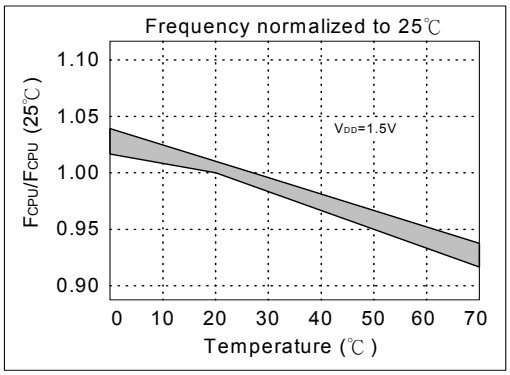
Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 1.7V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

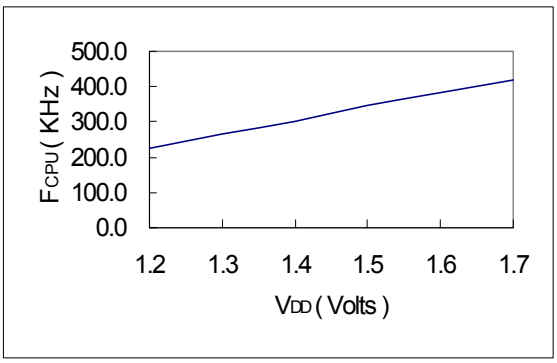
6.2. DC Characteristics

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	1.2	-	1.7	V	
Operating Current with 2Hz wake up	I_{OP}	-	3.0	-	μA	F_{CPU} = 0.3MHz @ 1.5V, no load use 32768Hz crystal
Operating Current with 2Hz wake up	I_{OP}	-	16	-	μA	F_{CPU} = 0.3MHz @ 1.5V, no load no use 32768Hz crystal
Operating Current without 2Hz wakeup	I_{OP}	-	35	-	μA	F_{CPU} = 0.3MHz @ 1.5V, no load
Standby Current	I_{STBY}	-	-	1.0	μA	VDD = 1.5V, 32768 Hz OFF
OSC Frequency	F_{OSC2}	-	0.3	-	MHz	VDD = 1.5V
		-	0.6	-		
		-	1.1	-		
Input High Level	V_{IH}	1.1	-	-	V	VDD = 1.5V
Input Low Level	V_{IL}	-	-	0.5	V	VDD = 1.5V
Output High Current (I/O)	I_{OH}	-	-1.0	-	mA	VDD = 1.5V V_{OH} = 1.0V
Output Sink Current (I/O)	I_{OL}	-	0.25	-	mA	VDD = 1.5V V_{OL} = 0.5V
CPU Clock	F_{CPU}	-	0.15	-	MHz	0.15, 0.3, 0.55MHz by code option $F_{CPU} = F_{OSC}/2$ @ 1.5V
		-	0.3	-		
		-	0.55	-		

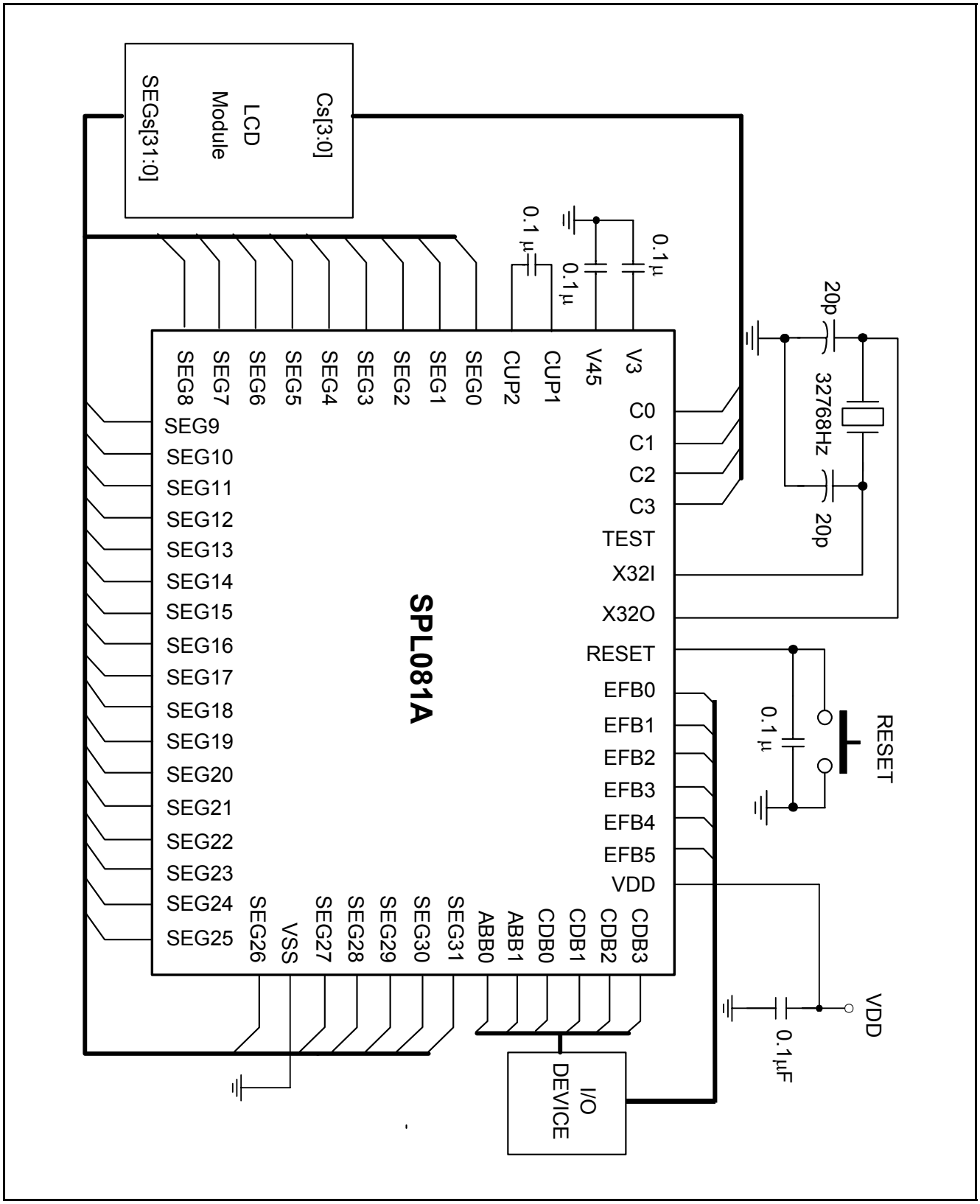
6.2.1. Frequency vs. temperature



6.2.2. Frequency vs. VDD



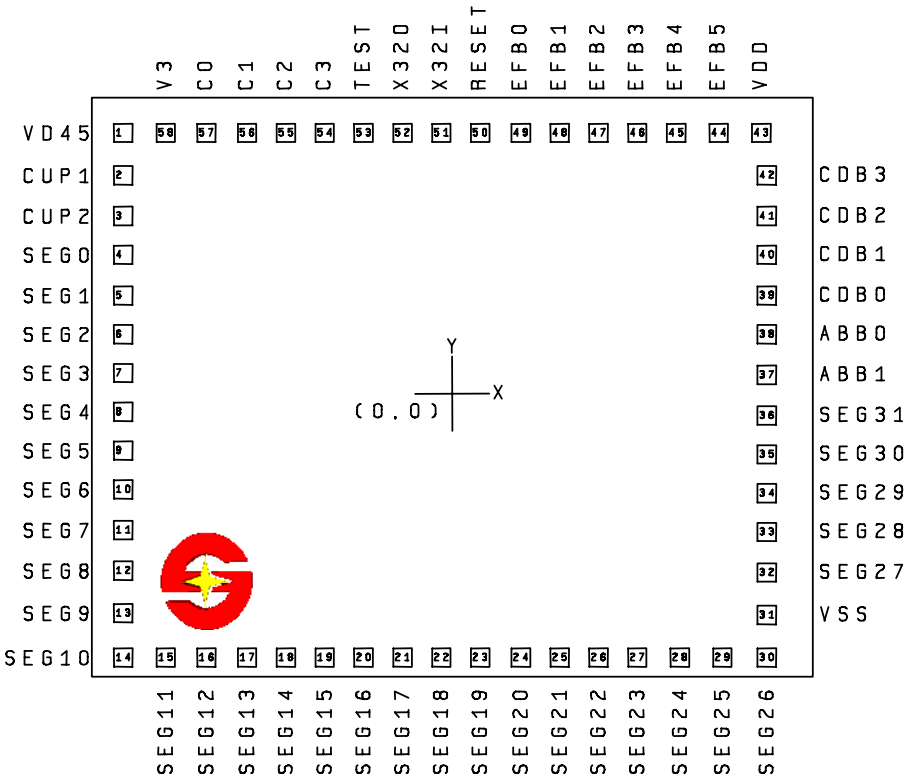
7. APPLICATION CIRCUIT



Note: The 0.1µF capacitor between VDD and VSS should be placed to IC as close as possible.

8. PACKAGE/PAD LOCATIONS

8.1. PAD Assignment



Chip Size: 2440μm x 2020μm

This IC substrate should be connected to VSS

Note1: Chip size included scribe line.

Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

8.2. Ordering Information

Product Number	Package Type
SPL081A-nnnnV-C	Chip form

Note1: Code number (nnnnV) is assigned for customer.

Note2: Code number (nnnn = 0000 - 9999); version (V = A - Z).

8.3. PAD Locations

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
1	V45	-1068	847	30	SEG26	1019	-858
2	CUP1	-1068	711	31	VSS	1019	-721
3	CUP2	-1068	574	32	SEG27	1019	-584
4	SEG0	-1068	447	33	SEG28	1019	-450
5	SEG1	-1068	320	34	SEG29	1019	-322
6	SEG2	-1068	193	35	SEG30	1019	-196
7	SEG3	-1068	66	36	SEG31	1019	-69
8	SEG4	-1068	-60	37	ABB1	1019	58
9	SEG5	-1068	-187	38	ABB0	1019	193
10	SEG6	-1068	-314	39	CDB0	1019	320
11	SEG7	-1068	-441	40	CDB1	1019	447
12	SEG8	-1068	-577	41	CDB2	1019	574
13	SEG9	-1068	-714	42	CDB3	1019	711
14	SEG10	-1068	-858	43	VDD	1001	847
15	SEG11	-931	-858	44	EFB5	864	847
16	SEG12	-795	-858	45	EFB4	727	847
17	SEG13	-668	-858	46	EFB3	601	847
18	SEG14	-541	-858	47	EFB2	474	847
19	SEG15	-414	-858	48	EFB1	347	847
20	SEG16	-287	-858	49	EFB0	220	847
21	SEG17	-160	-858	50	RESET	93	847
22	SEG18	-33	-858	51	X32I	-33	847
23	SEG19	93	-858	52	X32O	-160	847
24	SEG20	220	-858	53	TEST	-287	847
25	SEG21	347	-858	54	C3	-414	847
26	SEG22	474	-858	55	C2	-541	847
27	SEG23	601	-858	56	C1	-668	847
28	SEG24	737	-858	57	C0	-795	847
29	SEG25	874	-858	58	V3	-931	847

9. DISCLAIMER

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10. REVISION HISTORY

Date	Revision #	Description	Page
JUL. 28, 1998	0.1	Original	
AUG. 18, 1998	0.2	Modify CPU frequency: 0.3MHz @ 1.5V -> 300KHz or 550KHz (mask option) in the "*FEATURES*"	
OCT. 27, 1998	0.3	1. Modify CPU frequency: 550KHz -> 500KHz 2. Add "*PAD ASSIGNMENT AND LOCATIONS*"	
JAN. 12, 1999	0.4	Correct chip size: 2440μm X 2020μm	
OCT. 20, 1999	0.5	Add "Iop Condition" description in the "*DC CHARACTERISTICS*"	
MAY. 15, 2001	1.0	1. Delete "*PRELIMINARY*" 2. Add "Note: The 0.1μF capacitor between VDD and VSS…" 3. Add "*10. REVISION HISTORY*" 4. Renew to a new document format	6, 7 10
AUG. 27, 2001	1.1	1. Add Note1 in the "*8.1 PAD Assignment*" 2. Renew to a new document format	8