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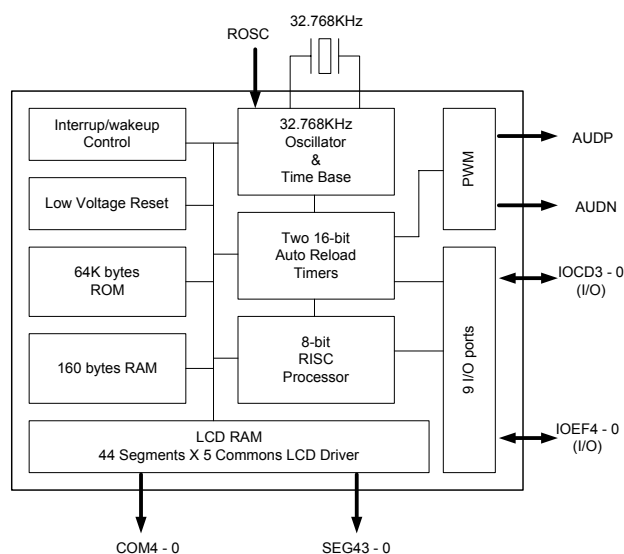
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64KB LCD CONTROLLER/DRIVER

1. GENERAL DESCRIPTION

The SPL31A, an 8-bit CMOS single chip microprocessor, contains RAM, ROM, I/Os, interrupt/wakeup controller, timer, 8-bit PWM audio output and automatic display controller/ driver for LCD. With a dual channel PWM driver, attractive sound effects can be generated easily. Built-in voltage doubler and voltage regulator provide robust and adjustable (16-level) LCD supply voltage to get the best display quality for specific panels. Furthermore, a software controllable standby mode is also implemented for power saving. The SPL31A is designed with state-of-the-art technology to fulfill the requirements of LCD applications especially for hand-held products.

2. BLOCK DIAGRAM



3. FEATURES

- Built-in 8-bit CPU
 - 160 bytes SRAM
 - 64K bytes ROM
 - Max. CPU clock: 3.0MHz @ 2.4V - 5.5V
 - Programmable CPU clock frequency, 1/2, 1/4, 1/8, 1/16, 1/32 or 1/64 of R-oscillator's clock frequency is available
 - Provides 7 interrupt sources
- Built-in 8-bit 2-channel PWM outputs
- Built-in 32.768KHz Crystal / R-oscillator
 - Crystal or R-oscillator (mask option)
 - Crystal oscillator switches from strong to Weak mode automatically
 - Internal time base generator
- Built-in System R-oscillator
 - Only one resistor is needed
- Two 16 bits timer/counters
- Low Voltage Reset / Low Voltage Detect
 - Provides 2.3V low voltage reset function
 - 2.4V/2.6V low voltage detect (Mask option)
- Low power consumption
 - Operating current: 1.0mA/1.0MHz @ 3.0V
 - Very low standby current : $I_{STBY} < 1.0\mu A$ @ 3.0V
 - In standby mode: stop all oscillators
- Max. 12 general purpose I/O
 - SEG[43:41] can be optioned to IOEF[7:5]
 - 8 IO pins support Key wake-up mode
- LCD controller / driver
 - 44 segments x 5 commons, max. 220 dots
 - Programmable bias option (1/2, 1/3 bias) and duty option (1/2, 1/3, 1/4, 1/5 duty)
 - Built-in voltage doubler and regulator to generate V_{LCD} voltage for LCD driver
 - Adjustable 16-level V_{LCD} for various panels
 - 1/3 bias: V_{LCD} (3.0V - 6.0V)
 - 1/2 bias: V_{LCD} (2.0V - 4.0V)

4. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
SEG43 - 0	5 - 48	O	LCD driver segment output
COM4 - 0	49 - 53	O	LCD driver common output
IOEF1 - 0	74 - 73	I/O	I/O port (provide key wake-up function)
IOEF4 - 2	3 - 1		
IOCD3 - 0	68 - 65	I/O	I/O port
ROSC	63	I	System R-oscillator input, connect to VDD through resistor
RESET	62	I	System reset input
AVDD	71	P	PWM power supply input
AUDP	70	O	PWM audio output
AUDN	72	O	PWM audio output
AVSS	69	P	PWM ground input
X32I	61	I	32.768KHz crystal input, or connect to VDD through resistor as R-oscillator input (Mask option)
X32O	60	O	32.768KHz crystal output
TEST	59	I	Test mode input
VDD	4	P	Power supply voltage input
VSS	64	P	Ground input
VLCD	54	I	LCD voltage, connect to VSS through a capacitor
VDD1	55	I	Connect coupling capacitors for charge pump
VDD2	58		
CUP1	56	I	Charge pump capacitor interconnection pins for LCD voltage generation
CUP2	57		

Note1: Legend: I = Input, O = Output, P = Power

Note2: SEG43 - 41 can be optioned to IOEF7 - 5, IOEF7 - 0 provide key wake-up function

Note3: Provides 220 bits read/writable LCD RAM buffer

Note4: 32.768KHz Crystal oscillator can be optioned to R-oscillator (connect to VDD through resistor).

5. FUNCTIONAL DESCRIPTIONS

5.1. Map of Memory and I/Os

* I/O PORT:

- IOCD Port \$0004
- IOEF Port \$0005

* I/O CONFIG

- IOCD_Config \$0000
- IOEF_Config \$0019

* NMI SOURCE:

- INT1 (from TIMER 1)

* INT SOURCE

- INT0 (from TIMER 0)
- INT1 (from TIMER 1)
- T16Hz (4Hz /8Hz /16Hz /32Hz)
- T2Hz (2Hz /1Hz)
- 128Hz
- 2KHz
- EXTINT (from IOCD0 pin)

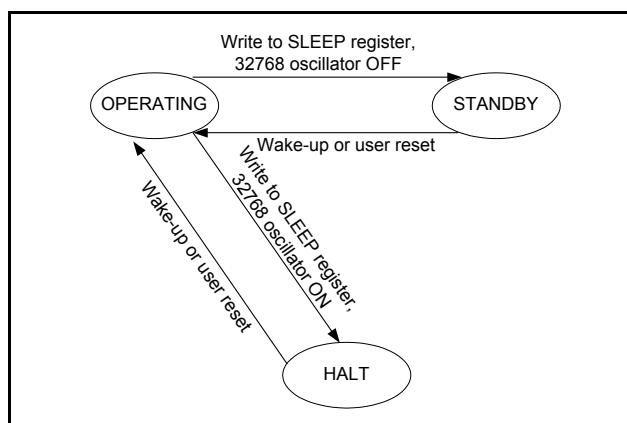
* WAKEUP SOURCE

- IOEF Port Change
- TIMER 0 Overflow
- T16Hz (4Hz /8Hz /16Hz /32Hz)
- T2 Hz (2Hz /1Hz)

* MEMORY MAP

\$0000	I/O & Registers
\$001F	
\$0020	LCD RAM Buffer
\$003D	reserved
\$0060	
	SRAM
\$00FF	reserved
\$0200	
	Test Program
\$05FF	
\$0600	Program ROM Bank #0
\$7FFA	NMI/Reset/IRQ Vector
\$7FFF	
	Program ROM Bank #1
\$FFFA	NMI/Reset/IRQ Vector
\$FFFF	

state is entered by writing the SLEEP register (\$09). There are four wake-up sources in SPL31A: port IOEF wake-up, TIMR0 wake-up, 4Hz/8Hz/ 16Hz/32Hz wake-up and 2Hz/1Hz wake-up. If any wake-up event occurs, execution of the next instruction continues in the operating state. In standby mode, all modules will be shut down, and RAM and I/Os remain in their previous states. Therefore current consumption is minimized. By writing to SLEEP register but keeps 32768 oscillator running, the system is in HALT state. CPU clock is halted while it waits for an event (key press, timer overflow) to generate a wake-up in HALT state. The 32768 related modules (timer/counter, LCD driver...) may remain active in the halt state. Following figure is a state diagram for the SPL31A.



State Diagram of SPL31A

5.2. ROM Area

SPL31A is a ROM based micro-controller with 220 dots LCD driver. The large ROM space can be defined as a program ROM, LCD font and audio data continuously without any limitation. To access the higher bank ROM area, user can program the BANK SELECT register (\$07) to 1, then fetch the data from address \$8000 to \$FFFF.

5.3. Operating States

The SPL31A provides three operating states: standby, halt, and operating state. Following table shows the differences between the three operating states.

	Operating	Halt	Standby
CPU	ON	OFF	OFF
32768 oscillator	ON	ON	OFF
LCD driver	ON	ON/OFF	OFF

In operating state, all modules (CPU, 32768 oscillator, timer/counter, LCD driver...) are activated. The halt/standby

After the chip is awakened from halt/standby state, CPU will continue to execute the next instruction. The RAM and I/O status will not be changed by wake-up.

5.4. Time-Base-Setting Register

Writing to TIME-SETTING register can program the time source of CPU wake-up and interrupt. For example, the programmer can change 2Hz wake-up and interrupt into 1Hz wake-up and interrupt by writing 80H into \$0A.

Thus, the system will wake up to service every second. Also, T16Hz (one of counter's clock source and wake-up & interrupt) can be one of 4Hz, 8Hz, 16Hz or 32Hz by setting bit0 and bit1 of TIME-SETTING register (\$0A). At power on state, the default value of T16Hz is 4Hz and T2Hz is 2Hz.

5.5. Timer/Counter

SPL31A contains two 16-bit timer/counters, TM0 and TM1 respectively. In the timer mode, TM0 and TM1 are reloadable up-counters. When the timer overflows from \$FFFF to \$0000, the carry signal will generate the INT signal if the corresponding bit is enabled in INT ENABLE register (\$0D). The timer will automatically reload the value assigned by the program and up

count continuously. If TM0 is specified as a counter, the user can reset the counter by loading 0 into register \$10 and \$11 and loading 0 into the counter by writing any data to \$12. After the counter is activated, the counter's value can also be read from above registers (\$10 and \$11) and the read instruction will not affect the counter's value or reset it.

The clock source of the timer/counter are selected as the following:

The clock source of the timer/counter are selected as the following.

Timer/Counter		Address	Clock Source
TM0	16-BIT Timer	\$0010	R-oscillator Output, the CARRY of timer 1
		\$0011	
		\$0012	
	16-BIT Counter	\$0010	Clock source A: IOCD0, R-oscillator Output, VDD, 32768Hz.
		\$0011	Clock source B: IOCD1, VDD, T16Hz, 128Hz.
		\$0012	Note: T16Hz can be one of 4Hz, 8Hz, 16Hz and 32Hz by setting \$0A (time-setting register)
TM1	16-BIT Timer	\$0013	R-oscillator Output, 32768 Hz
		\$0014	
		\$0015	
Mode Select Register		\$000B	Select TM0 & TM1 configuration

5.6. Speech and Melody

Since SPL31A can provide a large ROM size and wide CPU operation speed, it is suitable for speech and melody synthesis. For speech synthesis, this chip can provide INT for precise sampling frequency. Users can record or synthesize the sound and digitize the data into the ROM. The sound can be played back in the sequence designed by the internal user's program. Several algorithms are recommended for high fidelity and good compression of sound: such as PCM and ADPCM. For melody synthesis, SPL31A provides dual tone mode. Once in the dual tone mode, users only need to program the tone frequency of each channel by writing to timer/counter TM0 and TM1, and set the envelope of each channel. The hardware will toggle the tone wave automatically without users' care.

5.7. LCD Controller/Driver

SPL31A contains a LCD controller and driver for 220dots LCD display. Users can set the LCD configuration (bias, duty, display mode) by writing LCD control register (\$18). Once the LCD configuration is initialized, the desired pattern can be displayed by filling the LCD buffer with appropriate data. The LCD driver can still operate during halt mode by keeping 32768 oscillator running. Furthermore, programmer can turn off the LCD display through LCD control register for power saving. The LCD driver in SPL31A is designed to fit most LCD's specifications. 1/2 or 1/3 bias are available from the LCD driver. Meanwhile, The display duty can be programmed as 1/2, 1/3, 1/4 or 1/5 duty.

5.8. Voltage Doubler/Regulator

To get the best LCD quality, the LCD supply voltage should not change with the system power. The SPL31A provides a robust and adjustable (16-level) LCD supply voltage. Users can get desired VLCD to fit specific LCD panels by changing the output reference voltage (program \$16). The available VLCD voltage range are summarized as the following table:

Bias	Min. V_{LCD} (\$16 = 00h)	Max. V_{LCD} (\$16 = 0Fh)
1/2 bias	2.0V	4.0V
1/3 bias	3.0V	6.0V

Note1: If the LCD display is uneven with a large panel load, connect a resistor between the VDD1 pin and ground is suggested.

Note2: To make sure the chip work properly, the following equation must be satisfied.

$$\text{Min. } (V_{LCD}) > VDD, \text{ Otherwise, } VDD \text{ will change the } V_{LCD}.$$

5.9. PWM Output

Internally, SPL31A has one pair of PWM outputs supporting two sound channels. Each channel can be set to play speech or tone individually. SPL31A uses Pulse Width Modulation that is able to drive speaker or buzzer directly without any buffer or amplification circuit.

5.10. Low Voltage Reset

The SPL31A provides a low voltage reset function. The system will enter into LVRST state if and only if the power supply voltage VDD is lower than 2.3V.

5.11. Watchdog Timer (WDT)

An on chip watchdog timer is available on SPL31A. The WDT is designed for recovering from system abnormal operation. If the system is hanged, WDT will generate a system reset to restart system after 1 second. If WDT is enabled, the WDT should be cleared every two seconds to avoid accidental reset. The WDT can be cleared by writing the specified value 0FH to port \$0F. Note that the WDT only works when 32768 Hz clock is available.

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5.12. Low Voltage Detect

Furthermore, a Low Voltage Detect function is built in SPL31A. Once, the control register \$17 bit7 is set to 1 (enable), the programmer can compare VDD voltage level with reference voltage 2.4V/2.6V from reading \$17 bit0.

Note1: 50us delay time is recommended for voltage detect circuit stabilization.

Note2: Be sure to turn off voltage detect circuit if not needed to minimize power consumption.

5.13. Mask Options

5.13.1. 32768 crystal oscillator

- 1). X'TAL
- 2). R-oscillator

5.13.2. Low voltage detect

- 1). 2.4V
- 2). 2.6V

5.13.3. SEG[43:41] can be optioned to IOEF[7:5]

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to $V_+ + 0.5V$
Operating Temperature	T_A	0°C to +60°C
Storage Temperature	T_{STO}	-50°C to +150°C

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. DC Characteristics (VDD = 3.0V, T_A = 25°C)

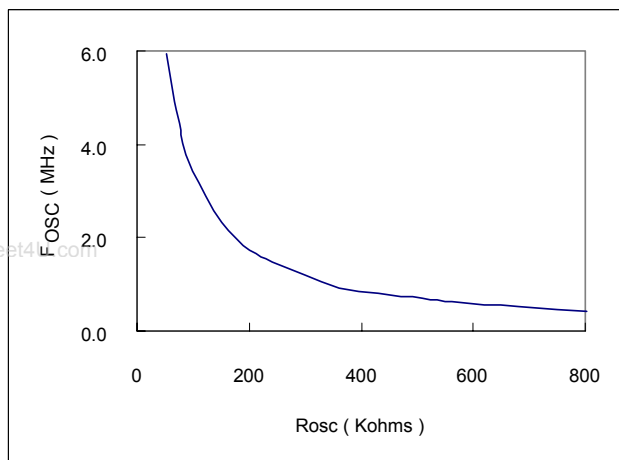
Characteristics	Symbol	Limit			Unit	Test condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery application
Operating Current	I_{OP}	-	0.8	-	mA	VDD = 3.0V, F_{CPU} = 600KHz
Standby Current	I_{STBY}	-	-	1.0	μA	VDD = 3.0V
Audio output current	I_{OH}	-	-50	-	mA	VDD = 3.0V, V_{OH} = 2.5V
		-	-90	-		VDD = 3.0V, V_{OH} = 2.0V
	I_{OL}	-	60	-	mA	VDD = 3.0V, V_{OL} = 0.5V
		-	110	-		VDD = 3.0V, V_{OL} = 1.0V
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High I	I_{OH}	-	-2.0	-	mA	VDD = 3.0V, V_{OH} = 2.4V
Output Sink I	I_{OL}	-	2.5	-	mA	VDD = 3.0V, V_{OL} = 0.8V

6.3. DC Characteristics (VDD = 4.5V, T_A = 25°C)

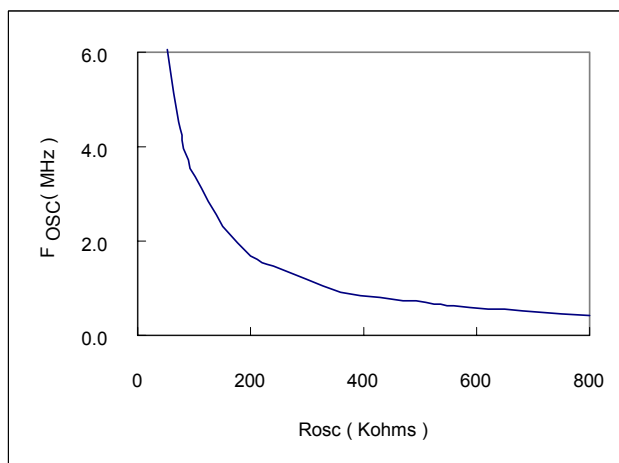
Characteristics	Symbol	Limit			Unit	Test condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.6	-	5.5	V	For 3-battery application
Operating Current	I_{OP}	-	1.6	-	mA	VDD = 4.5V, F_{CPU} = 600KHz
Standby Current	I_{STBY}	-	-	1.0	μA	VDD = 4.5V
Audio output current	I_{OH}	-	-100	-	mA	VDD = 4.5V, V_{OH} = 3.5V
	I_{OL}	-	70	-	mA	VDD = 4.5V, V_{OL} = 0.8V
Input High Level	V_{IH}	3.0	-	-	V	VDD = 4.5V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 4.5V
Output High I	I_{OH}	-	-2.0	-	mA	VDD = 4.5V, V_{OH} = 3.5V
Output Sink I	I_{OL}	-	2.5	-	mA	VDD = 4.5V, V_{OL} = 0.8V

6.4. The Relationships between the R_{OSC} and the F_{CPU}

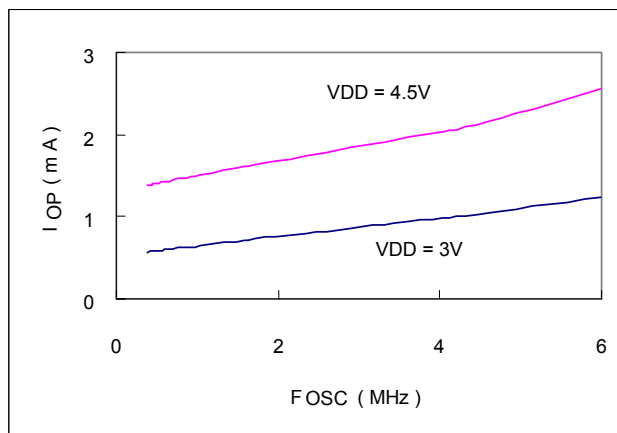
6.4.1. $V_{DD} = 3.0V$, $T_A = 25^\circ C$



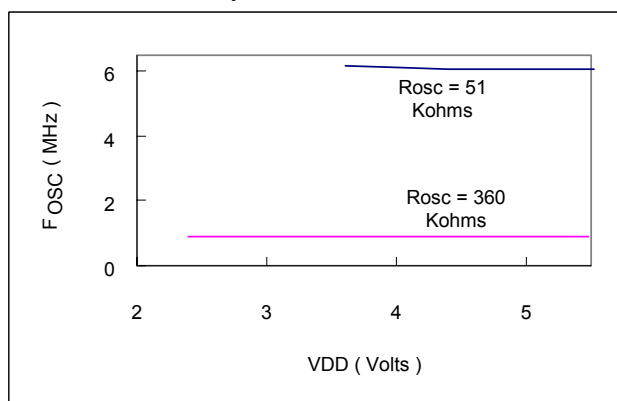
6.4.2. $V_{DD} = 4.5V$, $T_A = 25^\circ C$



6.5. The Relationships between the F_{CPU} and the I_{OP}

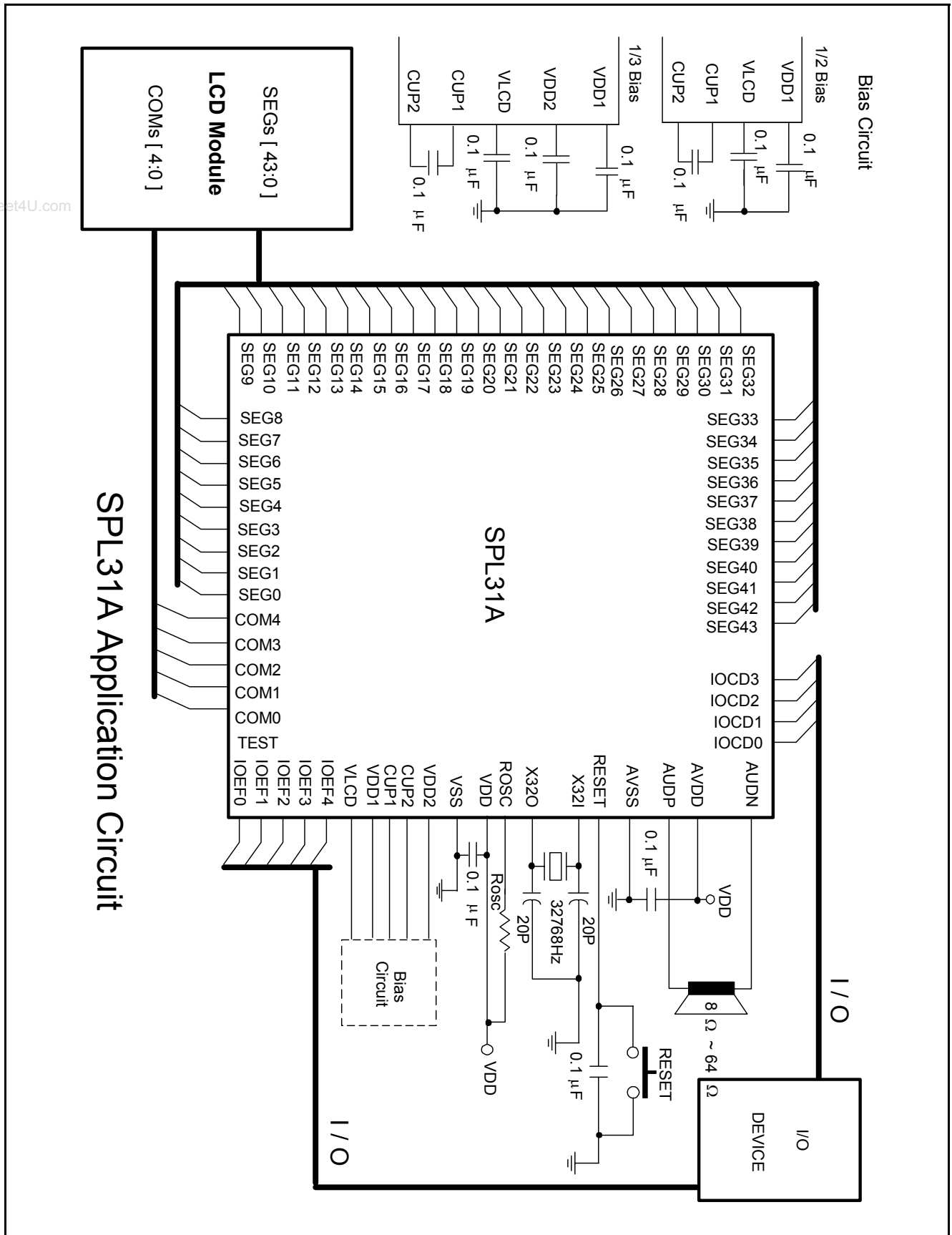


6.6. The Relationships between the F_{CPU} and the V_{DD}



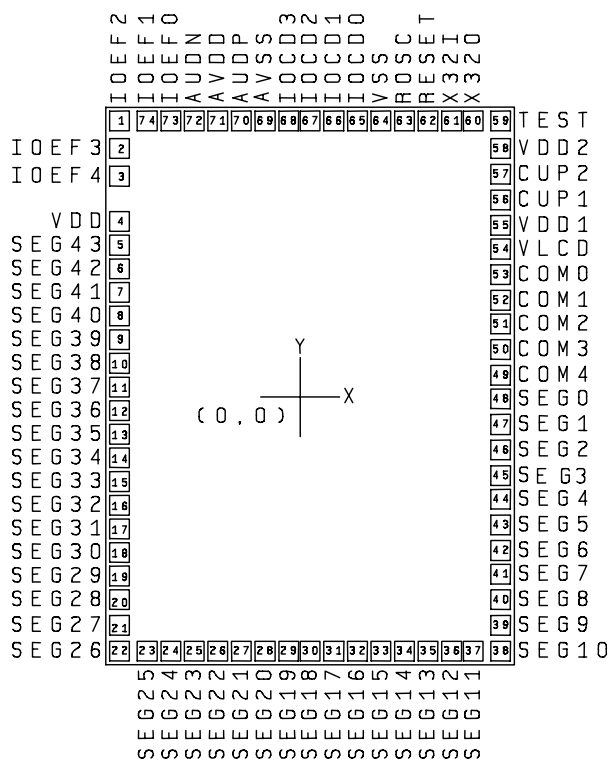


7. APPLICATION CIRCUITS



8. PACKAGE/PAD LOCATIONS

8.1. PAD Assignment



Chip Size: 2270μm × 3020μm

This IC substrate should be connected to VSS

Note1: Chip size included scribe line.

Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

8.2. Ordering Information

Product Number	Package Type
SPL31A-nnnnV-C	Chip form

Note1: Code number (nnnnV) is assigned for customer.

Note2: Code number (nnnn = 0000 - 9999); version (V = A - Z).

8.3. PAD Locations

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
1	IOEF2	-921	1395	38	SEG10	1021	-1295
2	IOEF3	-921	1258	39	SEG9	1021	-1168
3	IOEF4	-921	1116	40	SEG8	1021	-1035
4	VDD	-921	885	41	SEG7	1021	-908
5	SEG43	-921	765	42	SEG6	1021	-781
6	SEG42	-921	645	43	SEG5	1021	-654
7	SEG41	-921	525	44	SEG4	1021	-527
8	SEG40	-921	405	45	SEG3	1021	-400
9	SEG39	-921	285	46	SEG2	1021	-273
10	SEG38	-921	165	47	SEG1	1021	-146
11	SEG37	-921	45	48	SEG0	1021	-19
12	SEG36	-921	-75	49	COM4	1021	108
13	SEG35	-921	-195	50	COM3	1021	235
14	SEG34	-921	-315	51	COM2	1021	362
15	SEG33	-921	-435	52	COM1	1021	489
16	SEG32	-921	-555	53	COM0	1021	616
17	SEG31	-921	-675	54	VLCD	1021	743
18	SEG30	-921	-795	55	VDD1	1021	870
19	SEG29	-921	-915	56	CPU1	1021	997
20	SEG28	-921	-1035	57	CPU2	1021	1124
21	SEG27	-921	-1168	58	VDD2	1021	1258
22	SEG26	-921	-1295	59	TEST	1021	1395
23	SEG25	-784	-1295	60	X32O	884	1395
24	SEG24	-656	-1295	61	X32I	766	1395
25	SEG23	-538	-1295	62	RESET	647	1395
26	SEG22	-419	-1295	63	ROSC	529	1395
27	SEG21	-301	-1295	64	VSS	410	1395
28	SEG20	-182	-1295	65	IOCD0	292	1395
29	SEG19	-64	-1295	66	IOCD1	173	1395
30	SEG18	55	-1295	67	IOCD2	55	1395
31	SEG17	173	-1295	68	IOCD3	-64	1395
32	SEG16	292	-1295	69	AVSS	-182	1395
33	SEG15	410	-1295	70	AUDP	-301	1395
34	SEG14	529	-1295	71	AVDD	-419	1395
35	SEG13	647	-1295	72	AUDN	-538	1395
36	SEG12	766	-1295	73	IOEF0	-656	1395
37	SEG11	884	-1295	74	IOEF1	-784	1395

9. DISCLAIMER

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10. REVISION HISTORY

Date	Revision #	Description	Page
NOV. 17, 1999	0.1	Original	
SEP. 22, 2000	0.2	OSC Resistor Typ. 220K -> 177K	8
OCT. 19, 2000	1.0	Delete " <u>PRELIMINARY</u> "	
APR. 30, 2001	1.1	1. Correct Min. (V _{LCD}) - VDD > -0.5 to Min. (V _{LCD}) > VDD 2. Renew to a new document format	5
AUG. 10, 2001	1.2	1. Update " <u>6. ELECTRICAL SPECIFICATIONS</u> " 2. Correct chip size 3. Add Note1 in the " <u>8.1 PAD Assignment</u> " 4. Renew to a new document	8 - 9 11 11

