SPLC-20-9D-2-B Optical SMPTE 292M/297M/259M Video SFP (V_SFP) transceiver w/ Digital Diagnostics

ORDERING INFORMATION

SPLC-20- 9D - 2 - B

RELEASE ACTUATOR
B = Bail Actuator

TRASMITTER/RECEIVER TYPE
2 = 1310nm FPB / PIN Receiver

COMMUNICATIONS PROTOCOL
9D = SMPTE 292M/297M/259M with Digital Diagnostics; 143MBaud to 1.485GBaud

STRATOS

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Features

- SMPTE 292M/297M/259M compatible
- Based on industry standard SFP
- Keyed to support dual TX and RX options
- Handles Pathological test pattern
- Digital Diagnostic Monitoring Interface
- 100Ω differential AC coupled CML Outputs
- Die Cast Metal Housing
- Hot pluggable

PRODUCT OVERVIEW

The SPLC-20-9D-2-B optical Video Small Form Factor Pluggable (V_SFP) transceivers are high performance integrated duplex data links for bi-directional communication over single mode optical fiber. These transceivers are designed to transmit/receive data rates from 143Mbps to 1.485Gbps and are compatible with the following standards:

- SMPTE 292M (HDTV -- 1.485Gbps)
- SMPTE 297M/259M (SDTV -- 143/177/270/360Mbps)

The Stratos Lightwave V_SFP transceiver is hot pluggable which allows a suitably designed enclosure to be changed from one type of external interface to another simply by plugging in a V_SFP having the alternative external interface. The SPLC-20-9D-2-B operates using a single 3.3V supply.

This optoelectronic transceiver module is a Class 1 Laser product compliant with FDA Radiation Performance Standards, 21 CFR Subchapter J. This component is also Class 1 Laser compliant according to International Safety Standard IEC-825-1.

LONG WAVELENGTH LASER

The SPLC-20-9D-2-B transmitter is provided with 1310nm FP laser with angle polished fiber stub.

LONG WAVELENGTH RECEIVER

The SPLC-20-9D-2-B receiver is provided with long wavelength (1270 - 1620nm) PIN pre-amp with angle polished fiber stub.

MODULE SPECIFICATIONS - ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Storage Temperature	Tstg	-40	+85	°C	
Supply Voltage	$V_{CC}T$, $V_{CC}R$		6.0	V	VCC - ground
Data AC Voltage	Tx+, Tx-		2.6	Vpp	Differential
Data DC Voltage	Tx+, Tx-	-10	10	Vpk	V (Tx+ or Tx-) - ground

MODULE SPECIFICATION - RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Ambient Case Temperature	Tc	0		+70	°C	
Supply Voltage	$V_{DD}T$, $V_{DD}R$	+3.135	+3.3	+3.435	VDC	
Baud Rate	BRate	143		1485	MBaud	143/177/270/360/1485MBaud

PERFORMANCE SPECIFICATIONS - ELECTRICAL **0ºC<Tc<+70ºC; +3.135<Vcc<+3.465V**

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	Icc		135	155	mA	Tc = 25°C, Vcc = +3.3 V
				300	mA	0°C<Tc<+70°C, +3.135 V< Vcc <+3.465V
Surge Current	Isurge			30	mA	Surge above steady state value
TRANSMITTER						
CML/LVPECL Inputs (Differential)		300		1860	mVpp	AC coupled inputs
Input Impedance (Differential)	Zin	95	100	105	ohms	Rin > 100 kohms @ DC
Tx_DISABLE Input Voltage - High	ViH	2		3.45	V	
Tx_DISABLE Input Voltage - Low	ViL	0		0.8	V	
RECEIVER						
CML Outputs (Differential)		400	800	1200	mVpp	AC Coupled Outputs
Total Jitter [Pk - Pk]	TJ			135	ps	Measured with Color Bar Test Signal @1.485Gbps (note 1)
				740	ps	Measured with Color Bar Test Signal @143/177/270/360Mbps
SCL, SDA	VoH	2.5		Vcc+0.3	V	
	VoL	0		0.5	V	

Note 1: Maximum Jitter is specified for single module point-to-point applications only. In cascaded configurations, where the receiver electrical output is directly interfaced with the transmitter electrical input of a separate module, accumulated jitter may result in CRC errors to occur during pathological pattern transmission. For error-free operation in such a situation, use of re-clocker device is recommended at the output of the receiver before interfacing to the inputs of the optical transmitter. This will ensure that the output jitter will not exceed the input jitter tolerance of the succeeding transmitter input.

SPLC-20-9D-2-B OPTICAL SPECIFICATIONS - 1310nm FP/PIN RX **0ºC<Tc<+70ºC; +3.135<Vcc<+3.465V**

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
LINK DISTANCE						
9.0µm Core Diameter SMF (Note 2)		10	18		km	BER<1E-10 @ 360/1485Mbps
		15	30		km	BER<1E-10 @ 143/177/270Mbps
TRANSMITTER						
Optical Center Wavelength	λ	1274	1310	1356	nm	Tcase = +25ºC
Spectral Width	$\delta\lambda$			2.5	nm	RMS
Optical Transmit Power	Popt	-12		-7.5	dBm	Average @ 1310nm
Extinction Ratio	ER	9			dBm	P1/P0
Relative Intensity Noise	RIN			-117	dB/Hz	
Total Jitter [Pk - Pk]	TJ			135	ps	Measured with Color Bar Test Signal @1.485Gbps
				740	ps	Measured with Color Bar Test Signal @143/177/270/360MBaud
Output Rise/Fall Time	t_R, t_F			270	ps	20%-80%; Measured unfiltered @1.485GBaud
				1.5	ns	20%-80%; Measured unfiltered @143/177/270/360MBaud
RECEIVER						
Optical Input Wavelength	λ	1270		1620	nm	
Optical Input Power	Pr	-20		-3	dBm	Note 3
Optical Return Loss	ORL	29			dB	
RX_LOS --- Asserted	Pa	-29			dBm	No Signal Pins Designated for RX_LOS. Assert/Deassert Levels can be Monitored via Digital Diagnostics Interface.
RX_LOS --- Deasserted	Pd			-20	dBm	
RX_LOS --- Hysteresis	Pa - Pd		1.5	5	dB	

Note 2: Assumes minimum transmitter output power of -12dBm with minimum extinction ratio of 9dB over 9/125µm Single Mode Fiber (SMF) at 140/177/270/360/1485Mbps. The minimum link distances are based on worst case receiver sensitivity with color bar test signal. The minimum link distances will be reduced with SDI test matrix.

Note 3: Minimum receiver input power is defined for line BER < 1 x 10^{-10} running PRBS 2^{23} - 1 at 140/177/270/360/1485Mbps

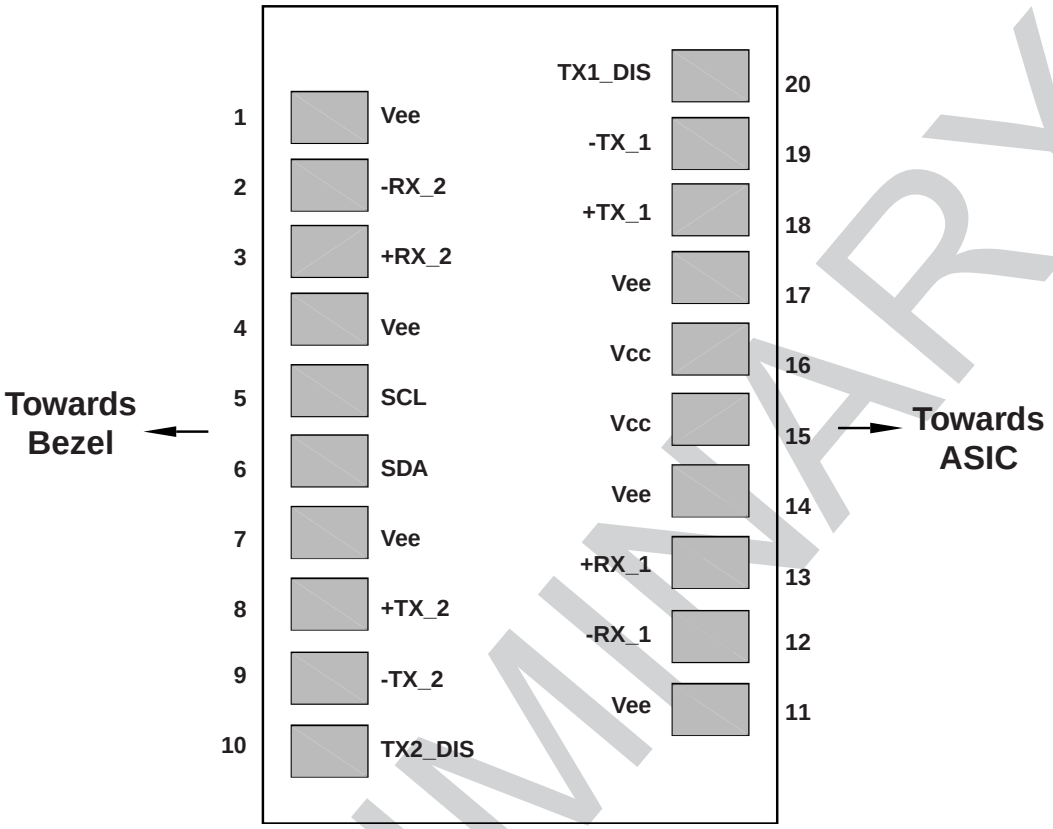


Figure 1. Diagram of Host Board Connector Block Pin Numbers and Names

PIN NO.	NAME	FUNCTION	PLUG SEQ.	NOTES
PIN 1	Vee	Signal Ground	1	
PIN 2	-RX_2	Inverted Received Data out (2)	3	Note 4
PIN 3	+RX_2	Non-Inverted Received Data out (2)	3	Note 4
PIN 4	Vee	Signal Ground	1	
PIN 5	SCL	Serial Clock	3	
PIN 6	SDA	Serial Data	3	
PIN 7	Vee	Signal Ground	1	
PIN 8	+TX_2	Non-inverted Data In (2)	3	Note 5
PIN 9	-TX_2	Inverted Data In (2)	3	Note 5
PIN 10	TX2_DIS	Transmitter Disable (2)	3	Note 6
PIN 11	Vee	Signal Ground	1	
PIN 12	-RX_1	Inverted Received Data out	3	Note 7
PIN 13	+RX_1	Non-Inverted Received Data out	3	Note 7
PIN 14	Vee	Signal Ground	1	
PIN 15	Vcc	Power Supply	2	+3.3V ±5%, Note 8
PIN 16	Vcc	Power Supply	2	+3.3V ±5%, Note 8
PIN 17	Vee	Signal Ground	1	
PIN 18	+TX_1	Non-inverted Data In	3	Note 9
PIN 19	-TX_1	Inverted Data In	3	Note 9
PIN 20	TX1_DIS	Transmitter Disable	3	Note 10: Module Disables on high or open

Plug Sequence: Pin engagement sequence during hot plugging.

NOTES:

(4) ± RX_2: Floating; Not internally connected

(5) ± TX_2: Floating; Not internally connected

(6) TX2_DIS: Floating; Not Internally Connected.

(7) ± RX_1: These are the differential receiver CML level outputs. They are AC coupled 100ohm differential lines which should be terminated with 100ohm (differential) at the user SERDES. The AC coupling is done inside the module and is thus not required on the host board. The voltage swing on these lines will be between 400 and 1200mV differential (200-600mV single ended) when properly terminated. Refer to figure 2 for recommended receive data lines terminations.

(8) Vcc: are the receiver and transmitter power supplies. They are defined as 3.3V±5% at the V_SFP connector pin. Maximum supply current is 300mA. Recommended host board power supply filtering is shown in figure 5. When the recommended supply filtering network is used, hot plugging of the V_SFP module will result in an inrush current of no more than 30mA greater than the steady state value.

(9) ± TX_1: are the differential transmitter inputs. They are AC coupled differential lines with 100ohm differential termination inside the module. The AC coupling is done inside the module and is thus not required on the host board. The inputs will accept differential swing of 300 - 1860 mV differential (150-930mV single ended).

(10) TX1_DIS: is an input that is used to shut down the transmitter optical output when laser fault condition (internally latched) occurs. . It is internally pulled up with a 4.7K - 10K ohm resistor. The states are:

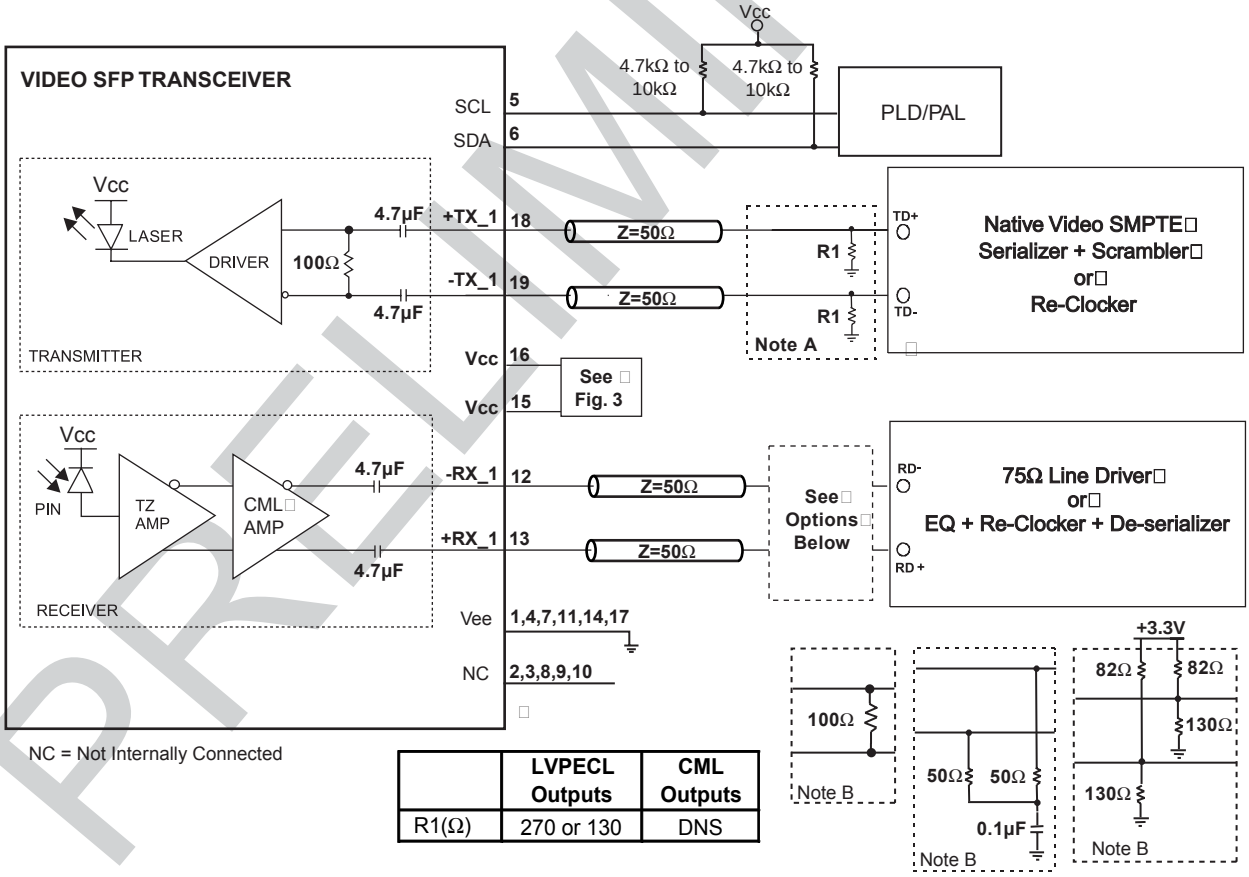
Low (0 - 0.8V):	Transmitter ON
(>0.8, <2.0V):	Undefined
High (2.0 - 3.465V):	Transmitter Disabled
Open:	Transmitter Disabled

TERMINATION CIRCUITS

Inputs to the SPLC-20-9D-2-B transmitter are AC coupled and internally terminated through 50 ohms to AC ground. These modules can operate with CML/LVPECL logic levels. The input signal must have at least a 300mV peak-to-peak differential signal swing. Output from the receiver section of the module is AC coupled CML level and is expected to drive into a 50 ohm load. Different termination strategies may be required depending on the particular chip being interfaced to. **The SPLC-20-9D-2-B product family is designed with AC coupled data inputs and outputs to provide the following advantages:**

- Close positioning of Tx/RX chip-set with respect to transceiver; allows for shorter line lengths and at gigabit speeds reduces EMI.
- Minimum number of external components.
- Internal termination reduces the potential for unterminated stubs which would otherwise increase jitter and reduce transmission margin.

Subsequently, this affords the customer the ability to optimally locate the chip-set being interfaced to as close to the SPLC-20-9D-2-B as possible and save valuable real estate. At gigabit rates this can provide a significant advantage resulting in better transmission performance and accordingly better signal integrity. Figure 2 illustrates the recommended transmit and receive data lines terminations



	LVPECL Outputs	CML Outputs
R1(Ω)	270 or 130	DNS

Figure 2. Recommended TRANSMIT and RECEIVE Data Terminations

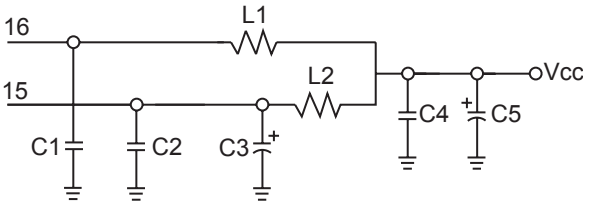
Notes:

A. Consult the Chipset manufacturer's applications information for biasing required for Tx outputs. Some chipset outputs are internally biased and may not need external bias resistors.

B. Consult Chipset manufacturer's data sheet and application data for appropriate receiver input biasing network.

POWER COUPLING

A suggested layout for power and ground connections is given in figure 3 below. Connections are made via separate voltage and ground planes. The ferrite bead should provide an impedance of 220Ω at 100MHz. Bypass capacitors should be placed as close to the 20 pin connector as possible.



VALUES:
C1, C2, C4 = 0.1µF
C3, C5 = 10µF, Tantalum
L1, L2 = Impedance of 220Ω at 100MHz

Figure 3. Suggested Power Coupling

DIGITAL DIAGNOSTIC MONITORING INTERFACE

The SPLC-20-9D-2-B modules are provided with externally calibrated digital diagnostic monitoring interface which allows real-time access to device operating parameters such as transceiver temperature, laser bias current, transmitted optical power, received optical power and transceiver supply voltage over a 2-wire interface. It also defines a system of alarm flags, which provides users with summary information on whether any of the operating parameters are outside of a factory set normal range.

The SPLC-20-9D-2-B Digital Diagnostics Monitoring Interface (DDMI) memory map is shown in figure 4 below. The contents of the memory map are described in details on following pages.

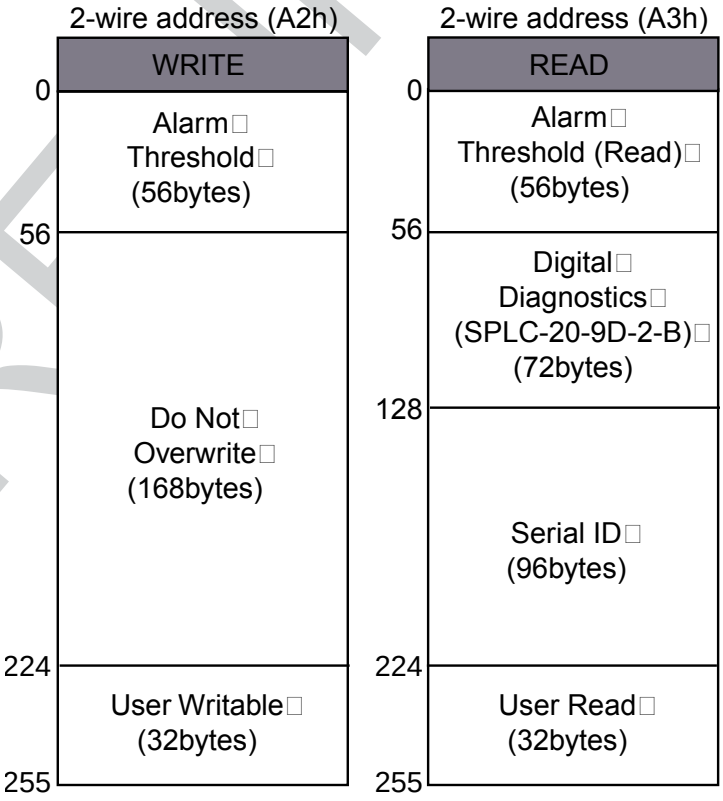


Figure 4. SPLC-20-9D-2-B (V_SFP Transceiver) Memory Map

DIGITAL DIAGNOSTICS:

ALARM THRESHOLDS:

Each A/D quantity has a corresponding high alarm and low alarm threshold. These factory preset values allow the user to determine when a particular value is outside of “normal” limits as determined by the transceiver manufacturer. The alarm thresholds are in "raw" units so they may be directly compared to the DDMI readout. To convert the alarm thresholds to real world units, they must also be scaled.

The V_SFP memory is read/writable as the write protect feature is not enabled. Thus, the host can change the factory set alarm threshold values.

Data Address	# Bytes	Name	Description
00-01	2	Temp High Alarm	MSB at Low Address
02-03	2	Temp Low Alarm	MSB at Low Address
04-05	2	Reserved	Reserved for future monitored quantities
06-07	2	Reserved	Reserved for future monitored quantities
08-09	2	Voltage High Alarm	MSB at Low Address
10-11	2	Voltage Low Alarm	MSB at Low Address
12-13	2	Reserved	Reserved for future monitored quantities
14-15	2	Reserved	Reserved for future monitored quantities
16-17	2	Bias High Alarm	MSB at Low Address
18-19	2	Bias Low Alarm	MSB at Low Address
20-21	2	Reserved	Reserved for future monitored quantities
22-23	2	Reserved	Reserved for future monitored quantities
24-25	2	TX Power High Alarm	MSB at Low Address
26-27	2	TX Power Low Alarm	MSB at Low Address
28-29	2	Reserved	Reserved for future monitored quantities
30-31	2	Reserved	Reserved for future monitored quantities
32-33	2	RX Power High Alarm	MSB at Low Address
34-35	2	RX Power Low Alarm	MSB at Low Address
36-37	2	Reserved	Reserved for future monitored quantities
38-39	2	Reserved	Reserved for future monitored quantities
40-55	16	Reserved	Reserved for future monitored quantities

Table D.1: Alarm Thresholds (2-wire Address A2h)

DIGITAL DIAGNOSTICS (Continued):

CALIBRATION CONSTANTS:

These are the scaling factors which allow the conversion of the raw DDMI output registers to real world units. The correction factors for the RX power are signed single precision floating point numbers corresponding to a 4th order correction formula. All other correction factors are slope/offset coefficients corrections. Please not that all of the slope coefficients are unsigned 16 bit numbers with a LSB value of 1/256th. The offset coefficients are simple signed 16 bit number a LSB = 1.

Data Address	# Bytes	Name	Description
56-59	4	RX_PWR (4)	Single precision floating point calibration data - RX optical power. Bit 7 of byte 56 is MSB. Bit 0 of byte 59 is LSB. RX_PWR(4) should be set to zero for "internally calibrated" devices.
60-63	4	RX_PWR (3)	Single precision floating point calibration data - RX optical power. Bit 7 of byte 60 is MSB. Bit 0 of byte 63 is LSB. RX_PWR(3) should be set to zero for "internally calibrated" devices.
64-67	4	RX_PWR (2)	Single precision floating point calibration data - RX optical power. Bit 7 of byte 64 is MSB. Bit 0 of byte 67 is LSB. RX_PWR(2) should be set to zero for "internally calibrated" devices.
68-71	4	RX_PWR (1)	Single precision floating point calibration data - RX optical power. Bit 7 of byte 68 is MSB. Bit 0 of byte 71 is LSB. RX_PWR(1) should be set to 1 for "internally calibrated" devices.
72-75	4	RX_PWR (0)	Single precision floating point calibration data - RX optical power. Bit 7 of byte 72 is MSB. Bit 0 of byte 75 is LSB. RX_PWR(0) should be set to zero for "internally calibrated" devices.
76-77	2	TX_I (Slope)	Fixed decimal (unsigned) calibration data, laser bias current. Bit 7 of byte 76 is MSB, bit 0 of byte 77 is LSB. TX_I (Slope) should be set to 1 for "internally calibrated" devices.
78-79	2	TX_I (Offset)	Fixed decimal (signed two's complement) calibration data, laser bias current. Bit 7 of byte 78 is MSB, bit 0 of byte 79 is LSB. TX_I (Offset) should be set to zero for "internally calibrated" devices.
80-81	2	TX_PWR (Slope)	Fixed decimal (unsigned) calibration data, transmitter coupled output power. Bit 7 of byte 80 is MSB, bit 0 of byte 81 is LSB. TX_PWR (Slope) should be set to 1 for "Internally calibrated" devices.
82-83	2	TX_PWR (Offset)	Fixed decimal (signed two's complement) calibration data, transmitter coupled output power. Bit 7 of byte 82 is MSB, bit 0 of byte 83 is LSB. TX_PWR (Offset) should be set to zero for "Internally calibrated" devices.
84-85	2	T (Slope)	Fixed decimal (unsigned) calibration data, internal module temperature. Bit 7 of byte 84 is MSB, bit 0 of byte 85 is LSB. T(Slope) should be set to 1 for "Internally calibrated" devices.
86-87	2	T (Offset)	Fixed decimal (signed two's complement) calibration data, internal module temperature. Bit 7 of byte 86 is MSB, bit 0 of byte 87 is LSB. T(Offset) should be set to zero for "Internally calibrated" devices.
88-89	2	V (Slope)	Fixed decimal (unsigned) calibration data, internal module supply voltage. Bit 7 of byte 88 is MSB, bit 0 of byte 89 is LSB. V(Slope) should be set to 1 for "Internally calibrated" devices.
90-91	2	V (Offset)	Fixed decimal (signed two's complement) calibration data, internal module supply voltage. Bit 7 of byte 90 is MSB, bit 0 of byte 91 is LSB. V(Offset) should be set to zero for "Internally calibrated" devices.
92-94	3	Reserved	Reserved
95	1	Checksum	Byte 95 contains the low order 8 bits of the sum of bytes 0 - 94.

Table D.2: Calibration constants for External Calibration (2-wire Address A3h)

DIGITAL DIAGNOSTICS (Continued):

The slope constants at addresses 76, 80,84, and 88, are unsigned fixed-point binary numbers. The slope will therefore always be positive. The binary point is in between the upper and lower bytes, i.e., between the eight and ninth most significant bits. The most significant byte is the integer portion in the range 0 to +255. The least significant byte represents the fractional portion in the range of 0.00391 (1/256) to 0.9961 (255/256). The smallest real number that can be represented by this format is 0.00391 (1/256); the largest real number that can be represented using this format is 255.9961(255 + 255/256). Examples of this format are illustrated below:

Decimal Value	Binary		Hexadecimal	
	MSB	LSB	MSB	LSB
0.0000	00000000	00000000	00	00
0.0039	00000000	00000001	00	01
1.0000	00000001	00000000	01	00
1.0313	00000001	00001000	01	08
1.9961	00000001	11111111	01	FF
2.0000	00000010	00000000	02	00
255.9921	11111111	11111110	FF	FE
255.9961	11111111	11111111	FF	FF

Table D.2a: Unsigned fixed-point binary format for slopes

The calibration offsets are 16-bit signed twos complement binary numbers. The least significant bit represents the same units as described above under “Internal Calibration” for the corresponding analog parameter, e.g., 2mA for bias current, 0.1mW for optical power, etc. The range of possible integer values is from +32767 to -32768. Examples of this format are shown in table below.

Decimal Value	Binary		Hexadecimal	
	MSB	LSB	MSB	LSB
+32767	01111111	11111111	7F	FF
+3	00000000	00000011	00	03
+2	00000000	00000010	00	02
+1	00000000	00000001	00	01
0	00000000	00000000	00	00
-1	11111111	11111111	FF	F
-2	11111111	11111110	FF	FE
-3	11111111	11111101	FF	FD
-32768	10000000	00000000	80	0

Table D.2b: Format for Offsets

External calibration of received optical power makes use of single-precision floating-point numbers as defined by *IEEE Standard for Binary Floating-Point Arithmetic*, IEEE Std 754-1985. Briefly, this format utilizes four bytes (32 bits) to represent real numbers. The first and most significant bit is the sign bit; the next eight bits indicate an exponent in the range of +126 to –127; the remaining 23 bits represent the mantissa. The 32 bits are therefore arranged as in Table below.

FUNCTION	SIGN	EXPONENT	MANTISSA		
BIT	31	30……23	22……0		
BYTE	3		2	1	0
← Most Significant					Least Significant →

Table D.2c: IEEE-754 Single-Precision floating point number format

DIGITAL DIAGNOSTICS (Continue):

Rx_PWR(4), as an example, is stored as shown in Table below:

BYTE ADDRESS	CONTENTS	SIGNIFICANCE
56	SEEEEEEE	Most
57	EMMMMMMM	2nd Most
58	MMMMMMMM	2nd Least
59	MMMMMMMM	Least

Where S = Sign bit; E = Exponent bit; M = Mantissa Bit

Table D.2d: Example of floating point representation

This portion of the memory map contains real-time measurements of V_SFP transceiver temperature, laser bias current, transmitted optical power, received optical power and transceiver supply voltage. The real-time diagnostics registers are shown in table D.3 below.

The V_SFP transceivers are externally calibrated which means that the measurements are raw A/D values and must be converted to real world units using calibration constants stored in EEPROM locations 56 – 95 at 2 wire serial bus address A3h (Table D.2). The conversion process is described on following page. The alarm threshold values should be interpreted in the same manner as real-time 16 bit data (i.e. They must be processed using the calibration constants before they can be evaluated).

Data Address	Bit	Name	Description
96	All	Temperature MSB	Internally measured module temperature
97	All	Temperature LSB	
98	All	Vcc MSB	Internally measured supply voltage in transceiver
99	All	Vcc LSB	
100	All	TX Bias MSB	Internally measured TX Bias current
101	All	TX Bias LSB	
102	All	TX Power MSB	Measured TX output power
103	All	TX Power LSB	
104	All	RX Power MSB	Measured RX input power
105	All	RX Power LSB	
106	All	Reserved	Reserved
107	All	Reserved	Reserved
108	All	Reserved	Reserved
109	All	Reserved	Reserved
Optional Status/Control Bits			
110	7	TX Disable State	Digital state of the TX_DISABLE Input Pin. Updated within 100msec of change of pin.
	6	Soft TX Disable	Read/write bit that allows software disable of laser. Writing '1' disables laser. Turn on/off time is 100 msec max from acknowledgement of serial byte transmission. This bit is "OR"d with the hard TX_DISABLE pin value. Note,TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. Default power up value is 0.
	5-1	Reserved	Reserved
	0	Data_Ready_Bar	Indicates transceiver has achieved power up and data is ready. Bit remains high until data is ready to be ready at which time the device is sets the bit low.
111	7-0	Reserved	Reserved

Table D.3: Real-time diagnostic registers (2-wire Address A3h)

DIGITAL DIAGNOSTICS (Continued):

(1) Internally measured transceiver temperature. Module temperature, T, read out in units of 1/256 ºC, yielding a total range of -128ºC to +128ºC. To calculate the module temperature in ºC:

$$T(ºC) = ((T_{SLOPE} * T_{AD} \text{ (16 bit signed twos complement value)}) + T_{OFFSET}) * 1/256$$

Refer to table D.2 for locations of T_{SLOPE} and T_{OFFSET}. Temperature accuracy is better than ±3 degrees Celsius over specified operating temperature and voltage. Please refer to Tables D.4 and D.5 for more information regarding 16 bit signed twos complement temperature format.

(2) Internally measured supply voltage: Module internal supply voltage, V, is read out in units of 100µV, yielding a total range of 0 - 6.55V. To calculate the module supply voltage in µV:

$$V = ((V_{SLOPE} * V_{AD} \text{ (16 bit unsigned integer)}) + V_{OFFSET}) * 100\mu V$$

Refer to table D.2 for locations of V_{SLOPE} and V_{OFFSET}. Accuracy is better than ±3% of the nominal value over specified operating temperature and voltage.

(3) Measured transmitter laser bias current: Module laser bias current, I, is read out in units of 2µA, yielding a total range of 0 to 131mA. To calculate the transmitter laser bias current in µAL

$$I = ((I_{SLOPE} * I_{AD} \text{ (16 bit unsigned integer)}) + I_{OFFSET}) * 2\mu A$$

Refer to table D.2 for locations of I_{SLOPE} and I_{OFFSET}. Accuracy is better than ±10% of the nominal value over specified operating temperature and voltage.

(4) Measured coupled TX output power: Module transmitter coupled output power, TX_PWR, is read out in units of 0.1µW, yielding a total range of 0 - 6.5mW. To calculate the TX output power in µW:

$$TX\_PWR = ((TX\_PWR_{SLOPE} * TX\_PWR_{AD} \text{ (16 bit unsigned integer)}) + TX\_PWR_{OFFSET}) * 0.1\mu W$$

Refer to table D.2 for locations of TX_PWR_{SLOPE} and TX_PWR_{OFFSET}. Accuracy is better than ±3dB over specified operating temperature and voltage. Data is assumed to be based on measurement of a laser monitor photodiode current. It is factory calibrated to absolute units using the most representative fiber output type. Data is not valid when the transmitter is disabled.

(5) Measured received optical power: Received power, RX_PWR, is read out in units of 0.1µW, yielding a total range of 0 - 6.5mW. To calculate the received optical power in µW:

$Rx\_PWR = [Rx\_PWR(4) * Rx\_PWR_{AD}{}^{4}$(16 bit unsigned integer) + $Rx\_PWR(3)*Rx\_PWR_{AD}{}^{3}$(16 bit unsigned integer) + $Rx\_PWR(2)*Rx\_PWR_{AD}{}^{2}$(16 bit unsigned integer) + Rx_PWR(1) * Rx_PWRAD (16 bit unsigned integer) + Rx_PWR(0)] * 0.1µW

Refer to table D.2 for locations of Rx_PWR(4-0). Absolute accuracy is dependent upon the exact optical wavelength. For the specified wavelength, accuracy is better than ±3dB over specified temperature and voltage. This accuracy is maintained for input power levels up to the lesser of maximum transmitted or maximum received optical power per the appropriate standard. It is maintained down to the minimum transmitted power minus cable plant loss (insertion loss or passive loss) per the appropriate standard.

DIGITAL DIAGNOSTICS (Continued):

Tables D.4 and D.5 below illustrate the 16 bit signed twos complement format used for temperature reporting. The most significant bit (D7) represents the sign, which is zero for positive temperatures and one for negative temperatures.

Most Significant Byte (								Data Address							
D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Sign	64	32	16	8	4	2	1	1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256

Table D.4: Bit weights (°C) for temperature reporting registers

Temperature		Binary		Hexadecimal	
Decimal	Fraction	HIGH byte	LOW byte	HIGH byte	LOW byte
+127.996	+127 255/256	01111111	11111111	7F	FF
+125.000	+125	01111101	00000000	7D	00
+25.000	+25	00011001	00000000	19	00
+1.004	+1 1/256	00000001	00000001	01	01
+1.000	+1	00000001	00000000	01	00
+.996	+255/256	00000000	11111111	00	FF
+0.004	+1/256	00000000	00000001	00	01
0.000	0	00000000	00000000	00	00
-0.004	-1/256	11111111	11111111	FF	FF
-1.000	-1	11111111	00000000	FF	00
-25.000	-25	11100111	00000001	E7	00
-40.000	-40	11011000	00000002	D8	00
-127.996	-127 255/256	10000000	00000001	80	01
-128.000	-128	10000000	00000000	80	00

Table D.5: Digital temperature format test cases.

DIGITAL DIAGNOSTICS (Continued):

ALARM FLAGS:

Data address 112-127 (Table D.6) contain an optional set of alarm bits. These alarm flags are not latched. It is recommended that the detection of an asserted flag bit should be verified by a second read of the flag at least 100msec later. For users who do not wish to set their own threshold values (address 0 to 55 at 2-wire address A2h) or read the values (address 0 - 55 at 2-wire address A3h), the flags alone can be monitored.

Alarm flags associated with transceiver temperature, supply voltage, TX bias current, TX output power and received optical power. Alarm flags indicate conditions likely to be associated with an in-operational link and cause for immediate action.

Data Address	Bits	Name	Description
112	7	Temp High Alarm	Set when internal temperature exceed high alarm level
	6	Temp Low Alarm	Set when internal temperature is below low alarm level
	5	Vcc High Alarm	Set when internal supply voltage exceed high alarm level
	4	Vcc Low Alarm	Set when internal supply voltage is below low alarm level
	3	TX Bias High Alarm	Set when internal TX Bias current exceed high alarm level
	2	TX Bias Low Alarm	Set when internal TX Bias current is below low alarm level
	1	TX Power High Alarm	Set when internal TX output power exceed high alarm level
	0	TX Power Low Alarm	Set when internal TX output power is below low alarm level
113	7	RX Power High Alarm	Set when internal RX input power exceed high alarm level
	6	RX Power Low Alarm	Set when internal RX input power is below low alarm level
	5	Reserved Alarm	
	4	Reserved Alarm	
	3	Reserved Alarm	
	2	Reserved Alarm	
	1	Reserved Alarm	
	0	Reserved Alarm	
114-127	All	Reserved	

Table D.6: Alarm Flag Bits (2-wire Address A3h)

SERIAL ID DESCRIPTION:

The SPLC-20-9D-2-B module provides memory mapped identification information that describes the V_SFP's capabilities, standard interfaces, manufacturer and other information. The information is static and is written at the time of manufacture. The serial ID and any other portion of memory map may be read "byte by byte" or in a "block read". The contents of the serial ID is shown in table D.7 below.

Data Address	Field Size (Bytes)	Name of field	Description of field
BASE OF FIELDS			
128	1	Identifier	Type of serial transceiver (see Table D.2)
129	1	Reserved	
130	1	Connector	Code for connector type (see Table D.3)
131-139	9	Reserved	
140	1	BR, Nominal	Nominal bit rate, units of 100Mbps
141	1	Reserved	
142	1	Length (9µ) - km	Link Length supported for 9/125 µm fiber, units of km
143	1	Length (9µ)	Link Length supported for 9/125 µm fiber, units of 100 m
144	1	Length (50µ)	Link Length supported for 50/125 µm fiber, units of 10 m
145	1	Length (62.5µ)	Link Length supported for 62.5/125 µm fiber, units of 10 m
146	1	Length (Copper)	Link Length supported for copper, units of meters
147	1	Reserved	
148-163	16	Vendor name	SFP vendor name (ASCII)
164-167	4	Reserved	
168-183	16	Vendor PN	Part number provided by SFP vendor (ASCII)
184-187	4	Reserved	
188-189	2	Wavelength	Laser Wavelength
190	1	Reserved	
191	1	CC_BASE	Check code for Base ID fields (address 128-190)
EXTENDED ID FIELDS			
192-193	2	Reserved	
194	1	BR, Max	Upper bit rate margin, units of 100Mbps
195	1	BR, Min	Lower bit rate margin, units of 1Mbps
196-205	10	Vendor SN	Serial number provided by vendor (ASCII)
206-211	6	Reserved	
212-217	6	Date Code	Vendor's manufacturing date code (see Table D.4)
218-222	5	Reserved	
223	1	CC_EXT	Check code for the Extended ID fields (address 192 - 222)

Table D.7: Serial ID Data Fileds (2-wire Address A3h)

SERIAL ID (Continued):

Identifier

The identifier value specifies the physical device described by the serial information. This value shall be included in the serial data. The defined identifier values are shown in table D.8.

Value	Description of physical device
00h-7Fh	Reserved
80h	Video SFP (V_SFP) transceiver
81h	Video SFP (V_SFP) dual transmitters
82h	Video SFP (V_SFP) dual receivers
83-FFh	Vendor specific

Table D.8: Identifier Values

Connector

The Connector value indicates the external connector provided on the interface. The defined connector values are shown in table D.9.

Value	Description of connector
00h-7Fh	Reserved
80h	Duplex LC
81h	Simplex ST
82h	Simplex Mini-BNC
83h-84h	Reserved
85-FFh	Vendor specific

Table D.9: Connector Values

Date Code:

The date code is an 8-byte field that contains the vendor's date code in ASCII characters. The date code is mandatory. The date code shall be in the format specified by table D.10.

Data Address	Description of field
84-85	ASCII code, two low order digits of year. (00 = 2000).
86-87	ASCII code, digits of month (01 = Jan through 12 = Dec)
88-89	ASCII code, day of month (01-31)

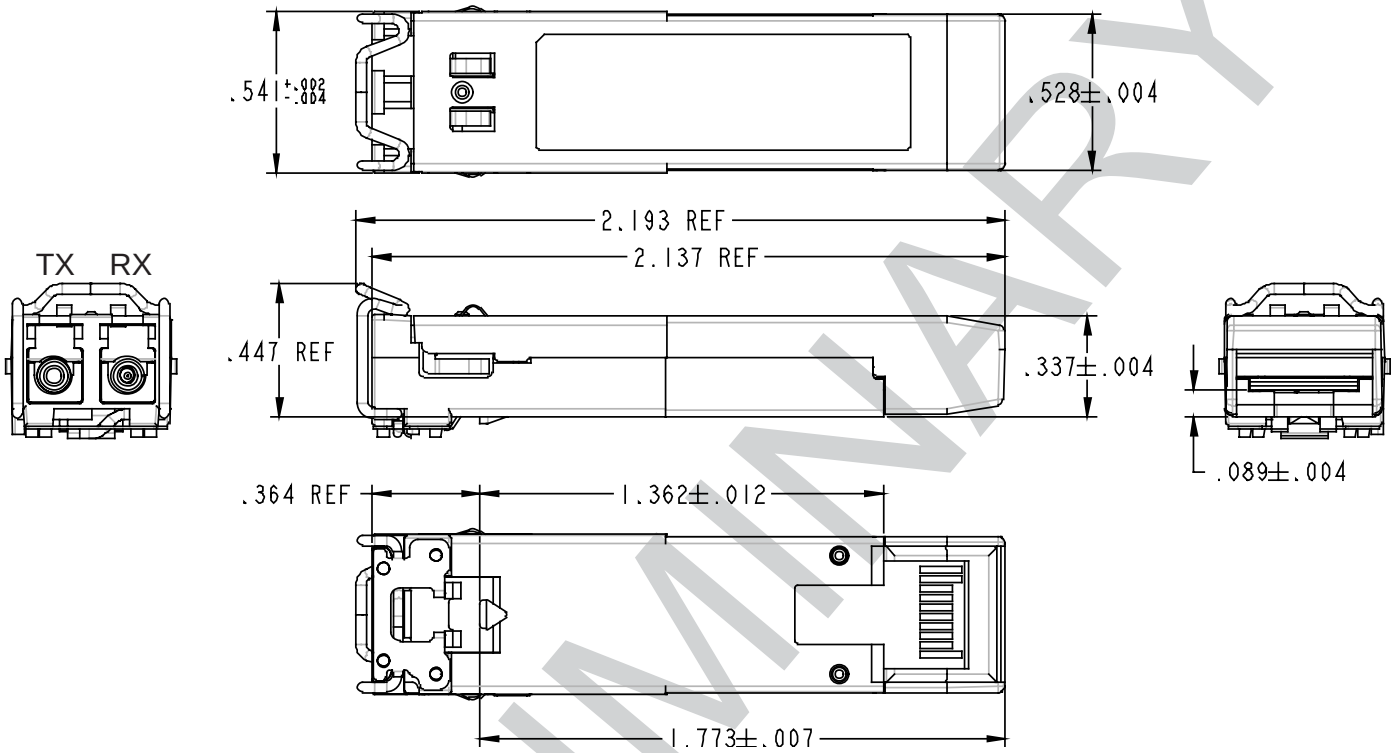
Table D.10: Date Code

USER WRITABLE MEMORY:

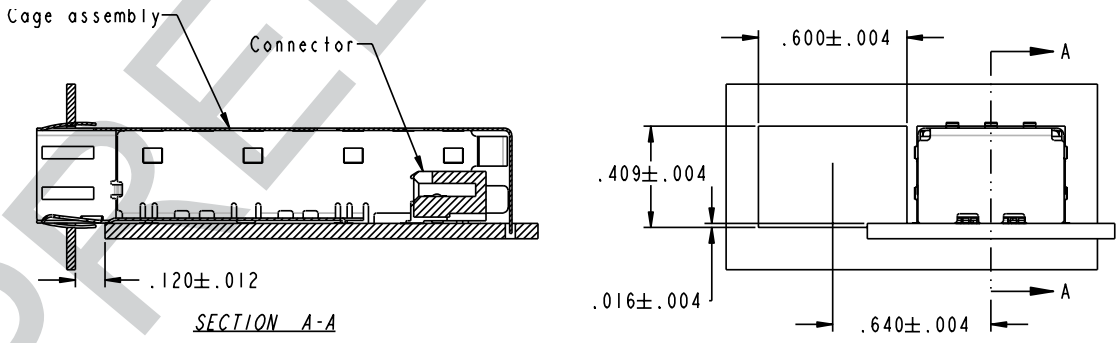
Data Address	# Bytes	Name	Description
223-255	32	User EEPROM	User Writable EEPROM

Table D.11: User Accessible EEPROM (2-wire Address A2h)

V_SFP MECHANICAL DIMENSIONS (inches) with BAIL ACTUATOR

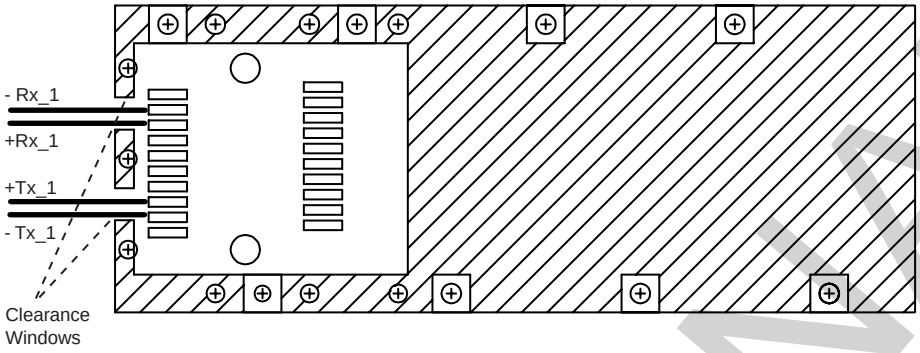


V_SFP PANEL CUTOUT

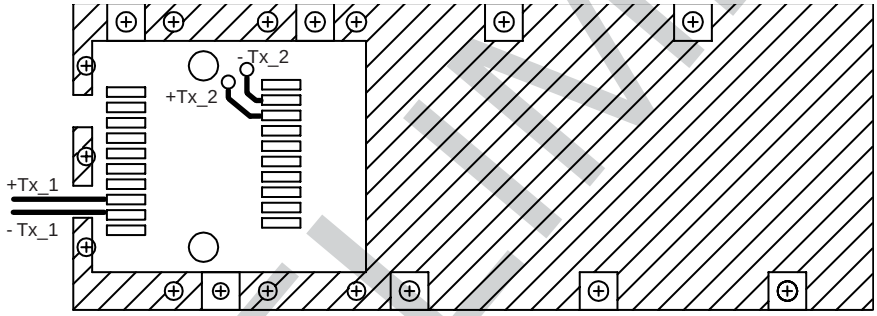


VIDEO SFP RECOMMNEDED HOST LAYOUT:

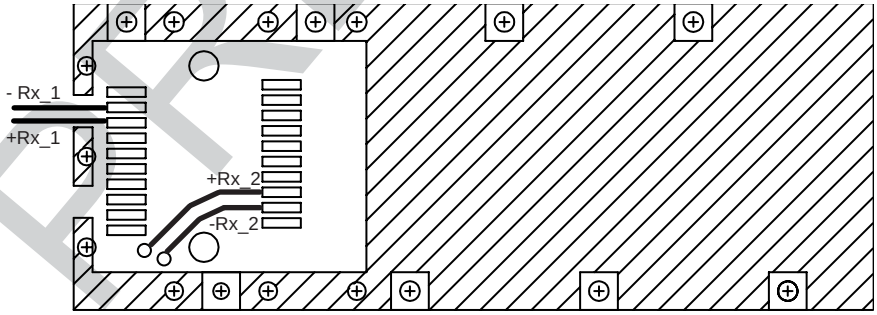
The video transceiver, dual transmitter, dual receiver, simplex transmitter, and simplex receiver modules share identical signal pin-outs. This provides the host flexibility to design one PCB to accommodate all three video SFPs. The video cage, however has only two signal trace clearance windows. Therefore, we recommend routing ±TX_2 and ±RX_2 signal traces to the bottom PCB layer before crossing through the video SFP cage outline.



Video SFP Transceiver SPLC-20-9D-X-X (TX/TX) NOTE: ±TX_2 AND ±RX_2 are not internally connected in Video SFP transceiver



Dual Transmitter Video SFP SP2T-20-9D-X-X (TX/TX) NOTE: ±TX_2 are not internally connected in simplex transmitter Video SFP (SP1T-20-9D-X-B)



Dual Receiver Video SFP SP2R-20-9D-X-X (RX/RX) NOTE: ±RX_2 are not internally connected in simplex receiver Video SFP (SP1R-20-9D-X-X)

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