DATA SHEET

SPLC063B1

80 Channel Segment LCD Driver

Preliminary

SEP. 19, 2007

Version 0.1

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80 CHANNEL SEGMENT LCD DRIVER

1. GENERAL DESCRIPTION

The SPLC063B1 is a LCD driver LSI which is fabricated by low power CMOS technology. Basically it consists of two set of 40-bit bi-directional shift registers, 40 data latch flip-flops and 40 liquid crystal display driver circuits. It has 80-channel outputs and can be applied as segment driver. The SPLC063B1 receives serial display data from a display control LSI, converts it into parallel data and supplies liquid crystal display waveforms to the liquid crystal. Its interface is compatible with the SPLC100. It reduces the number of LSI's and lowers the cost of a LCD module.

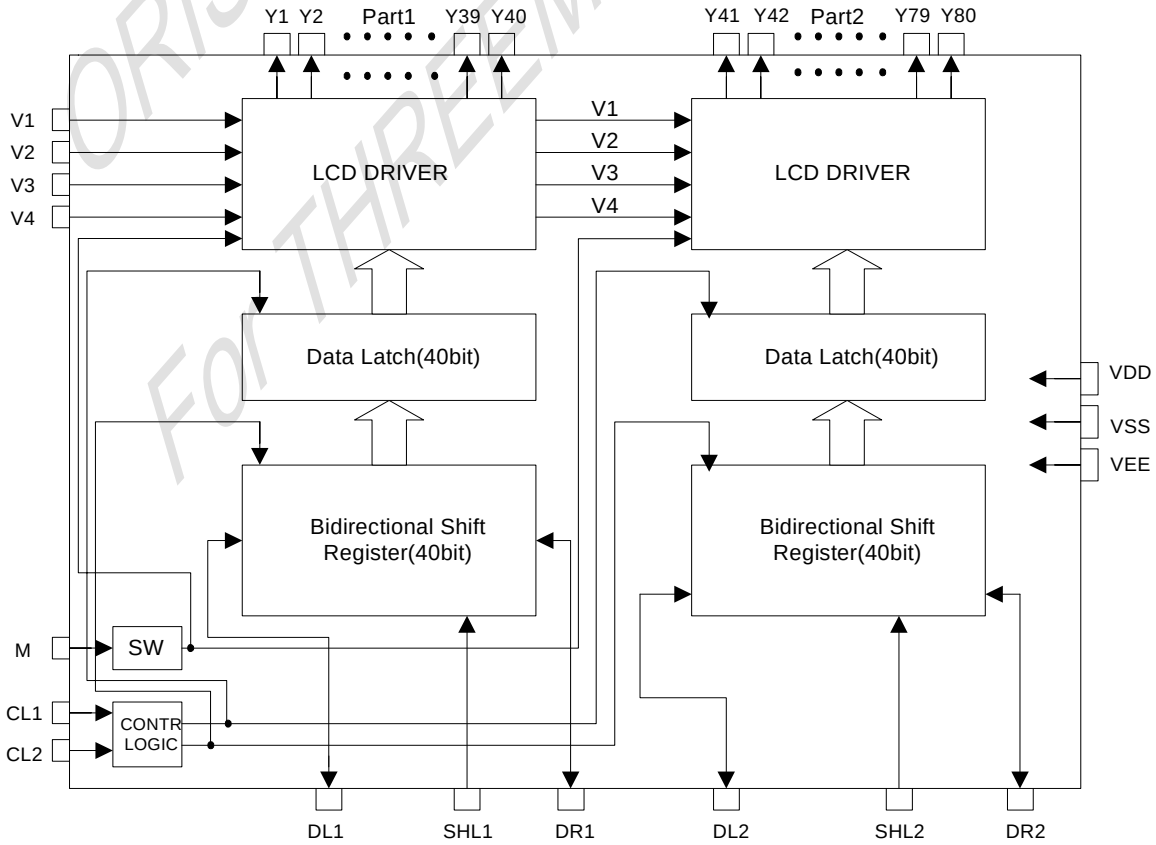
2. FEATURES

- Liquid crystal display driver with serial/parallel conversion function.
- Interface compatible with the SPLC100; connectable with SPLC780.
- Internal output circuits for LCD driver: 80
- Internal serial/parallel conversion circuits:
  - 40-bit bi-directional shift register X 2
  - 40-bit latch X 2
- Power supply:
  - Internal logic: 2.7V - 5.5V
  - Liquid crystal display driver circuit: 3.0V - 8V
- CMOS process.

3. ORDERING INFORMATION

Product Number	Package Type
SPLC063B1-C	Chip form
SPLC063B1-HQ061	Green Package form - QFP 100L

4. BLOCK DIAGRAM



4.1. Block Functions

4.1.1. LCD driver

Select one of four levels of voltage V1, V2, V3, and V4 for driving a LCD and transfer it to the output terminals according to the combination of M and the data in the latch circuit.

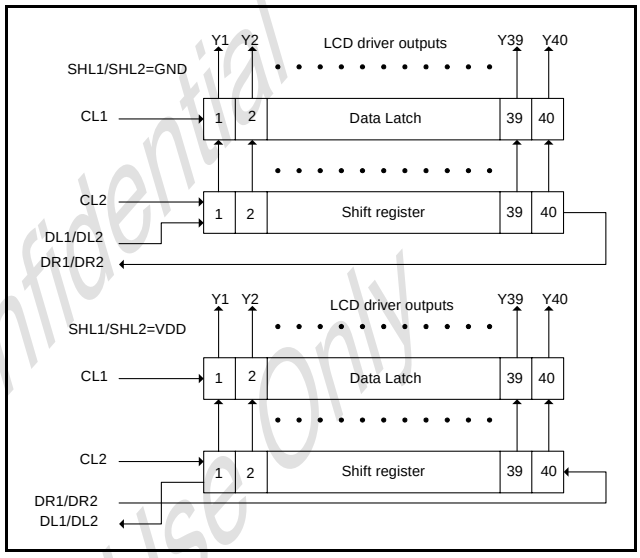
4.1.2. Data latch

Latches the data input from the bi-directional shift register at the fall of CL1 and transfer its outputs to the LCD driver circuits.

4.1.3. Bi-directional shift register

Shifts the serial data at the fall of CL2 and transfuse the output of each bit of the register to the latch circuit. When SHL1/SHL2 = GND, the data input from DL1/DL2 shifts from bit 1 to bit 40 in order of entry.

On the other hand, when SHL1/SHL2 = VDD, the data shifts from bit 40 to bit-1. The data of the last bit of the register is latched to be output from DR1/DR2 at the rise of CL2, when SHL1/SHL2 = GND. The data of the last bit of the register is latched to be output from DL1/DL2 at the rise of CL2 when SHL1/SHL2 = VDD.



Relation between SHL1/SHL2 and the Shift Direction

5. SIGNAL DESCRIPTIONS

<table>
<tr><th>Mnemonic (No.)</th><th>Input
Output</th><th colspan="2">Name</th><th>Description</th><th>Interface</th></tr>
<tr><td>VDD (59)</td><td rowspan="3">Power</td><td colspan="2">Operating Voltage</td><td>For logical circuit (2.7V - 5.5V)</td><td rowspan="3">Power Supply</td></tr>
<tr><td>VSS (GND) (55)</td><td colspan="2" rowspan="2">Negative Supply Voltage</td><td>0V (GND)</td></tr>
<tr><td>VEE (50)</td><td>For LCD driver circuit</td></tr>
<tr><td>V1, V2 (51, 52)</td><td>Input</td><td colspan="2" rowspan="2">LCD driver output voltage level</td><td>Bias voltage level for LCD driver (Select level)</td><td rowspan="2">Power</td></tr>
<tr><td>V3, V4 (53, 54)</td><td>Input</td><td>Bias voltage level for LCD driver
(Nonselect level)</td></tr>
<tr><td>Y1 - Y40</td><td>Output</td><td rowspan="3">Part1</td><td>LCD driver</td><td>LCD driver output</td><td>LCD</td></tr>
<tr><td>SHL1 (57)</td><td>Input</td><td rowspan="2">Data Interface</td><td>Selection of the shift direction of shift register
<table><tr><td>SHL1</td><td>DL1</td><td>DR1</td></tr><tr><td>VDD</td><td>OUT</td><td>IN</td></tr><tr><td>VSS</td><td>IN</td><td>OUT</td></tr></table></td><td>VDD or VSS</td></tr>
<tr><td>DL1, DR1 (61, 62)</td><td>Input
Output</td><td>Data input/output of shift register (part1)</td><td>Controller or
SPLC063B1</td></tr>
<tr><td>Y41 - Y80</td><td>Output</td><td rowspan="3">Part2</td><td>LCD driver</td><td>LCD driver output</td><td>LCD</td></tr>
<tr><td>SHL2 (58)</td><td>Input</td><td rowspan="2">Data Interface</td><td>Selection of the shift direction of shift register
<table><tr><td>SHL2</td><td>DL2</td><td>DR2</td></tr><tr><td>VDD</td><td>OUT</td><td>IN</td></tr><tr><td>VSS</td><td>IN</td><td>OUT</td></tr></table></td><td>VDD or VSS</td></tr>
<tr><td>DL2, DR2 (63, 64)</td><td>Input Output</td><td>Data input/output of shift register (part 2)</td><td>Controller or
SPLC063B1</td></tr>
<tr><td>M (65)</td><td>Input</td><td colspan="2">Alternated signal for LCD driver output</td><td>The alternating signal to convert LCD driver waveform to AC</td><td>Controller</td></tr>
<tr><td>CL1, CL2 (56, 60)</td><td>Input</td><td colspan="2">Data shift/latch clock</td><td>CL1: Data latch clock
CL2: Data shift clock</td><td>Controller</td></tr>
</table>

6. FUNCTIONAL DESCRIPTIONS

6.1. Dot Matrix LCD Driver with 80 Channel Outputs.

6.2. Input / Output Signal

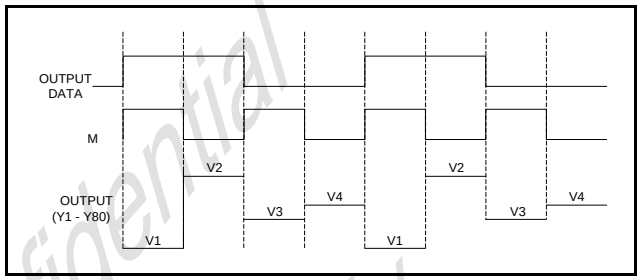
— Output: 40 X 2 channel waveform for LCD driving

— Input:

1). Serial display data and control pulse from the controller LSI.

2). Bias voltage (V1 - V4).

6.3. LCD Output Waveform



V1, V2: selected level

V3, V4: Non-selected level

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristic	Symbol	Value	Unit
Operation Voltage	VDD	-0.3 to +7.0	V
LCD Driver Supply Voltage	VEE	VDD-10V to VDD+0.3V	V
Operating Temperature	T_A	-20 to +75	°C
Storage Temperature	T_{STO}	-55 to +125	°C
Input voltage (1)	V_{IN1}	-0.3 to VDD+0.3	V
Input voltage (2)	V_{IN2}	VDD+0.3 to VEE-0.3	V

Note1: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

Note2: Input Voltage (2) applies to V1 - V4; Input Voltage (1) applies to other pins.

7.2. DC Characteristics

(VDD = 2.7V - 5.5V, VDD - VEE = 3.0V - 8V, T_A = +25℃)

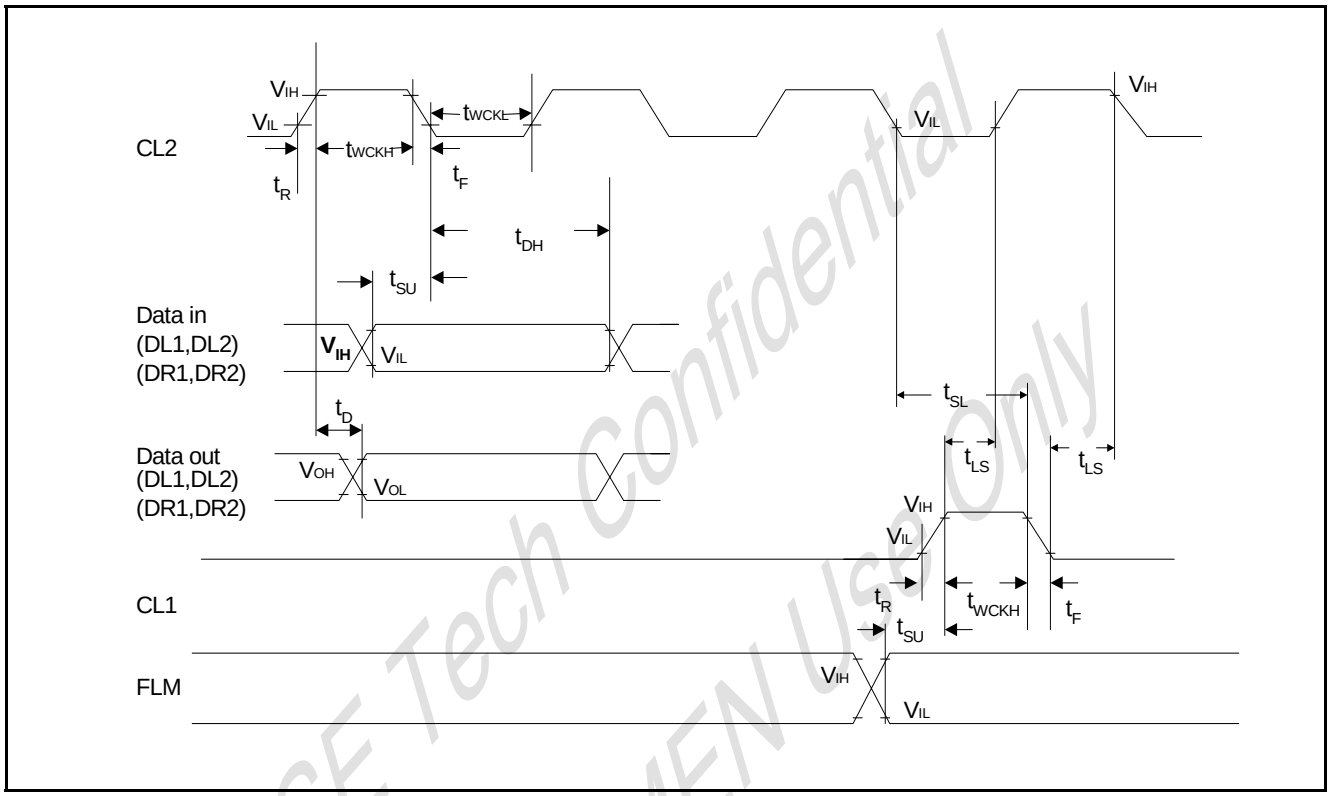
Characteristic	Symbol	Test Condition	Min.	Max.	Unit	Applicable Pin
Operating Current	I_{DD}	f_{CL2} = 400KHz	-	1.0	mA	VDD, VEE
Supply Current	I_{EE}	f_{CL1} = 1.0KHz	-	10	μA	
Input High Voltage	V_{IH}		0.7VDD	VDD	V	CL1, CL2, DL1, DL2, DR1, DR2, SHL1, SHL2, M
Input Low Voltage	V_{IL}		0	0.3VDD		
Input Leakage Current	I_{LKG}	V_{IN} = 0 to VDD	-5.0	5.0	μA	
Output High Voltage	V_{OH}	I_{OH} = -0.4mA	VDD-0.4	-	V	DL1, DL2, DR1, DR2
Output Low Voltage	V_{OL}	I_{OL} = +0.4mA	-	0.4		
Voltage Descending	V_{D1}	I_{ON} = 0.1mA for one of Y1 - Y80	-	1.1	V	V(V1 - V4)-Y(Y1 - Y80)
	V_{D2}	I_{ON} = 0.05mA for each Y1 - Y80	-	1.5		
Leakage Current	I_V	V_{IN} = VDD to VEE (Output Y1 - Y80; floating)	-10	10	μA	V1 - V4

7.3. AC Characteristics

(VDD = 2.7V - 5.5V, VDD - VEE = 3.0V - 8V, T_A = +25℃)

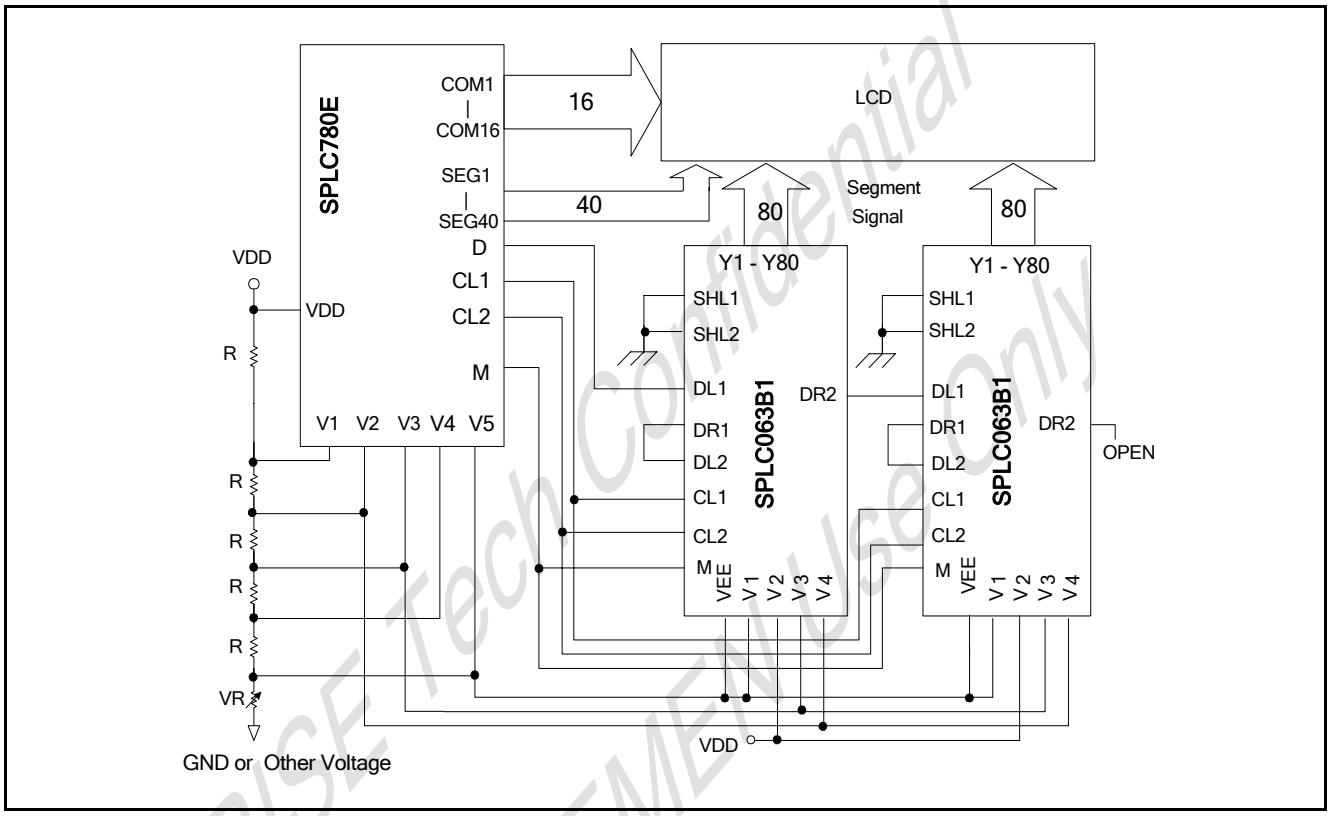
Characteristic	Symbol	Application Pin	Min.	Max.	Unit	Test Condition
Data shift frequency	f_{CL}	CL2	-	400	KHz	
Clock High level Width	t_{WCKH}	CL1, CL2	800	-	ns	
Clock Low level Width	t_{WCKL}	CL2	800	-		
Data set-up time	t_{SU}	DL1, DL2, DR1, DR2	300	-		
Clock set-up time	t_{SL}	CL1, CL2	500	-		(CL2→CL1)
Clock set-up time	t_{LS}		500	-		(CL1→CL2)
Clock rise/fall time	t_R/t_F		-	200		
Date delay time	t_D	DL1, DL2, DR1, DR2	-	500		C_L = 15pF
Date hold time	t_{DH}	DL1, DL2, DR1, DR2	300	-		

7.4. Timing Characteristic

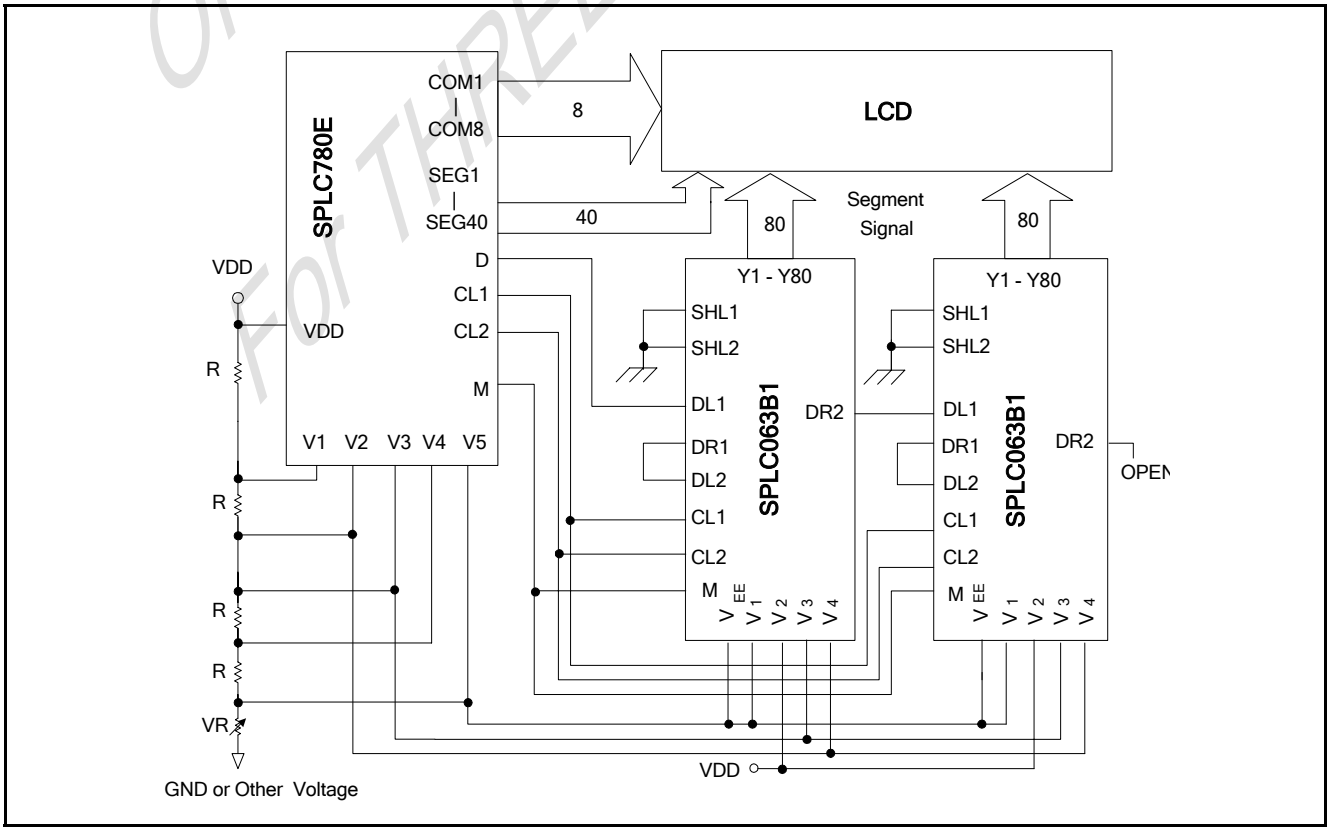


8. APPLICATION CIRCUITS

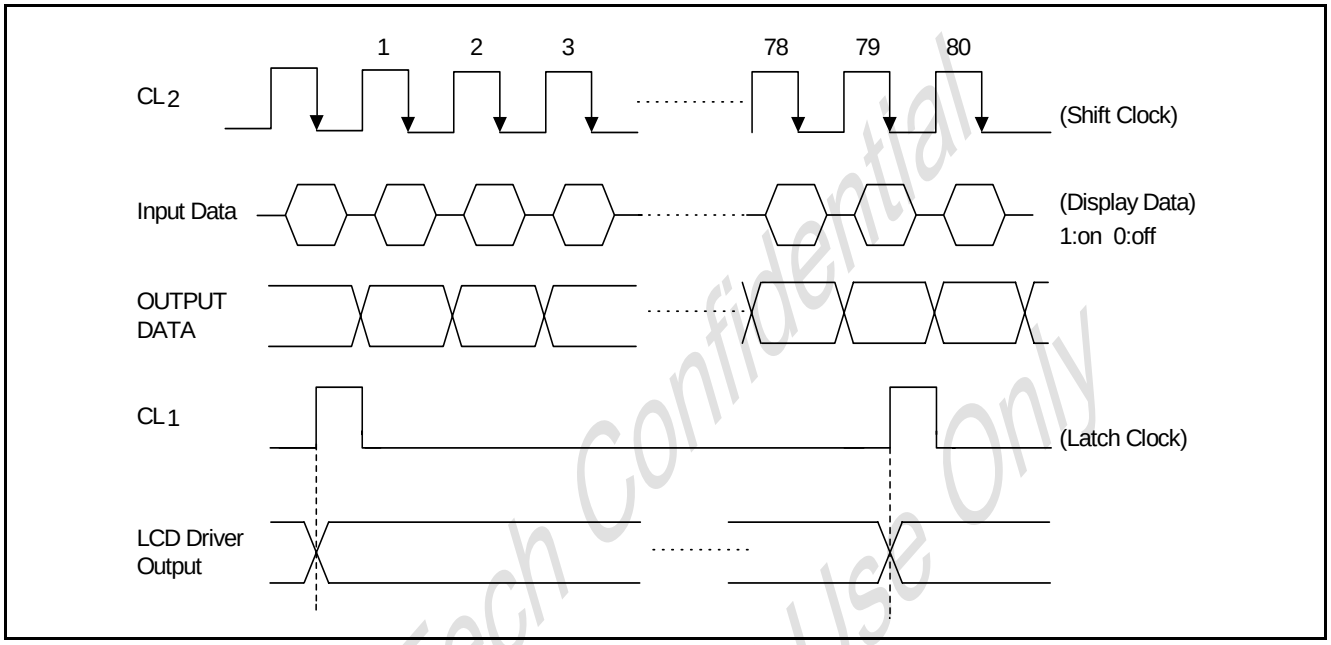
8.1. Application Circuit for 1/16 Duty, 1/5 Bias



8.2. Application Circuit for 1/8 Duty, 1/4 Bias

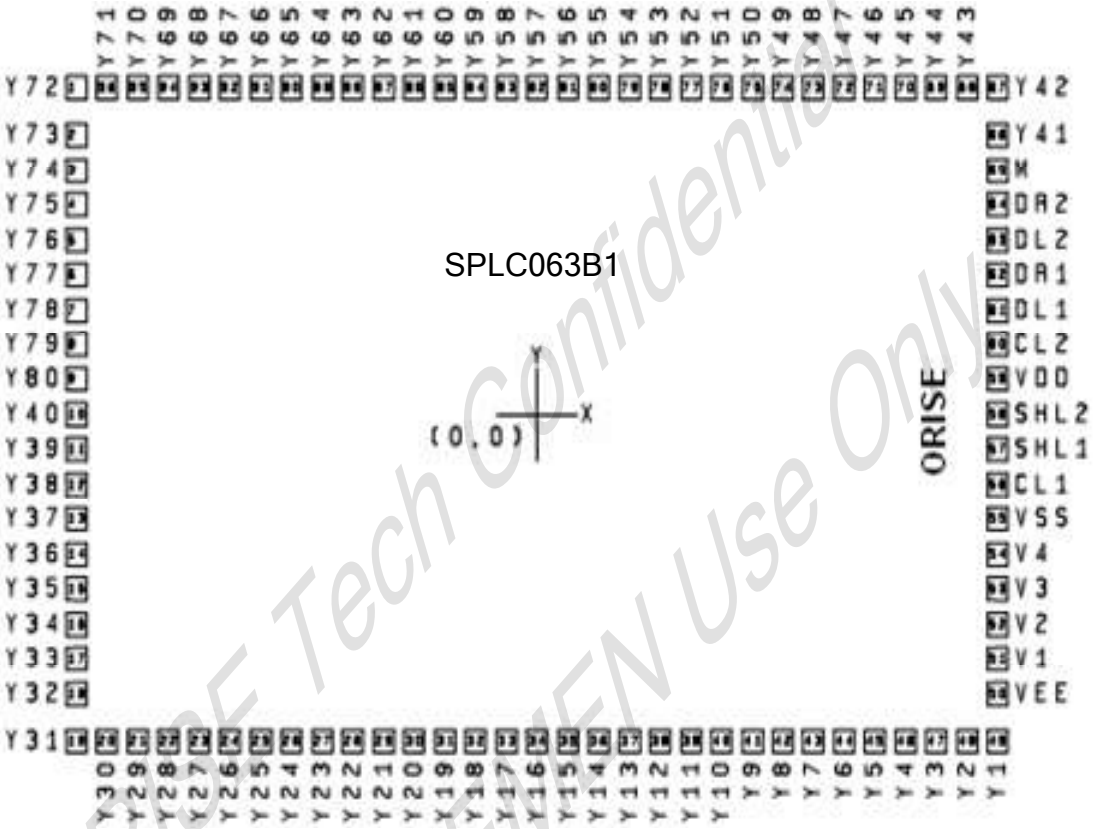


8.3. Timing Chart of Input and Output Data



9. PACKAGE/PAD LOCATIONS

9.1. PAD Assignment



Chip Size : 3296*2096μm

Pad Size : 86*86 μm

This IC's substrate should be connected to VDD

Note1: Chip size included scribe line.

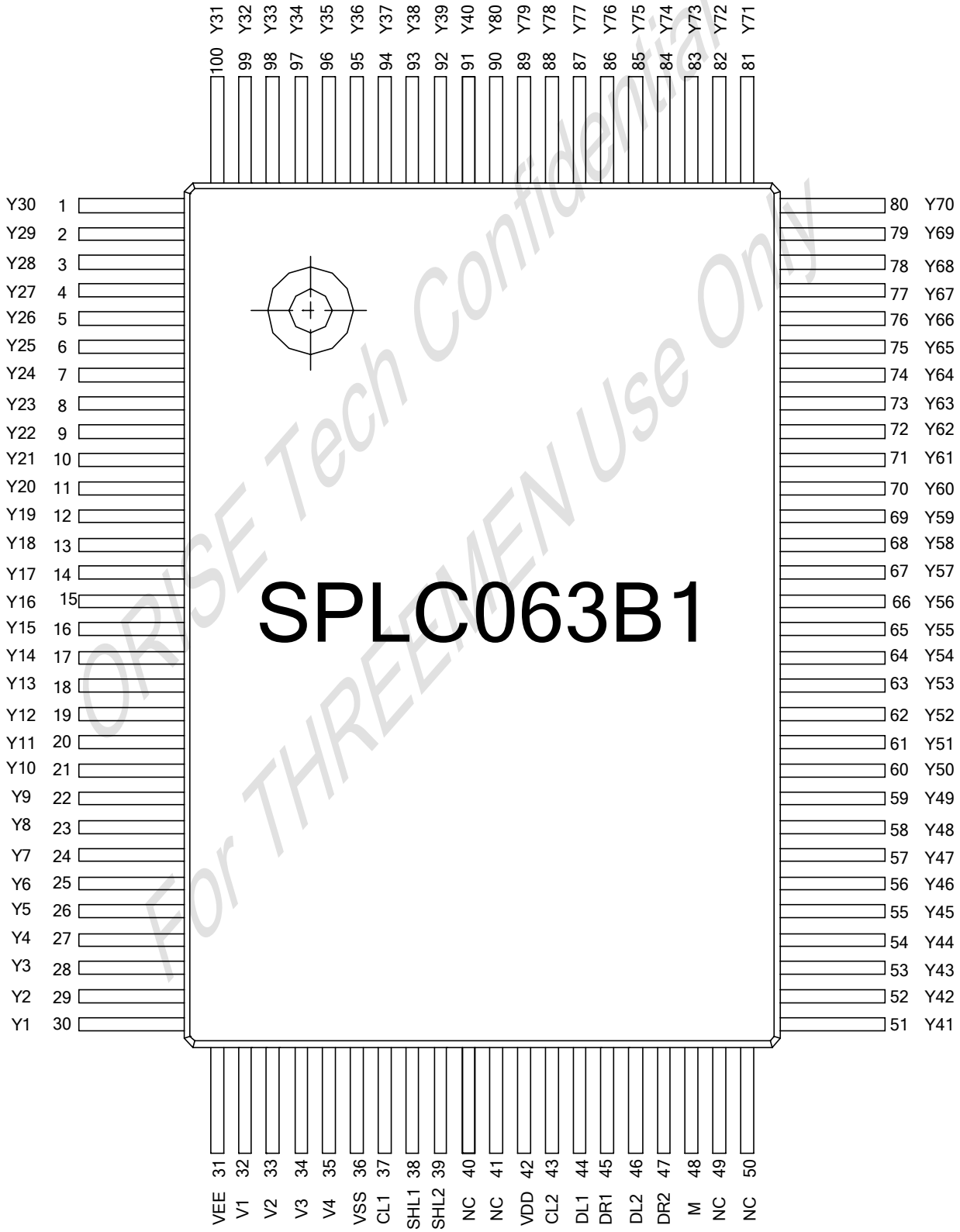
Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

9.2. PAD Locations

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
1	Y72	-1550	950	49	Y1	1550	-950
2	Y73	-1550	830	50	VEE	1550	-830
3	Y74	-1550	720	51	V1	1550	-720
4	Y75	-1550	610	52	V2	1550	-610
5	Y76	-1550	505	53	V3	1550	-505
6	Y77	-1550	400	54	V4	1550	-400
7	Y78	-1550	300	55	VSS	1550	-300
8	Y79	-1550	200	56	CL1	1550	-200
9	Y80	-1550	100	57	SHL1	1550	-100
10	Y40	-1550	0	58	SHL2	1550	0
11	Y39	-1550	-100	59	VDD	1550	100
12	Y38	-1550	-200	60	CL2	1550	200
13	Y37	-1550	-300	61	DL1	1550	300
14	Y36	-1550	-400	62	DR1	1550	400
15	Y35	-1550	-505	63	DL2	1550	505
16	Y34	-1550	-610	64	DR2	1550	610
17	Y33	-1550	-720	65	M	1550	720
18	Y32	-1550	-830	66	Y41	1550	830
19	Y31	-1550	-950	67	Y42	1550	950
20	Y30	-1435	-950	68	Y43	1435	950
21	Y29	-1325	-950	69	Y44	1325	950
22	Y28	-1215	-950	70	Y45	1215	950
23	Y27	-1110	-950	71	Y46	1110	950
24	Y26	-1005	-950	72	Y47	1005	950
25	Y25	-900	-950	73	Y48	900	950
26	Y24	-800	-950	74	Y49	800	950
27	Y23	-700	-950	75	Y50	700	950
28	Y22	-600	-950	76	Y51	600	950
29	Y21	-500	-950	77	Y52	500	950
30	Y20	-400	-950	78	Y53	400	950
31	Y19	-300	-950	79	Y54	300	950
32	Y18	-200	-950	80	Y55	200	950
33	Y17	-100	-950	81	Y56	100	950
34	Y16	0	-950	82	Y57	0	950
35	Y15	100	-950	83	Y58	-100	950
36	Y14	200	-950	84	Y59	-200	950
37	Y13	300	-950	85	Y60	-300	950
38	Y12	400	-950	86	Y61	-400	950
39	Y11	500	-950	87	Y62	-500	950
40	Y10	600	-950	88	Y63	-600	950
41	Y9	700	-950	89	Y64	-700	950
42	Y8	800	-950	90	Y65	-800	950
43	Y7	900	-950	91	Y66	-900	950
44	Y6	1005	-950	92	Y67	-1005	950
45	Y5	1110	-950	93	Y68	-1110	950
46	Y4	1215	-950	94	Y69	-1215	950
47	Y3	1325	-950	95	Y70	-1325	950
48	Y2	1435	-950	96	Y71	-1435	950

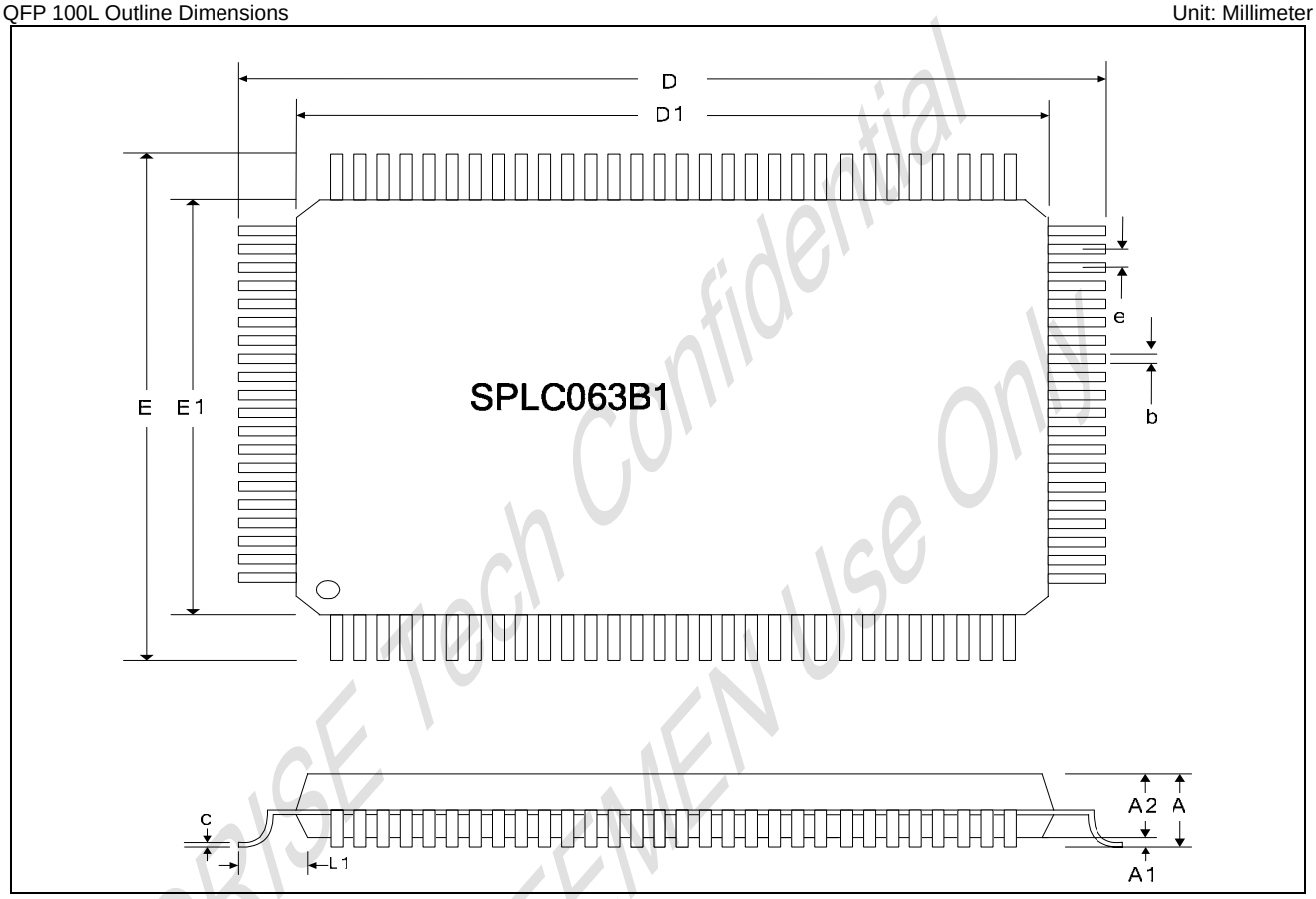
9.3. PIN Assignment

QFP 100L Top View



9.4. Package Information

QFP 100L Outline Dimensions Unit: Millimeter



Symbol	Dimension in mm		
	Min.	Nom.	Max.
A	--	--	3.40
A1	0.25	--	--
A2	2.73	2.85	2.97
b	0.25	0.30	0.38
c	0.13	0.15	0.23
D	23.00	23.20	23.40
D1	19.90	20.00	20.10
E	17.00	17.20	17.40
E1	13.90	14.00	14.10
e	0.65 BSC		
L1	1.60 REF		

10. LEAD FRAME PACKAGE PCB DESIGN AND MANUFACTURING GUIDELINES

10.1. Purpose

The purpose of this specification is to identify plastic surface mount devices (SMDs) those are sensitive to moisture-induced stress, so that they can be properly design PCB and assembly packaged, stored and handled to avoid subsequent mechanical damage during the assembly solder reflow attachment and /or repair operation.

10.2. Scope

10.2.1. PCB layout guideline

10.2.2. PCB process

10.2.3. Storage Condition and Period for Package

10.2.4. Recommended SMT Temperature Profile

10.3. Noun definition

10.3.1. NSMD: Non Solder Mask Defined

10.3.2. SMD: Solder Mask Defined

10.3.3. CSP: Chip scale Package

10.3.4. PCB :Printed Circuit Board

10.4. Responsibility unity:

ORISE Quality Assurance unity

10.5. Contents

10.5.1. Applicable documents

IPC-SM-782: Surface Mount Design & Land Pattern Standard

IPC-7351Generic Requirements for Surface Mount Design and Land Pattern Standard.

IPC-7525: Stencil Design Guidelines

J-STD-020: IPC/JEDEC Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Device

IPC JEDEC: J-STD-033A Standard for Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

IPC-HDBK-001: Handbook & Guide to the Requirements of Soldered Electronic Assemblies with Amendment 1

IPC -6016: Qualification & Performance Specification for High Density Interconnect (HDI) Layers or Boards

IPC-STD-003: Solderability Tests for Printed Boards

JESD22-B111: Board Level Drop Test of Components for Handheld Electronic Products

JESD22-B110: Subassembly Mechanical Shock

IPC-A-610: Acceptability of Electronic Assemblies

10.5.2. PCB layout guideline

PCB designer comply with IPC-SM-782 and IPC-7095 requirements is recommended

10.5.3. PCB process

10.5.3.1. Board material

The Glass transition temperature (Tg) of Board material greater than 170 degree C is recommended for Pb- free and Green package.

10.5.3.2. Surface Finishes

In order to achieve high assembly yields, use of a surface finish that is planar

And has good solderability performance is important. Below methods are all known to provide an acceptable land pad surface.

*OSP (Organic Solderability Preservative)

*Nihau (Electroplated nickel /gold)

*Immersion Ag

*Immersion Sn

10.5.3.3. Solder Paste: No clean flux is recommended.

10.5.3.4. Stencil Design Guidelines: Refer to IPC-7525 Stencil Design Guidelines process

10.5.3.5. Reflow Oven: Forced convection reflow with nitrogen is recommended for Pb-free and Green package..

10.5.3.6. Reflow profile: Using more than 8 zone oven is recommended for Pb-free and Green package.

10.5.3.7. To use IPC-A-610 is recommended for soldered electrical and electronic assemblies.

10.5.4. Storage condition and period for package

Orise technology evaluates all plastic surface mount devices (SMDs) to ICP/JEDEC J-STD-020A, moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices, or refers to IPC JEDEC J-STD-033A Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

10.5.4.1. The primary facts for the package storage include oxidation, static, and therefore, the following rules are recommended to be applied for the storage.

10.5.4.2. The storage temperature should be 25℃ ± 5℃, and the humidity should be in the range of 50% ± 10% R.H. after opening the dry pack.

After the dry bag is opened, devices that will be subjected to infrared reflow, vapor-phase reflow, or equivalent processing.

10.5.4.3. Must be:

a. Mounted within 168 hours(Level 3) and 72 hours(Level 4) at factory conditions of ≦ 30℃/ 60% R.H. or

b. Stored at ≦ 20% R.H.

10.5.4.4. Devices require baking, before mounting, if:

a. Humidity Indicator Card shown warning message when read at 25℃±5℃, or

b. 10.5.4.3 is not met.

10.5.4.5. If baking is required. Devices may be baking for:

a. 192 hour at 40℃+5℃/-0℃ and <5% R.H. for low temperature device containers, or

b. 24 hours at 125±5℃ for high temperature device containers

10.5.4.6. The storage condition should be consistent with the operation condition to prevent dewing phenomena.

10.5.4.7. The storage location should be kept away from water and smoke; an isolated area with positive pressure control is preferred.

10.5.4.8. For a long-term storage, it is recommended to keep in a container with Nitrogen in it.

10.5.4.9. Avoid heavy objects stacked on the pack.

10.5.4.10. Avoid the static damage; use an anti-static bag for the package.

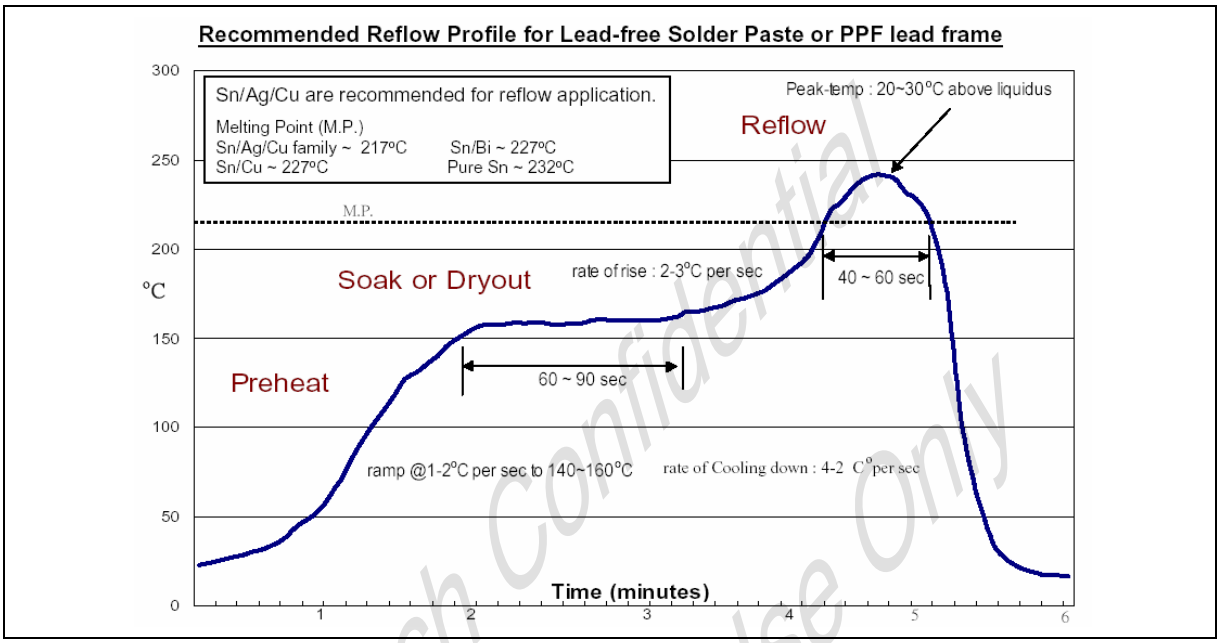
10.5.5. The classification of moisture sensitivity for Orise's product packages are shown in the following

For Lead Free / Green Packages

Package	Moisture sensitivity level	Max. Reflow temperature	Floor life storage condition	Dry pack
QFP	LEVEL 3	255 +5/-0℃	168Hrs @ ≦ 30℃/ 60% R.H.	Yes

10.5.6. Recommended SMT Temperature Profile

This "Recommended" temperature profile is a rough guideline for SMT process reference. Most of ORISE leadframe base product choice Matte Tin and Sn/Bi for plating recipe. For PPF (Pre-Plated Frame) product with 63/37 solder paste, we recommend 240℃~245℃ for peak temperature.



10.6. References

IPC:

http://www.ipc.org

*NEMI (National Electronics Manufacturing Initiative)

http://www.nemi.org

*HDPUG (High Density Package Users Group)

http://www.hdpug.org

*JEDEC (Joint Electronic Device Engineering Council)

http://www.jedec.org

*JEITA (Japan Electronic Industry Association)

http://www.jeita.org

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12. REVISION HISTORY

Date	Revision #	Description	Page
SEP. 19, 2007	0.1	Original	19