DATA SHEET

SUNPLUS

SPLC701B

11x12 and 6x12 Text and Graphics Liquid Crystal Display Controller/Driver

MAY. 17, 2005

Version 1.5

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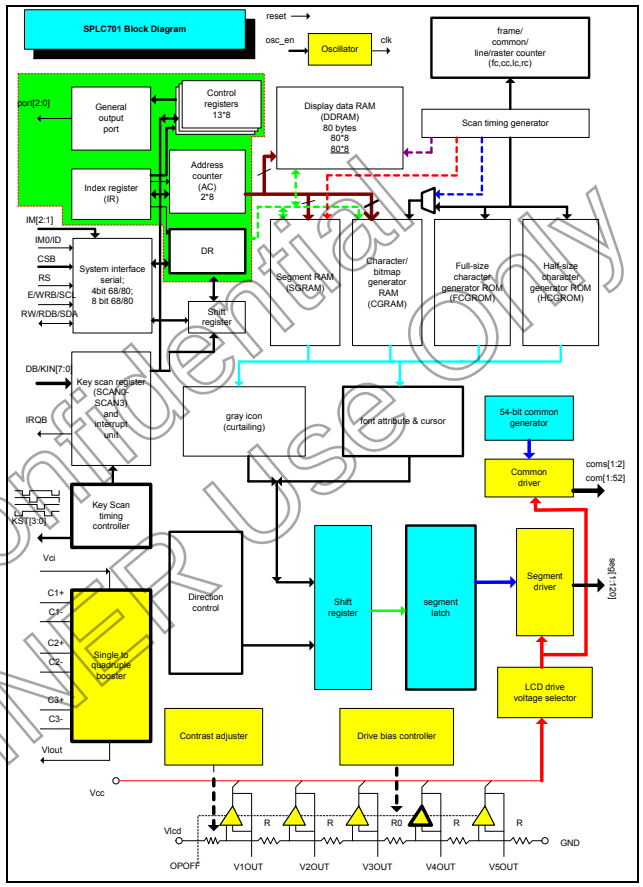
11x12 and 6x12 Text and GRAPHICS LIQUID CRYSTAL DISPLAY CONTROLLER/DRIVER

1. GENERAL DESCRIPTION

The SPLC701B, a fresh designed LCD controller with advanced CMOS technology from SUNPLUS, is able to display one to four lines of 10 kanji-font characters with 11 x 12 dots full-size format. A 5 x 12 dot half-size alphanumeric characters can also be displayed. It also has the capability to show 120 x 52 dots graphical LCD, 160 mono-blinking icons, and 40 gray-scale icons. With modern technology, the SPLC701B contain nine primary functions in a single compact chip.

1). Five types of MPU interface, 80/68 8-bit/4-bit and clock synchronous serial interface.
2). Key-scan support.
3). Varieties of dot-matrix LCD.
4). Three RAMs: one for character code, one for icon, and the other for graphics or user font.
5). Two ROMs: one for kanji-font, the other for alphanumeric characters.
6). 120-segment / 54-common driver.
7). 1X-4X booster.
8). Voltage follower & bias circuits.
9). Built-in RC-oscillator.

2. BLOCK DIAGRAM



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3. FEATURES

- Driver Output Circuits
  - Common outputs: 52 common + 2 common for icon
  - Segment outputs: 120 segment
- Internal Memory
  - Full-size Character Generator ROM (FCGROM):1,072,896 bits (8,128 characters x 11 x 12 dots)
  - Half-size Character Generator ROM (HCGROM): 15,360 bits (256 characters x 5 x 12 dots)
  - Character Generator RAM (CGRAM): 6,240 bits (40 characters x 12 x 13 dots)
  - Display Data RAM (DDRAM): 640 bits (80 half-size characters or 40 full-size characters)
  - Segment/Icon RAM (SGRAM/ICONRAM): 480 bits (160 mono-blinking icon + 40 gray- scale icon)
- MPU Interface
  - 8-bit parallel interface mode: 68-series and 80-series
  - 4-bit parallel interface mode: 68-series and 80-series
  - Serial interface mode: 3-pin clock synchronous serial interface
- Function Set
  - Font attribute
  - Character/line cursor
  - Full screen reversal
  - Combined display (super-imposed display) of kanji characters and bitmap graphics
  - Partial display
  - Vertical scroll (dot unit)
  - COM / SEG bi-directions (4-type LCD application available)
  - H/W reset (RESETB)
- I/O Peripheral Support
  - Up to 4*8(32key) key matrix (only serial interface)
  - Three general output ports
  - One interrupt source
- Build-In Analog Circuit
  - Internal RC OSC circuit or external clock
  - Electronic-volume for contrast control (32 steps)
  - Voltage converter (1 to 4 times)
  - Voltage follower & bias circuit
- Operating Voltage Range
  - Power voltage (VCC): 2.0V - 3.6V
  - LCD driving voltage (VLCD = V1 - VSS): 4.5V - 12V (max.)
- Low-Power Operating
  - Single, double, triple, or quadruple booster for LCD voltage
  - Amplifier for low-power LCD driving supply and bleeder-resistors incorporated
  - Power saving functions: standby and sleep modes
  - Wake-up function: key scan interrupt
  - Multiple duty selection
  - Programmable LCD duty ratios and bias values
- Display Capability
  - Text mode (4-line 10-character or 20 half-size characters) + 200 icons
  - Graphical mode (120x52 graphics display) + 200 icons
  - Super-imposed mode (Text mode + Graphical mode)
  - Icon is consisted of 160 mono-blinking icons + 40 gray-scale icons
- Applicable Duty Ratios

Display Size(NL)	Duty	Contents of Outputs
0 line(000)	2	Icon
1 line(001)	15	Icon + 1*10 full-size characters (120*13 dot-matrix)
2 line(010)	28	Icon + 2*10 full-size characters (120*26 dot-matrix)
3 line(011)	41	Icon + 3*10 full-size characters (120*39 dot-matrix)
4 line(100)	54	Icon + 4*10 full-size characters (120*52 dot-matrix)

- Applicable Character/Pixel Per Line

Character/Pixel	NC
6 full-size character/72 pixel	00
8 full-size character/96 pixel	01
10 full-size character/120 pixel	10

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4. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
IM2 - 0	2 - 4	I	Interface mode, 80/68/serial; 8/4, please refer below table on next section
OPOFF	5	I	Voltage follower(V1-V5 OP) off VDD: disable internal OP VSS: enable internal OP
TEST	6	I	Test pin, please leave it open
DB7/KIN7 DB6/KIN6 DB5/KIN5 DB4/KIN4 DB3/KIN3 DB2/KIN2 DB1/KIN1 DB0/KIN0	15 16 17 18 19 20 21 22	I/O	**Parallel interface:** Data bus **Serial interface:** Key scan bus
RESETB	23	I	System reset signal, low active
CSB	24	I	Chip select, low active
RS	25	I	**Parallel interface:** Register select **Serial interface:** 32-key wakeup enable
E/WRB/SCL	26	I	68enable/80wrb/serial CLK
RW/RDB/SDA	27	I/O	68rw/80rdb/serial data
OSC1	33	I	Test pin, please leave it open
OSC2	32	I	Test pin, please leave it open
VTEST1	61	I	Tied to VSS
VTEST2	62	-	Test pin, please leave it open
VTEST3*	63	I	Tied to VSS
PORT2 - 0	7 - 9	O	Port2 - 0 are general digital output
IRQB	10	O	Interrupt request when key was pressed, low active
KST3 - 0	11 - 14	O	Key strobe signal (key scan cycle: internal CLK divided by 64,128,256,512)
COMS2/S1 COMS1/S2	92 245	O	Common output signals for icon(such as battery, antenna, status icon)
COM7/46 - COM26/27 COM47/6 - COM52/1 COM46/7 - COM42/11 COM41/12 - COM35/18 COM34/19 - COM31/22 COM30/23 - COM28/25 COM27/26 COM6/COM47 COM5/COM48 COM4/49 - COM1/52	65 - 85 86 - 91 213 - 217 219 - 226 228 - 231 233 - 235 237 238 239 241 - 244	O	Common output signals for character/graphics
SEG120/1 - SEG1/120	212 - 93	O	Segment output signals for segment-icon display and character/graphics display.
VCI	37, 38	-	Power supply to the booster, if VCI short with VDD, **do not use ITO to short <VDD,VCI>** , please short it on FPC metal line or PCB trace, <VSS,VDD> need 0.1μ capacitor placed to IC as close as possible.

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Mnemonic	PIN No.	Type	Description
VDD (VCC)	34, 35	-	Power supply for logic, if VCI short with VDD, **do not use ITO to short <VDD,VCI>** , please short it on FPC metal line or PCB trace, **<VSS,VDD>** need **0.1μ capacitor** placed to IC as close as possible.
VSS VSSP	28, 29 30, 31	I	Ground pin, **do not use ITO to short <VSS,VSSP>**, please short it on FPC metal line or PCB trace, **<VSS,VDD>** need **0.1μ capacitor** placed to IC as close as possible.
VLCD	54, 55	-	Power supply for LCD driver. **<VLCD,VSS>** need **0.1μ capacitor** placed to IC as close as possible.
V5 - 1	60 - 56	I/O	Using capacitor to stabilize the output or supply voltage externally.
VLOUT	52, 53	-	Booster output. **<VLOUT,VSS>** need **0.1μ capacitor** placed to IC as close as possible.
C1+	48, 49	Booster capacitance	External capacitance should be connected when booster works at 2X/3X/4X.
C1-	50, 51	Booster capacitance	External capacitance should be connected when booster works at 2X/3X/4X.
C2+	44, 45	Booster capacitance	External capacitance should be connected when booster works at 3X/4X.
C2-	46, 47	Booster capacitance	External capacitance should be connected when booster works at 3X/4X.
C3+	40, 41	Booster capacitance	External capacitance should be connected when booster works at 4X.
C3-	42, 43	Booster capacitance	External capacitance should be connected when booster works at 4X.
VDDDUM1 – 2	240, 74	Dummy	Dummy for default mode setting
VSSDUM1 – 2	1, 64	Dummy	Dummy for default mode setting
TI3 TI2 TI1 TI0 SE	236 232 227 223 218	Test pin	Test pin, please leave it open
XFUSE1, XFUSE0	36, 39	Test pin	Test pin, please leave it open

4.1. Code information

Sunplus provide multi-lingual character, below is some example.

Code #	Description	Status
002	Simplified Chinese	ES
003	Japanese Kanji	Production
004	Traditional Chinese	ES
005	Korean	ES
xxx	Unicode database of 30,000 characters	ES

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5. FUNCTIONAL DESCRIPTIONS

5.1. System Interface

The SPLC701B provides five types of MPU interface:

1). Three-pin clock-synchronized serial interface

2). Motorola 68-system 4-bit

3). Motorola 68-system 8-bit

4). Intel 80-system 4-bit

5). Intel 80-system 8-bit

The interface mode is selected by the IM[2-0] pins.

IM2	IM1	MPU Interface Mode
0	0	Clock-synchronized serial interface
0	1	68-system bus interface
1	0	Inhibited
1	1	80-system bus interface

Serial:

When two SPLC701B share the same csb, scl, sda bus, the two panel is identified by whether IM0 equal start byte ID bit.

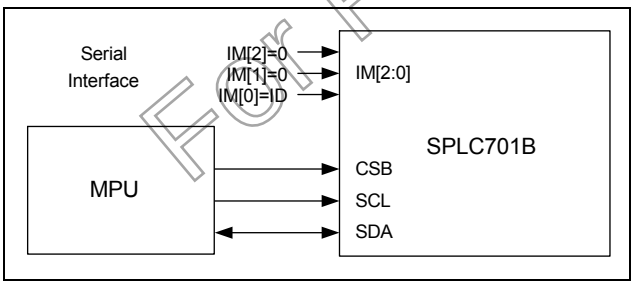
IM0	Start Byte
0	01110-**0**
1	01110-**1**

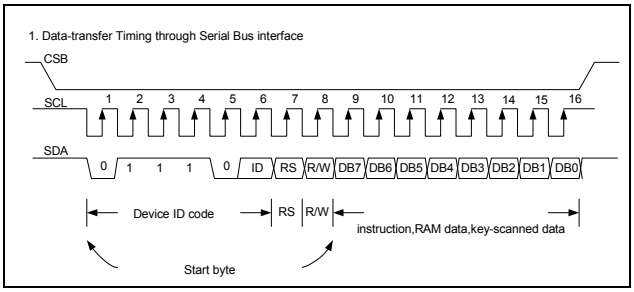
Parallel:

Bus width selection:

IM0	Bus Width Selection
0	8-bit
1	4-bit

5.2. Serial Interface





Setting the IM1 and IM2 pins (interface mode pins) to the GND level allows standard clock-synchronized serial data transfer, using the chip select line (CSB), serial data line (SDA), and serial transfer clock line (SCL). For a serial interface, the IM0/ID pin function uses an ID pin.

The SPLC701B initiates serial data transfer by transferring the start byte at the falling edge of CSB input. It ends serial data transfer at the rising edge of CSB input. The SPLC701B is selected when the 6-bit chip address in the start byte transferred from the transmitting device matches the 6-bit device identification code assigned to the SPLC701B. The SPLC701B, when selected, receives the subsequent data string. The least significant bit of the identification code can be determined by the ID pin. The five upper bits must be 01110. The seventh bit of the start byte is used as a register select bit (RS): that is, when RS = 0, an instruction can be issued or key scan data can be read, and when RS = 1, data can be written to or read from RAM. Read or write is selected according to the eighth bit of the start byte (R/W bit) as shown in below table. After receiving the start byte, the SPLC701B receives or transmits the subsequent data byte-by-byte. The data is transferred with the MSB first. Two bytes of RAM read data after the start byte are invalid. The SPLC701B starts to read correct RAM data from the third byte.

Register Selection by RS and R/W Bits.

RS	RW	Description
0	0	Write to the Index Register (IR)
0	1	Parallel: Read the Status Register; Serial: Key Scan Data Register(SR)
1	0	Write to the control registers: RAM Address Register, and RAM-Write-Data-Register(WD)
1	1	Read the RAM-Read-Data-Register(RD)

Note1: Key scan interface is available for serial interface only.

Note2: In bus mode, RS and RW are pin input; in serial mode, RS and RW are embedded in the start byte.

Note3: Every time you want to access R15 - 0, make sure IR is correctly point to it.

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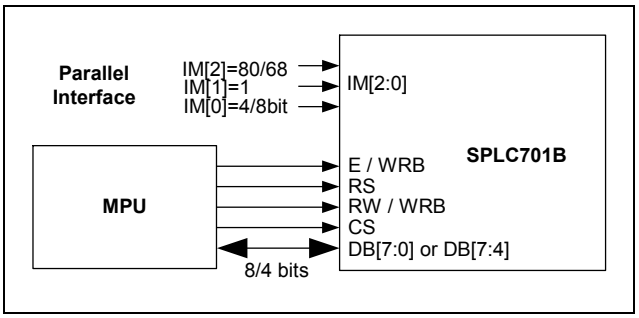
5.3. Parallel Interface



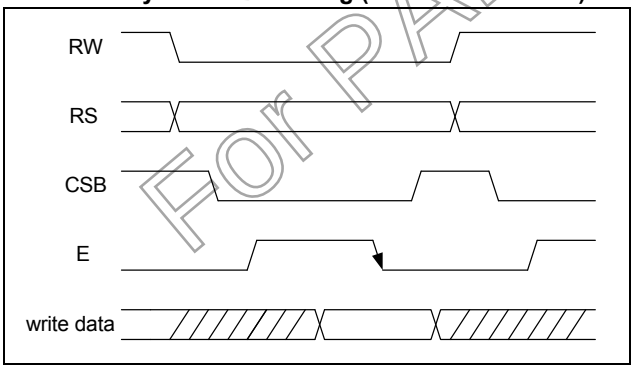
5.3.1. 8-bit interface

Setting the IM2/1/0 (interface mode) to the GND/VCC/GND level allows E-clock-synchronized 8-bit parallel data transfer. Setting the IM2/1/0 (interface mode) to the VCC/VCC/GND level allows 80-system 8-bit parallel data transfer. When the number of buses or the mounting area is limited, use a 4-bit bus interface or serial data transfer. Using a parallel bus interface disables the key scan function. To prevent this, use a clock-synchronized serial interface.

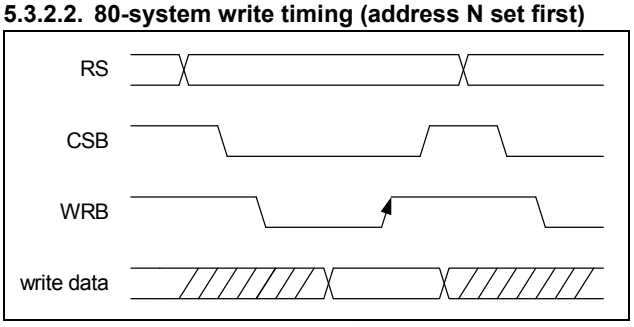
5.3.2. 4-bit interface

Setting the IM2/1/0 (interface mode) to the GND/VCC/VCC level allows E-clock-synchronized 4-bit parallel data transfer using pins DB7/KIN7-DB4/KIN4. Setting the IM2/1/0 (interface mode) to the VCC/VCC/VCC level allows 80-system 4-bit parallel data transfer. 8-bit instructions and RAM data are divided into upper/lower nibbles and the transfer starts from the upper nibble.

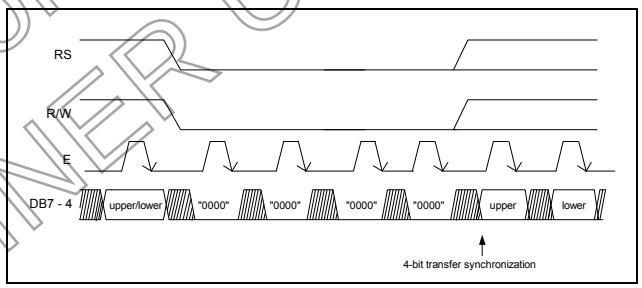
5.3.2.1. 68-system write timing (address N set first)



5.3.2.2. 80-system write timing (address N set first)



The SPLC701B supports the transfer synchronization function which resets the upper/lower counter to count upper/lower 4-bit data transfer in the 4-bit bus interface. Noise causing transfer mismatch between the upper and lower nibbles can be corrected by a reset triggered by consecutively writing a 0000 instruction four times. The next transfer starts from the upper nibble. Executing synchronization function periodically can recover any runaway in the display system.



4-bit Transfer Synchronization

5.4. Control Register

The SPLC701B contains five types of registers:

Name	Description
IR(Index Register)	Specify the index address of the register to be accessed.
SR(Status/ Scan Register)	Parallel: busy flag, LCD scan status Serial: key scan data
CR(Control Register)	Clear display Start oscillation Driver output control LCD drive waveform LCD drive control Power control Key scan cycle / IRQ enable / General Output Entry mode Cursor control Display control Scroll control Half-size font bank selection Half-size font attribute selection

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Name	Description
AR(Address Register)	Address for internal SRAM Auto up/down count when access
DR(Data Register)	Data register for internal SRAM WD: data written to WD is automatically written into internal SRAM RD: Data is read and temporarily latch in RD

Execution time for instructions (excluding display cleared) is zero clock cycle and instructions can be written consecutively. Data written into the WD from MPU is also automatically written into the DDRAM, CGRAM, or SGRAM. Data is read and temporarily latched in the RD while reading from the RAM. Also, the first read data is invalid and the second data is normal. After reading, data in the DDRAM, CGRAM, or SGRAM at the next address is sent to the RD for the next reading from the MPU.

5.5. Key Scan Registers (Scan0 to Scan3)

The key matrix scanner senses and holds the key states at each rising edge of the key strobe signals that are output by the SPLC701B. The key strobe signals are output as time-multiplexed signals from KST0 to KST3. After passing through the key matrix, these strobe signals are used to sample the key status on eight inputs from KIN0 to KIN7, enabling up to 32 keys to be scanned. The states of inputs, KIN0 to KIN7, are sampled by key strobe signal KST0 and latched into register, SCAN0.

Similarly, the data sampled by strobe signals, KST1 to KST3, is latched into registers, SCAN1 to SCAN3, respectively. **Software should read twice to forth time to determine a valid key, and the read cycle must be greater than key-scan cycle.**

5.6. General Output Ports (Port2 - 0)

The SPLC701B contains three general output ports. These ports are unable to drive currents, such as, for LED or back-light. An external transistor is a must for current boosting.

5.7. Address Counter (AC)

The Address Counter (AC) assigns addresses to the DDRAM, CGRAM, or SGRAM. When an address is written into RAM Address Register, the address information is sent to the AC. Selection of the DDRAM, CGRAM, and SGRAM is also determined concurrently by the RAM selected bit (RM1/0). After writing data into DDRAM, CGRAM, or SGRAM, the AC is automatically incremented by 1 (or decremented by 1). After reading the data, the AC is automatically updated or not updated by the RDM bit.

The cursor display position is determined by the address counter value.

1	2	3	4	5	6	7	8	9	10	11	12	Display position
00	01	02	03	04	05	06	07	08	09	0A	0B	DDRAM address

(AC = 02)

Note: The cursor/blink or black-white reversed control is also active when the address counter indicates the CGRAM or SGRAM.

5.8. Display Data RAM (DDRAM)

Display data RAM (DDRAM) stores display data represented in 8-bit character codes in the character display mode. Its capacity is 80 x 8 bits, or 80 characters, which is equivalent to an area of 10 characters x 4 lines. Any number of display lines (LCD drive duty ratio) from 1 to 4 can be selected by software. Here, assignment of DDRAM addresses is identical to all display modes. The displayed line at the top of the display (display-start-line) can also be selected through register's setting. The graphical display mode does not use data in the DDRAM.

5.9. Full-Size Character Generator ROM (FCGROM)

Full-size character generator ROM (FCGROM) generates 11 x 12-dot character patterns from 13-bit character codes. It is equipped with 8,128 full-size font patterns such as the JIS Level-1 and Level-2 Kanji Set or non-Kanji Set. The 11*12 font is displayed within 12*13 area.

5.10. Half-Size Character Generator ROM (HCGROM)

Half-size character generator ROM (HCGROM) generates 5 x 12-dot character patterns from 7-bit character codes. It is formed with two banks of 128 half-size font patterns and 256 half-size fonts in total. The 5*12 font is displayed within 6*13 area.

5.11. Booster (DC-DC Converter)

The booster doubles, triples, or quadruples a voltage input to the Vci pin. With this, both the internal logic units and LCD drivers can be controlled with a single power supply. Boost output level from single to quadruple boost can be programmed by software.

5.12. Cursor/Blink Controller

The cursor / blink (or black-white reversed) control is used to create a cursor or a flashing area on the display in a position corresponding to the location stored in the Address Counter (AC).

5.13. Character Generator RAM (CGRAM)

In text mode, character generator RAM (CGRAM) allows users to redefine the character patterns in the character display mode.

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Up to 40 character patterns of 12 x 13-dot characters can be simultaneously displayed. DDRAM-specified character code can be selected to display one of these users' font patterns.

In graphic or superimposed mode, the CGRAM serves as a RAM to store 120 x 52-dot bit pattern data in the graphical display mode. Display patterns are directly written into CGRAM. User font code set in DDRAM are illegal.

5.14. Segment RAM (SGRAM)

The segment RAM (SGRAM) enables control of segments such as icons and marks through the user program. Segments and characters are driven by a multiplexing driving method. The SGRAM has a capacity of 120 x 4 bits, and can control a display of up to 200 icon segments(40 grayscale segments and 160 mono-blinking segments). The segment icon are driven while COMS1 and COMS2 outputs are being selected. The 40 grayscale-controlled segments output the same display data in both the COMS1 and COMS2 modes. Bits in the SGRAM corresponding to segments to be displayed are set directly by the MPU regardless of the contents of the DDRAM and CGRAM.

5.15. Timing Generator

The timing generator generates timing signals for the operation of internal circuits (e.g. DDRAM, CGROM, CGRAM, and SGRAM). The RAM read timing for display and internal operating timing by MPU access are generated separately to avoid interfering to each other. This prevents flickering in areas other than the display area when writing data to DDRAM, for instance.

5.16. Contrast Adjuster

The contrast adjuster can be applied to adjust LCD contrast in 32 steps by varying the LCD driving voltage through software that can be used to select an appropriate LCD brightness or to compensate for temperature.

5.17. Oscillation Circuit (OSC)

The SPLC701B provides R-C oscillation with build-in register. The frame rate is about 75Hz.

The appropriate oscillation frequency for different display size can be obtained by adjusting NC[1:0]. ***Clock pulses can not be supplied externally***. Since R-C oscillation stops during the standby mode, current consumption can be reduced.

5.18. V-PIN Voltage Follower

A voltage follower for each voltage level (V1 to V5) reduces current consumption by the LCD driving power supply circuit. No external resistors are required because of the internal bleeder-resistor, which generates different levels of LCD driving voltage. This internal bleeder-resistor can be software-specified from 1/2 bias to 1/8 bias, according to the liquid crystal display driving duty. The voltage followers can be turned off when multiplexing driving is not used.

5.19. Liquid Crystal Display Driver Circuit

The liquid crystal display (LCD) driver circuit consists of 54 common signal drivers (COM52 - 1, COMS1, and COMS2) and 120 segment signal drivers (SEG120 - 1). When the number of lines are selected by a program, the required common signal drivers automatically output driving waveforms while the other common signal drivers continue to output unselected waveforms. Character pattern data is sent serially through a 120-bit shift register and latched when all necessary data arrive. The latched data then enables the segment signal drivers to generate driving waveform outputs. The shift direction of 120-bit data can be changed by the SGS bit. The shift direction for the common driver can also be alternated by the CMS bit through selecting an appropriate direction for the device mounting configuration. When multiplexing driving is not used, or during the standby or sleep mode, all the above common and segment signal drivers output the GND level, halting the display.

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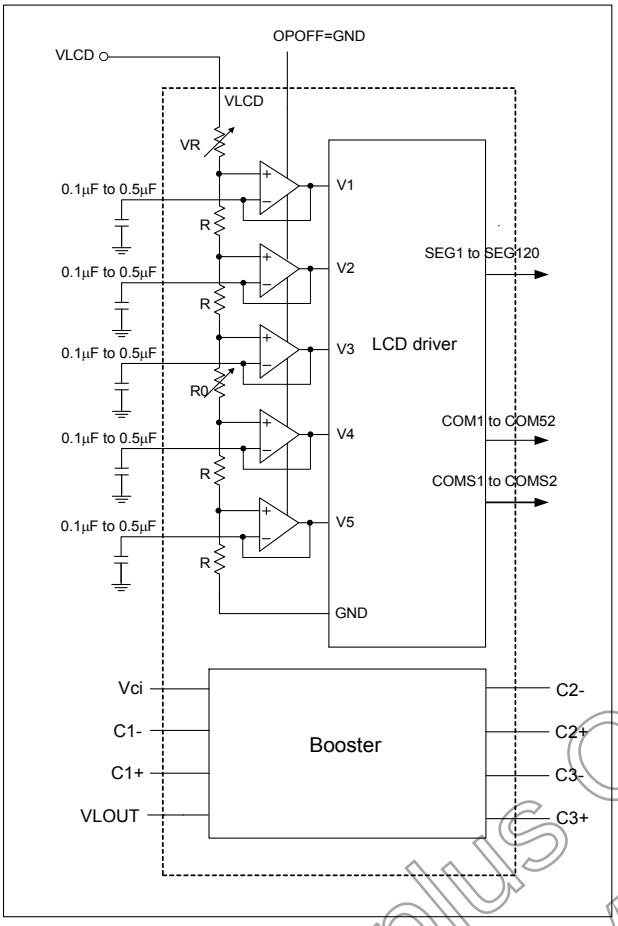
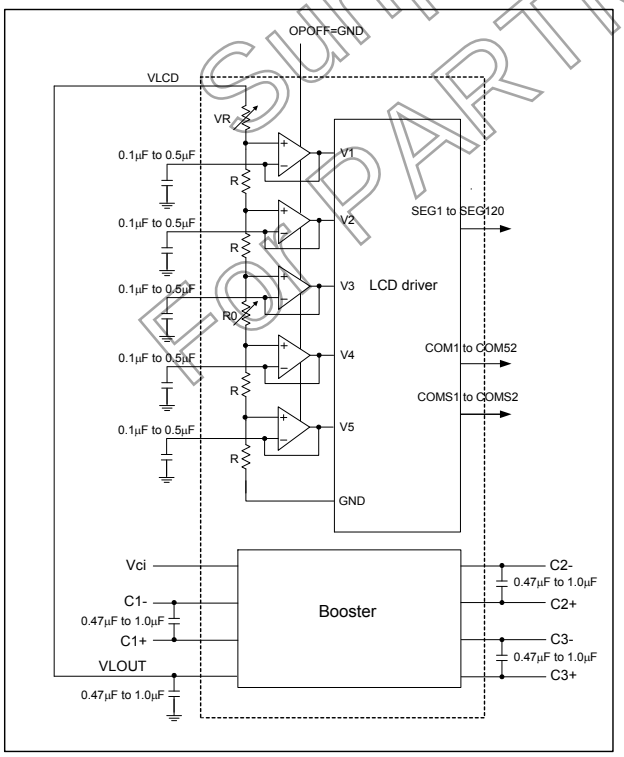


External Power Supply for LCD Driver Voltage Generation



Use Booster for LCD Driver Voltage Generation

6. INSTRUCTION DESCRIPTIONS

6.1. Registers

The SPLC701B consists of the following five types of registers:

1). Index Register (IR): Select control registers, RAM addresses, or data registers

2). Status Register (SR): Read the internal state or key scan data

3). Control Registers (R0 - RC): Set the display control or key scan control

4). RAM Address Registers (RD and RE): Select RAMs and set RAM addresses

5). RAM Data Register (RF): Receives the written and read data for the RAM

Normally, instructions that transfer display data are used the most. The mechanism of auto-increment by 1 (or auto-decrement by 1) of internal SPLC701B RAM addresses after each data write can reduce the **MPU program load.**

Because instructions other than the display cleared instruction are executed in 0 cycles, instructions can be written in succession. While the display cleared instruction is being executed for internal operation or during reset, no instruction other than the SR read instruction can be executed.

Register Selection by RS and R/W Bits

RS	RW	Description
0	0	Write to the Index Register (IR)
0	1	Parallel: Read the Status Register; Serial: Key Scan Data Register(SR)
1	0	Write to the control registers: RAM Address Register, and RAM-Write-Data-Register(WD)
1	1	Read the RAM-Read-Data-Register(RD)

Note1: Key scan interface is available for serial interface only.

Note2: In bus mode, RS and RW are pin input; in serial mode, RS and RW are embedded in the start byte.

Note3: Every time you want to access R15-0, make sure IR is correctly point to it.

There are four 8-bits registers, SCAN0, SCAN1, SCAN2, SCAN3. These registers strobe external key data bus on rising edge of KST0, KST1, KST2, KST3, respectively. And only available at serial interface mode.

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6.2. Instruction Table

Register	RW	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
IR (index)	0	0	0	0	0	0	ID3	ID2	ID1	ID0	ID: index
SR (status)	1 read	0	BF	NF1	NF0	0	LF3	LF2	LF1	LF0	BF: busy flag NF: display line position LF: display row position
	1 read	0	KSD7	KSD6	KSD5	KSD4	KSD3	KSD2	KSD1	KSD0	KSD: key scan data
R0 (clear display)	0	1	0	0	0	0	0	0	0	1	Clear display (85 clock cycle)
R1 (start oscillation)	0	1	0	0	0	0	0	0	0	1	DB0: Start oscillation
R2 (driver output control)	0	1	0	NL2	NL1	NL0	0	CEN	CMS	SGS	NL: number of display lines CEN: centering CMS: common shift direction SGS: segment shift direction
R3 (drive waveform)	0	1	B/C	EOR	0	NW4	NW3	NW2	NW1	NW0	B/C: choose C type waveform EOR: EOR with frame NW: number of raster-row
R4 (drive control)	0	1	BS2	BS1	BS0	CT4	CT3	CT2	CT1	CT0	BS: bias selection CT: contrast selection
R5 (power control)	0	1	AMP	0	BT1	BT0	0	0	SLP	STB	AMP: turn on booster and OP BT: booster ratio SLP: sleep STB: standby
R6 (key scan control)	0	1	0	PT2	PT1	PT0	KSB	IRE	KF1	KF0	PT: general output port KSB: key standby IRE: interrupt enable KF: key scan frequency
R7 (entry mode)	0	1	0	0	0	REV	SPR	GR	RDM	I/D	REV: screen reversal SPR: superimposed mode GR: graphic mode RDM: read/modify/write inst. I/D: increment/decrement
R8 (cursor control)	0	1	0	0	0	CH	LC	BW	C	B	CH: cursor home LC: line cursor BW: black-white reversed blinking C: 13th raster-row cursor B: black blinking
R9 (display control)	0	1	0	0	DC	DS	0	0	NC1	NC0	DC: main display on DS: icon display on NC: number of display character
RA (scroll control)	0	1	0	0	SN1	SN0	SL3	SL2	SL1	SL0	SN: display start line SL: display start raster-row
RB (half-size ROM select)	0	1	0	0	0	0	RL4	RL3	RL2	RL1	Set the half-size font bank of every line
RC (half-size display attribute)	0	1	A41	A40	A31	A30	A21	A20	A11	A10	Set the half-size font attribute of every line

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Register	RW	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
RD (upper RAM address set)	0	1	RM1	RM0	0	0	0	AD10	AD9	AD8	RM: RAM select AD: RAM address
RE (lower RAM address set)	0	1	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	AD: RAM address
RF (RAM data, write)	0	1	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0	Data write to DD/CG/SG RAM
RF (RAM data, read)	1 read	1	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	Data read from DD/CG/SG RAM

6.3. Index Register (IR)

RW	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	ID3	ID2	ID1	ID0

The Index Register designates control registers (R0 to RC), RAM address registers (RD and RE), and RAM data register (RF). The register index value must be set between addresses 00000000_2 to 00001111_2. **Every time you want to access R15 - 0, make sure IR is correctly point to it.**

6.4. Status/Scan Register (SR)

RW	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	BF	NF1	NF0	0	LF3	LF2	LF1	LF0
1	0	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0

In the parallel interface, the Status Register reads the busy flag (BF), LCD-driven display lines (NF1/0), and display raster-rows (LF3 - 0). In the serial interface, the SR reads the key scan data in key scan registers, SCAN0 to SCAN3. After the start byte has been transferred, the SR starts reading from SCAN0, SCAN1, SCAN2, and SCAN3 in sequence. After SCAN3 has been read, SCAN0 is re-read again.

NF1	NF0	Display Line Position
0	0	Displaying the 1st line
0	1	Displaying the 2nd line
1	0	Displaying the 3rd line
1	1	Displaying the 4th line

LF3	LF2	LF1	LF0	Display Line Position
0	0	0	0	Displaying the 1st raster-row
0	0	0	1	Displaying the 2nd raster-row
0	0	1	0	Displaying the 3rd raster-row
0	0	1	1	Displaying the 4th raster-row
•	•	•	•	•
1	0	1	1	Displaying the 12th raster-row
1	1	0	0	Displaying the 13th raster-row

6.5. Clear Display (R0)

RW	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	0	0	0	0	0	1

The display cleared instruction writes half-size space code A0H (half-size HCROM for character code A0H is a blank pattern) into all DDRAM addresses. It then sets DDRAM address 0 into the address counter (AC). It also sets I/D to 1 (increment mode) in the entry mode. Since the execution time of this instruction needs 85 clock cycles, do not transfer the next instruction during this period.

6.6. Start Oscillation (R1)

RW	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	0	0	0	0	0	1

The start oscillation instruction restarts the oscillator from the halt state in the standby mode. After issuing this instruction, wait at least 10 ms for oscillation to stabilize before issuing the next instruction.

6.7. Driver Output Control (R2)

RW	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	NL2	NL1	NL0	0	CEN	CMS	SGS

NL2 - 0: Specify the display lines. Display lines change the liquid crystal display driving duty ratio. DDRAM address mapping does not depend on the number of display lines.

CEN: Center the screen for artistic display. It is simply switches the scan order from (COMS1, COM1, COM2, COM3,.., COMS2) to (COMS1, COM14, COM15,..., COMS2) in sequence.

CMS: Reverse the output shift direction of a common driver.

SGS: Reverse the output shift direction of a segment driver.

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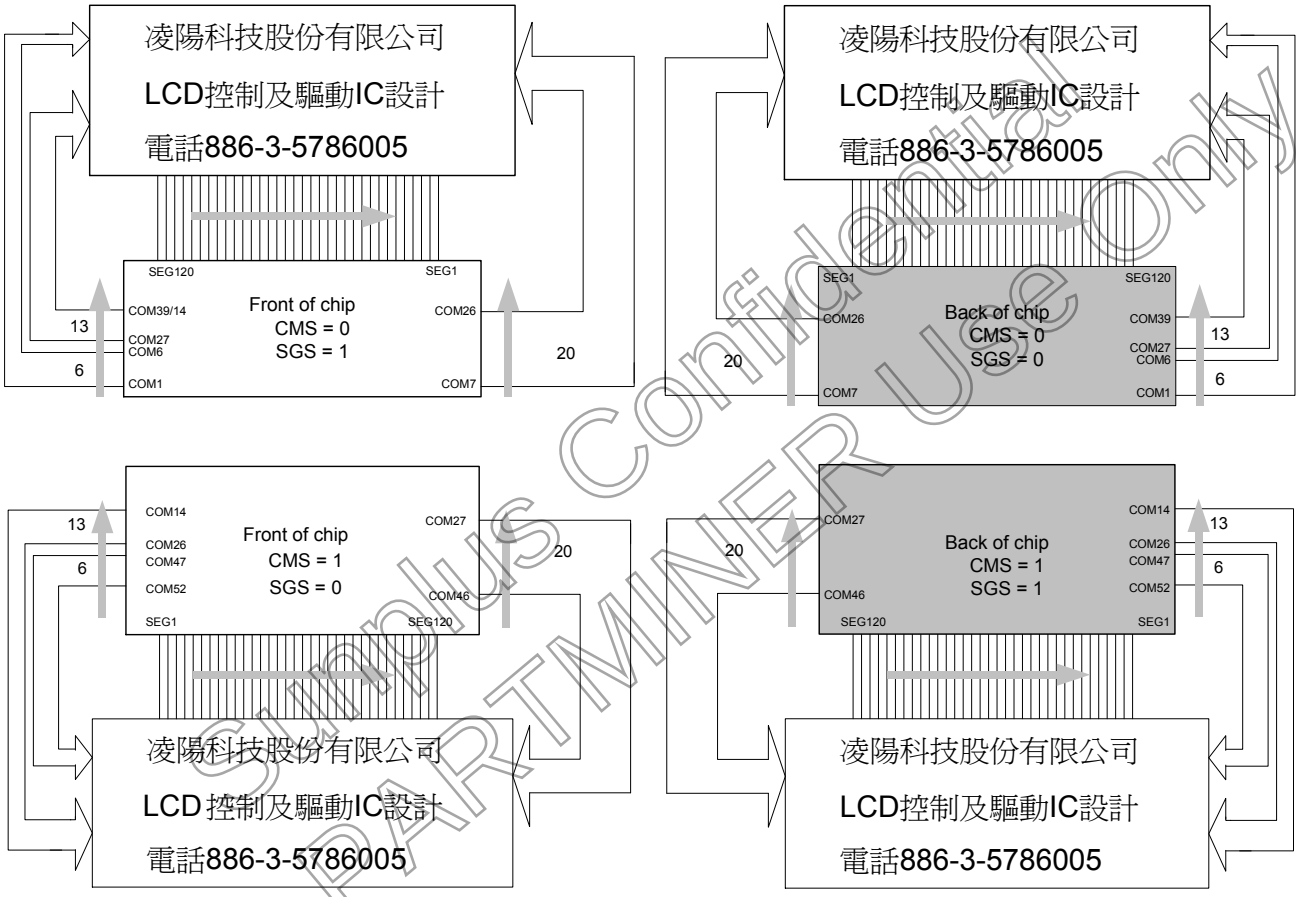
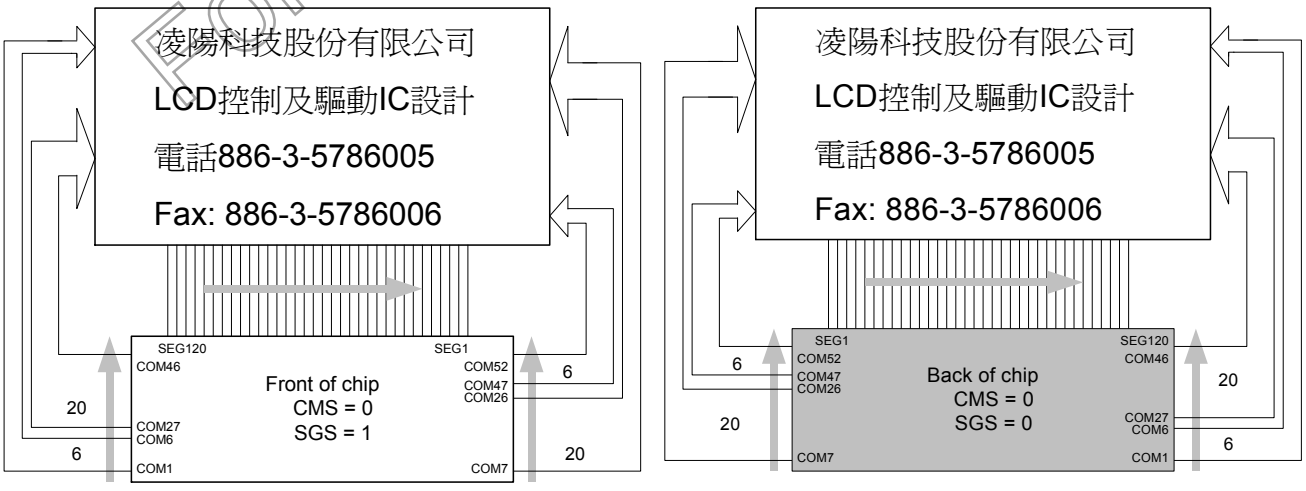
NL2	NL1	NL0	Display Lines	LCD Drive Duty Ratio	Common Driver Used
0	0	0	Only Segment(Icon)	1/2 Duty	COMS1, COMS2
0	0	1	Segment+1 line	1/15 Duty	COM13 - 1, COMS1, COMS2
0	1	0	Segment+2 lines	1/28 Duty	COM26 - 1, COMS1, COMS2
0	1	1	Segment+3 lines	1/41 Duty	COM39 - 1, COMS1, COMS2
1	0	0	Segment+4 lines	1/54 Duty	COM52 - 1, COMS1, COMS2



3-line Display Pattern Wiring



4-line Display Pattern Wiring

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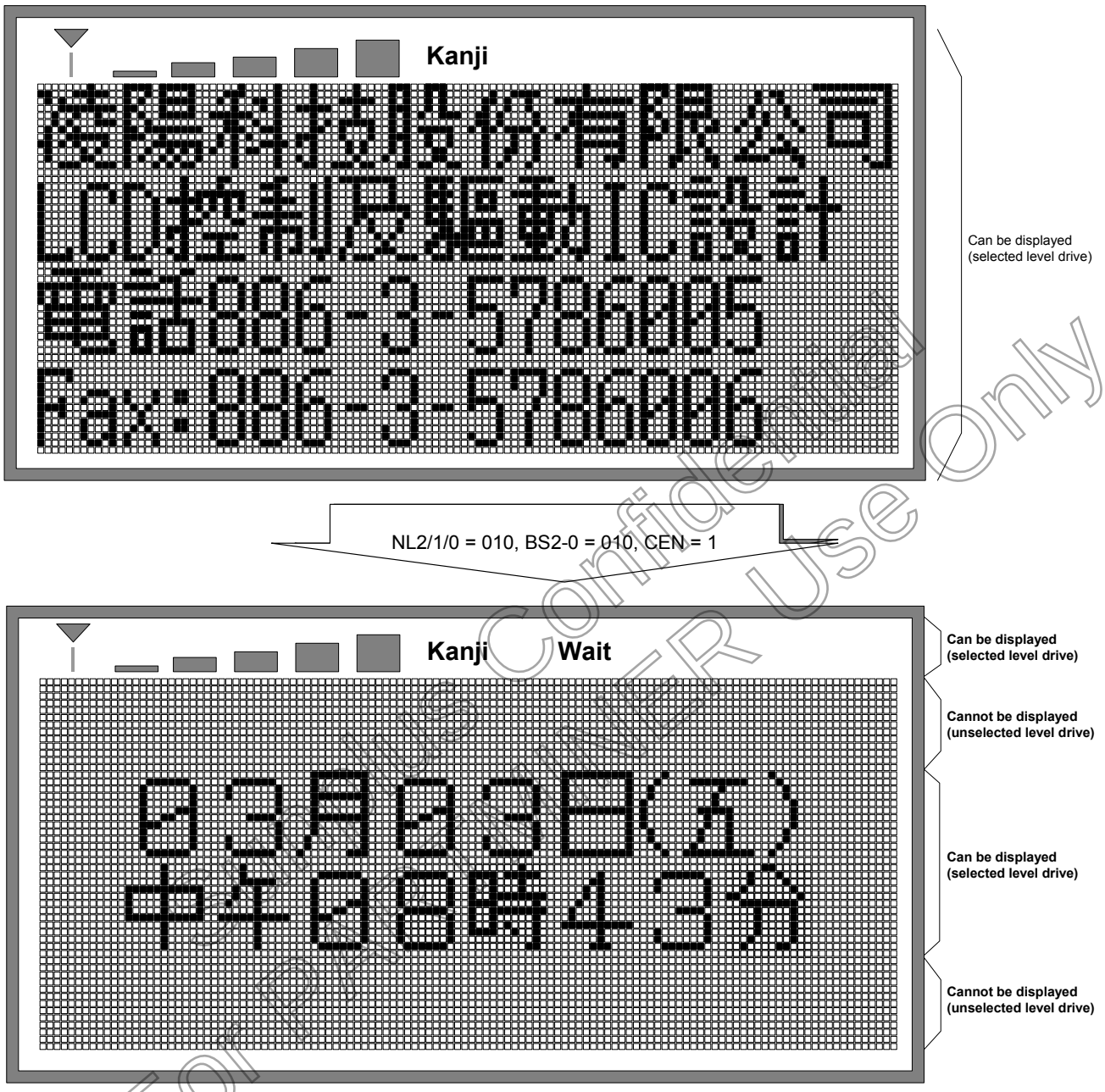

Partial-on Display (Date and Time Indicated)

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6.8. LCD Driving Wave (R3)

RW	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	B/C	EOR	0	NW4	NW3	NW2	NW1	NW0

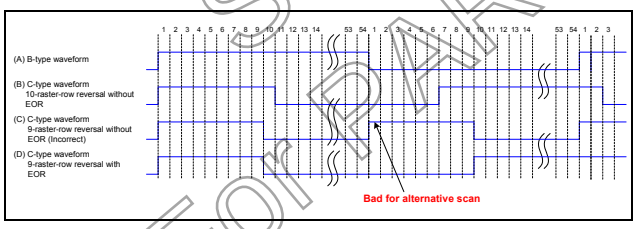
B/C: Specifies the LCD alternating method. When B/C = '0', a B-pattern waveform is generated and alternates in every frame. When B/C = '1', a C-pattern waveform is generated and alternates (n-raster-row reversed AC drive) in every NW[4:0]+1 raster-row.

EOR: When the C-pattern waveform is set and EOR = '1', the odd/even frame-select signals and the n-raster-row reversed signals are EORed for alternating drive. EOR is used when the LCD is not alternated by combining the set values of the LCD driving duty ratio and n raster-row.

NW4 - 0: Specify the number of raster-rows n that will alternate at the C-pattern waveform setting. NW4 - 0 alternate in every n + 1 raster-row, and the one to the 32 raster-rows can be selected.

The SPLC701B supports not only the LCD reversed AC drive in a one-frame unit (B-pattern waveform) but also the n-raster-row reversed AC drive which alternates in an n-raster-row unit from one to 32 raster-rows (C-pattern waveform). When a problem affecting display quality occurs, such as crosstalk at high-duty driving of more than three lines (1/42 duty), the n-raster-row reversed AC drive (C-pattern waveform) can improve the quality.

Determine the number of raster-rows n for alternating after confirmation of the display quality with the actual LCD panel. However, if the number of AC raster-rows is reduced, the LCD alternating frequency becomes high. Because of this, the charge or discharge current is increased in the LCD cells.



Example of an AC signal under n-raster-row Reversed AC Drive

Note: The C-type waveform 9-rater-row reversal without EOR may produce incorrect scan because 54 commons are completely divided by 9-raster-row with even number of 6. It will cause offset DC voltage on LCD panel. As a result, if C-type waveform 9-rater-row is selected, the EOR signal in LCD DRIVING WAVE must be enabled (set to 1). However, if 6-rater-row reversal is selected, 54 commons are completely divided by 6-raster-row with odd number of 9. The EOR signal in LCD DRIVING WAVE must be disabled (set to 0).

6.9. LCD Driving Control (R4)

RW	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BS2	BS1	BS0	CT4	CT3	CT2	CT1	CT0

BS2 - 0: Set the LCD driving bias values in the range of 1/2 to 1/8 bias. The LCD driving bias value can be selected according to the LCD driving duty and LCD driving voltage.

CT4 - 0: Control the LCD driving voltage (potential difference between V1 and GND) to adjust contrast. A 32-step adjustment is possible.

BS2	BS1	BS0	LCD Drive Bias
0	0	0	1/8 bias drive
0	0	1	1/7 bias drive
0	1	0	1/6 bias drive
0	1	1	1/5.5 bias drive
1	0	0	1/5 bias drive
1	0	1	1/4.5 bias drive
1	1	0	1/4 bias drive
1	1	1	1/2 bias drive

CT4	CT3	CT2	CT1	CT0	Variable Register (VR)	Potential Difference between V1 and GND	Display Color
0	0	0	0	0	3.2R	(Small)	(Light)
0	0	0	0	1	3.1R		
0	0	0	1	0	3.0R		
0	0	0	1	1	2.9R		
0	0	1	0	0	2.8R		
0	0	1	0	1	2.7R		
0	0	1	1	0	2.6R		
:	:	:	:	:	:		
1	1	1	0	1	0.3R		
1	1	1	1	0	0.2R		
1	1	1	1	1	0.1R	(Large)	(Deep)

6.10. Contrast Adjuster

Software can adjust contrast for an LCD by varying the liquid-crystal drive voltage (potential difference between VLCD and V1) through the CT bits of the contrast adjustment register (electron volume function). The value of a variable resistor (VR) can be adjusted within a range from 0.1 x R through 3.2 x R, where R is a reference resistance. The SPLC701B incorporates a voltage-follower operational amplifier for each of V1 to V5 to reduce current flowing through the internal bleeder resistors, which generate different liquid-crystal drive voltages.

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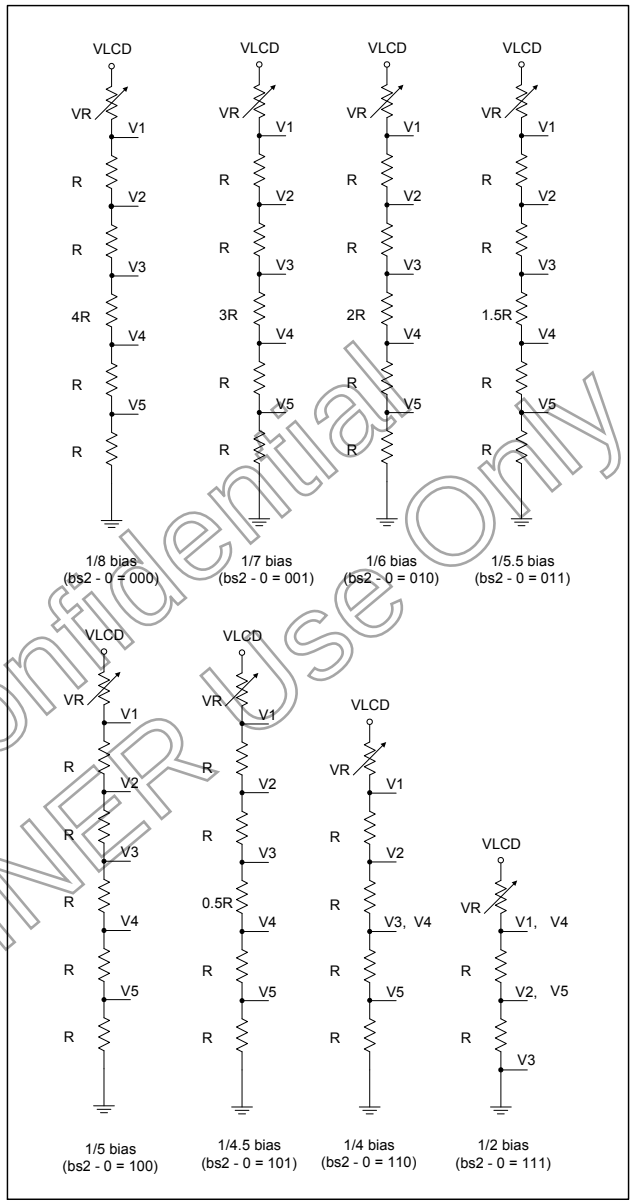
6.11. LCD Drive Bias Selector

An optimum liquid crystal display bias value can be selected using BS2 - 0 bits, according to the liquid crystal drive duty ratio setting (NL2 - 0 bits). Liquid crystal display drive duty ratio and bias value can be displayed while switching software applications to match the LCD panel display status. The optimum bias value calculated using the following expression is an ideal value where the optimum contrast is obtained. Driving by using a lower value than the optimum bias value provides lower contrast and lower liquid crystal display voltage (potential difference between V1 and GND). When the liquid crystal display voltage is insufficient even if a quadruple booster is used or output voltage is lowered because the battery life has been reached, the display can be made easier to see by lowering the liquid crystal bias. The liquid crystal display can be adjusted by using the contrast adjustment register (CT4 - 0 bits) and selecting the booster output level (BT1/0 bits).

Optimum bias value for 1/N duty ratio drive voltage = $\frac{1}{\sqrt{N+1}}$

Optimum Drive Bias Values:

LCD drive duty ratio (NL2-0)	1/54 duty NL2-0 = 100	1/41 duty NL2-0 = 011	1/28 duty NL2-0 = 010	1/15 duty NL2-0 = 001	1/2 duty NL2-0 = 000
Optimum drive bias value (BS2-0)	1/8 bias BS2-0 = 000	1/7 bias BS2-0 = 001	1/6 bias BS2-0 = 010	1/4.5 bias BS2-0 = 101	1/2 bias BS2-0 = 111



LCD Driver Bias Circuit

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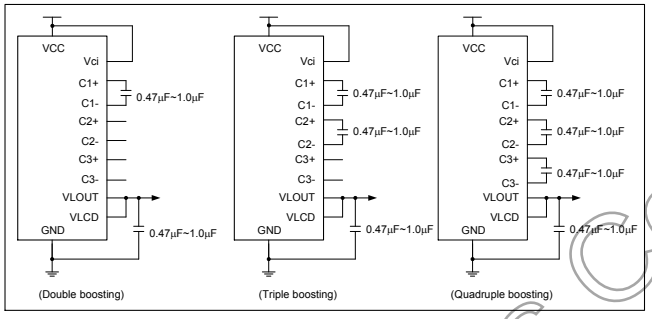
6.12. Power Control (R5)

RW	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	AMP	0	BT1	BT0	0	0	SLP	STB

AMP: When AMP = '1', each voltage follower for V1 to V5 pins and the booster are turned on. When AMP = '0', current consumption can be reduced while the display is not being used.

BT1 - 0: Switch the output of V5 between single, double, triple, and quadruple boost. The LCD drive voltage level can be selected according to its driving duty ratio and bias. A lower amplification of the booster consumes less current. When BT1/0 = "00", a single boost is output. When BT1/0 = "01", a double boost is output. When BT1/0 = "10", a triple boost is output. When BT1/0 = "11", a quadruple boost is output.



Booster Application Circuit

SLP: When SLP = '1', the SPLC701B enters the sleep mode where the internal operations are halted except for the key scan function and the R-C oscillator, thus reducing current consumption. Only the following instructions can be executed during the sleep mode.

1). Key scan data read
2). Key scan control (IRE, KF1/0 bit)
3). Power control (AMP, SLP, and STB bits)
4). Port control (PT2 - 0 bits)

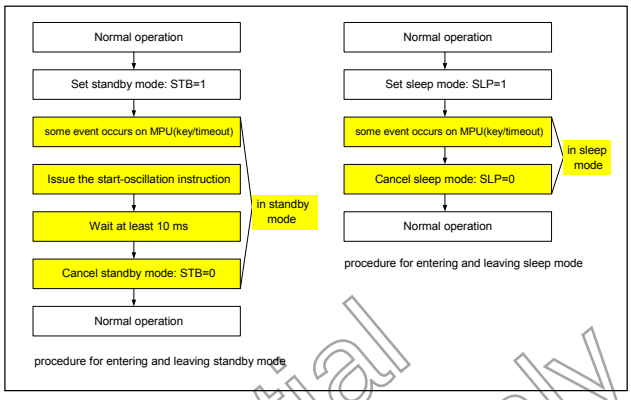
During the sleep mode, the other RAM data and instructions cannot be updated therefore they are retained.

STB: When STB = '1', the SPLC701B enters the standby mode, where display operation and key scan completely stops, halting all the internal operations including the internal R-C oscillator. Further, no external clock pulses are supplied.

This setting can be used as the system wake-up because an interrupt is generated when a specific key is pressed. Only the following instructions can be executed during the standby mode.

1.Standby mode cancel (STB = '0')
2.Voltage follower circuit on/off (AMP = 1/0)
3.Start oscillation
4.Key scan interrupt generation enabled/disabled (IRE = 1/0)
5.Port control (PT2 - 0 bits)

During the standby mode, the other RAM data and instructions may be lost. To prevent this, they must be set again after the standby mode is **canceled.**



6.13. Key Scan Control (R6)

RW	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	PT2	PT1	PT0	KSB	IRE	KF1	KF0

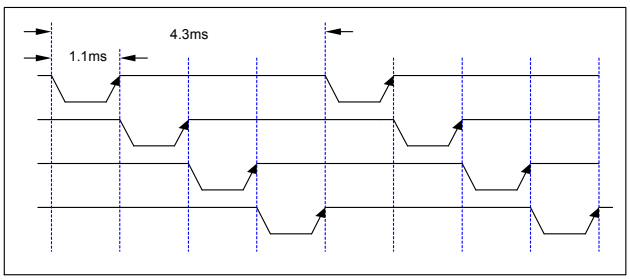
PT2 - 0: Control the output level of a port output pin (PORT2 - 0). When PT0 = 0, the PORT0 pin outputs the GND level, and when PT0 = 1, it outputs the VCC level. Similarly, PT1 and PT2 bits control PORT1 and PORT2 output levels respectively.

KSB: When KSB = '1', the mode enters key standby and the key scan is stopped. In this case, key scan interrupts can be generated as well as in the standby mode. When KSB = '0', the keys are scanned normally.

IRE: When IRE = '1', it permits interrupts when a key is pressed. This causes interrupts to occur in the standby period when the oscillator clock is halted, as well as key scan interrupts during normal operation, allowing system wake-up.

KF1 - 0: Set the key scan cycle. The following table shows the key scan pulse width and key scan cycle used when the oscillation frequency (fosc) is 60KHz, which depend on the oscillation frequency.

KF1	KF0	Key Scan Pulse Width	Key Scan Cycle
0	0	0.25ms	1.1ms(64 clock cycle)
0	1	0.5ms	2.1ms(128 clock cycle)
1	0	1.1ms	4.3ms(256 clock cycle)
1	1	2.1ms	8.5ms(512 clock cycle)



Key Strobe Output Timing (KF1/0 = 10, fosc = 60KHz)

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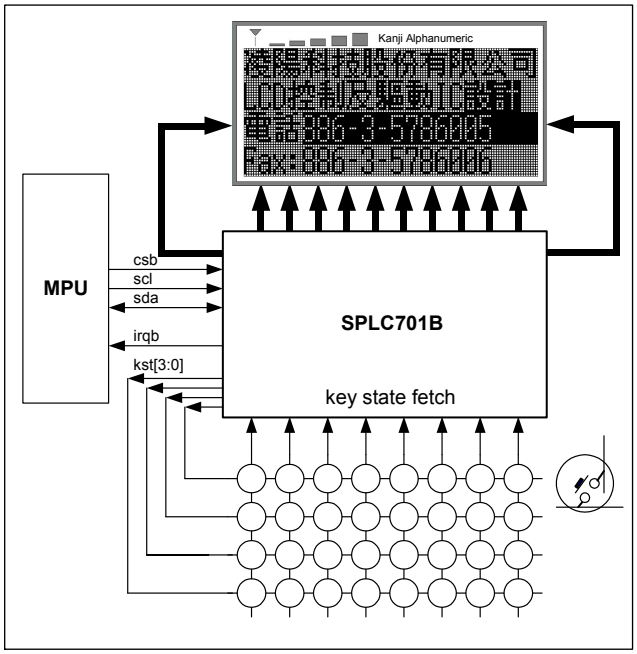
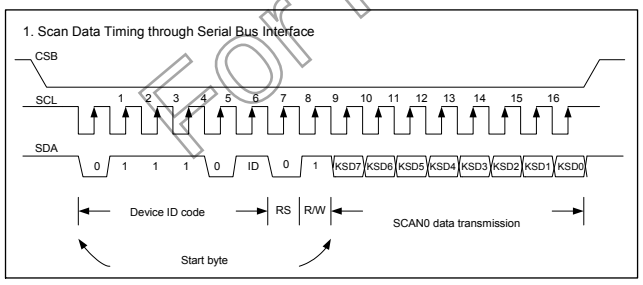
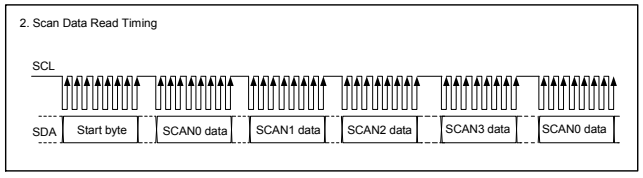


The key matrix scanner senses and holds the key states at each rising edge of the key strobe signals that are output by the SPLC701B. The key strobe signals are output as time-multiplexed signals from KST0 to KST3. After passing through the key matrix, these strobe signals are used to sample the key status on eight inputs from KIN0 to KIN7, enabling up to 32 keys to be scanned. The states of inputs, KIN0 to KIN7, are sampled by key strobe signal KST0 and latched into register, SCAN0. Similarly, the data sampled by strobe signals, KST1 to KST3, is latched into registers, SCAN1 to SCAN3, respectively. Key pressing is stored as 1 in these registers. **Software should read twice to forth time to determine a valid key, and the read cycle must be greater than key-scan cycle.**





Up to three keys can be pressed simultaneously. Note, however, that if the third key is pressed on the intersection between the rows and columns of the first two keys pressed, incorrect data will be sampled. For three-key input, the third key must be on a separate column or row.

Additionally, the SPLC701B supports the key standby mode in which only the key scan circuit enters the standby state. When 1 is set to the key standby mode setting bit (KSB), only key scanning is stopped. In this case, as well as in the normal standby mode, the key wake-up interrupt function can be used. For example, this function is used when only key scanning is stopped to improve the sensitivity of the wave received by a radio system during calling.

If the interrupt enable bit (IRE) is set to 1, the SPLC701B sends an interrupt signal to the MPU on detecting that a key has been pressed in the key scan circuit by setting the IRQB output pin to a low level. An interrupt signal can be generated by pressing any key in a 32-key matrix. The interrupt level continues to be output during the key scan cycle while the key is being pressed.

Normal key scanning is performed and interrupts can occur in the SPLC701B sleep mode (SLP = 1). Accordingly, power consumption can be minimized in the sleep mode, by triggering the MPU to read key states via the interrupt which is generated only when the SPLC701B detects a key input.

On the other hand, normal key scanning stops in the standby mode (STB = 1) or in the key standby mode (KSB = 1). During this period, the KST0 output is kept low, so the SPLC701B can always monitor eight key inputs (KIN7 - 0) connected to KST0 when RS = GND. Therefore, if any of the eight keys is pressed, an interrupt occurs. When RS = VCC, all outputs KST0 to KST3 are kept low, so the SPLC701B can always monitor 32 key inputs. If any of the 32 keys is pressed, an interrupt occurs. Accordingly, power consumption or noise generation can be further minimized in the standby mode, where the whole system is inactive, by triggering the MPU via the interrupt which is generated only when the SPLC701B detects a key input from the above keys.

Interrupts may occur if noise occurs in KIN7 - 0 input during key scanning. Interrupts must be inhibited if not needed by setting the interrupt enable bit (IRE) to 0.

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6.14. Entry Mode (R7)

RW	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	0	REV	SPR	GR	RDM	I/D

REV: When REV = '1', the REV displays all characters and graphics display sections except for the segment display section with black-white reversal.

SPR: When SPR = '1', the SPR displays combined character and graphics display screens (the super-imposed display mode). **In this case, user fonts using the CGRAM in the character display mode** cannot **be displayed. The priority of SPR is higher than GR.**

GR: Activates the character mode when GR = '0'. Displays the font pattern on the CGROM or CGRAM according to the character code written in the DDRAM. It activates the graphics mode when GR = '1'. It displays a given pattern according to the bit map data written in the CGRAM. In this case, data in the DDRAM is not used for display. Segment pattern display set to the SGRAM is enabled both in the character mode and graphics mode.

RDM: When RDM = '0', the RDM increments or decrements the address counter value according to the I/D bit setting after reading the data from the DDRAM/CGRAM/SGRAM. When RDM = '1', the address counter is not updated after the data has been read from the RAM. The address counter is used when the RAM data is read, modified, and written. Since the first read data is invalid, the read must be done twice. After writing to the RAM, the address counter value must be incremented or decremented.

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DDRAM address by 1 when a character code is written into or read from DDRAM. The cursor or blinking moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to the writing and reading of CGRAM and SGRAM.

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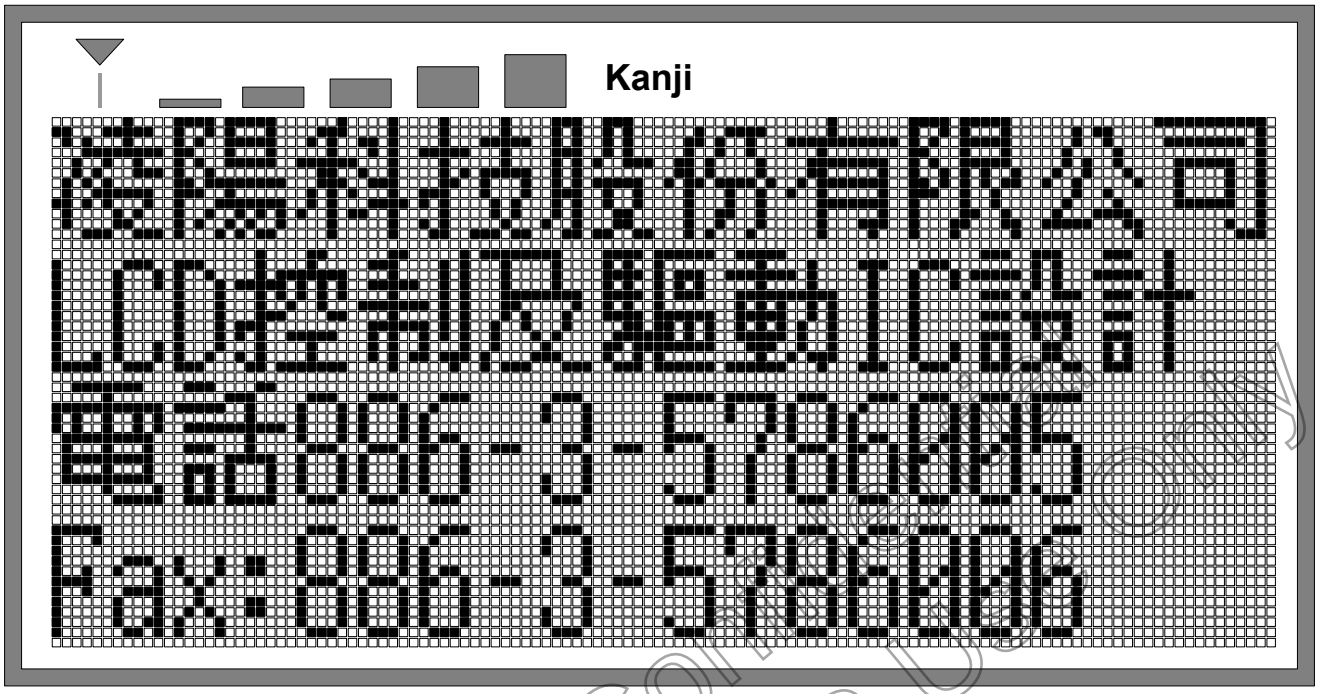
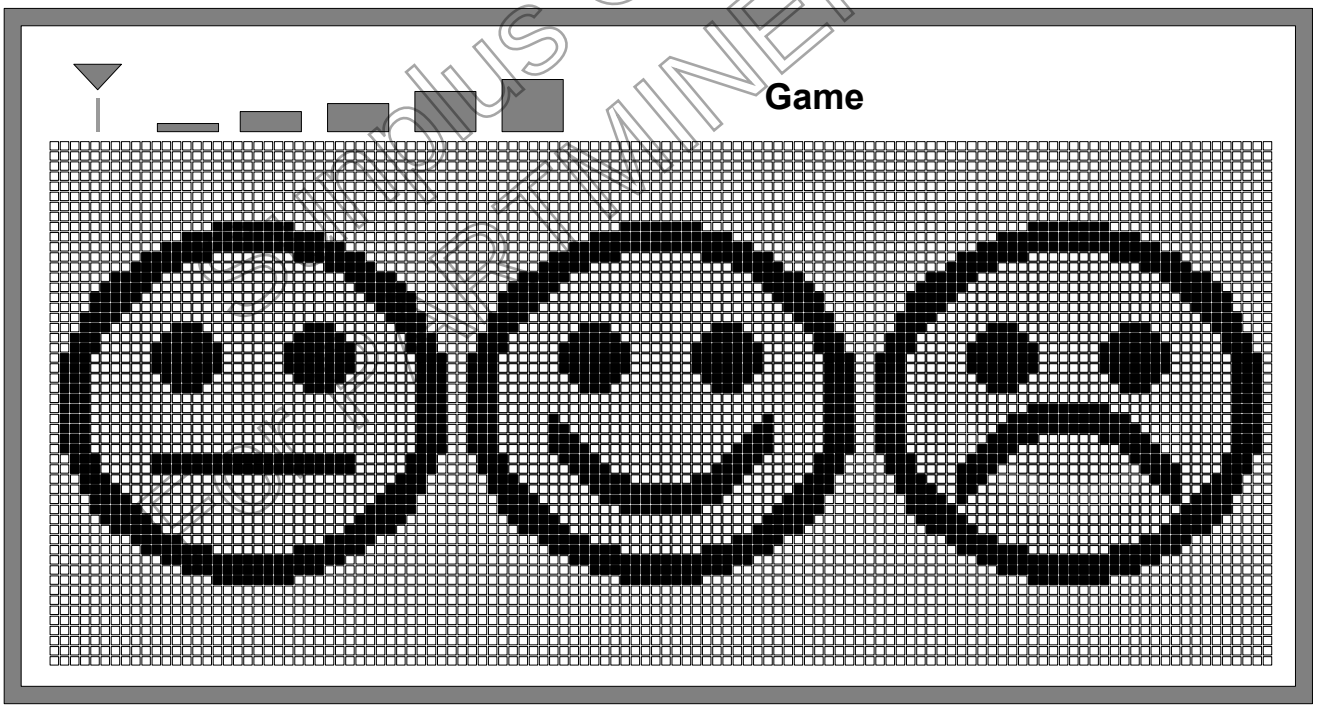


Example of Chinese in the Character Display Mode (GR = 0)



Example of Graphics Display in the Graphics Display Mode (GR = 1)

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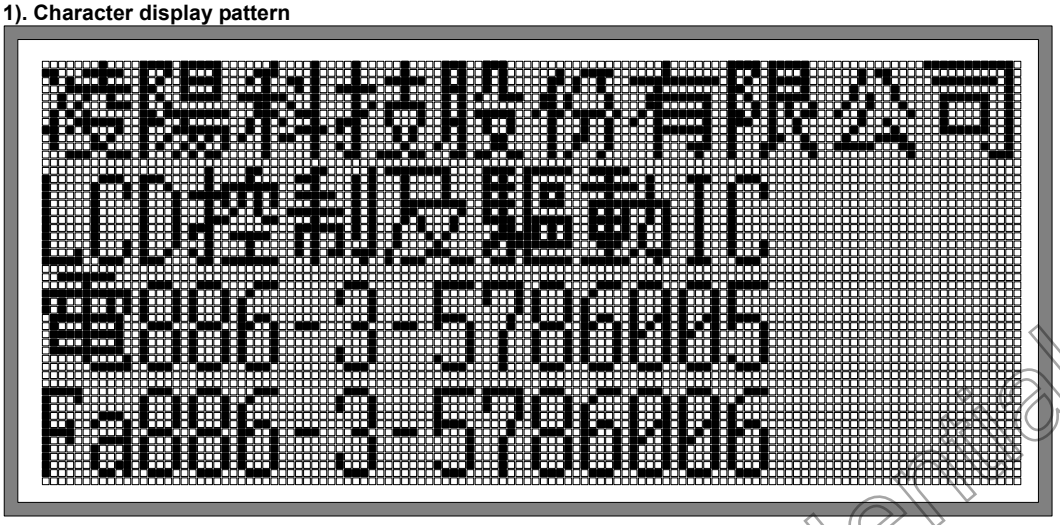
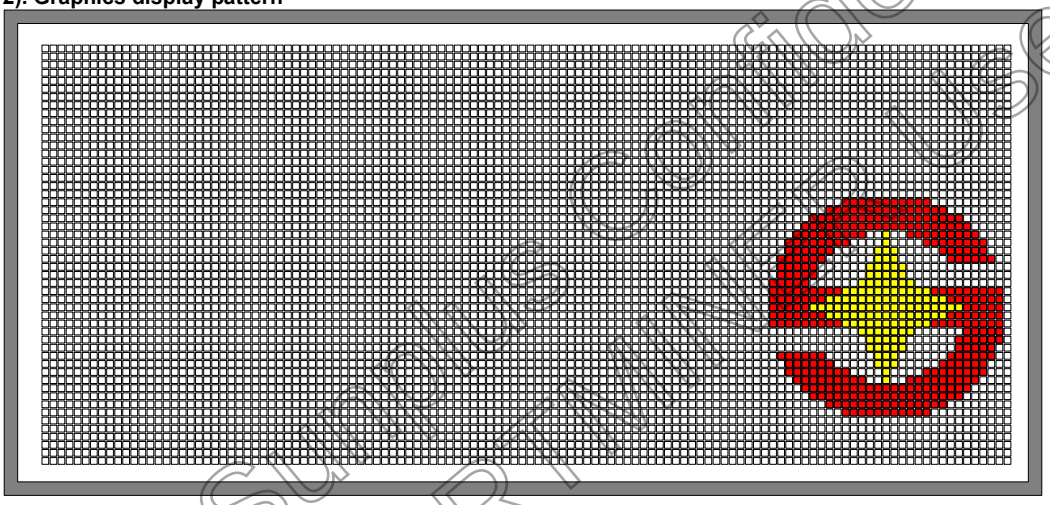
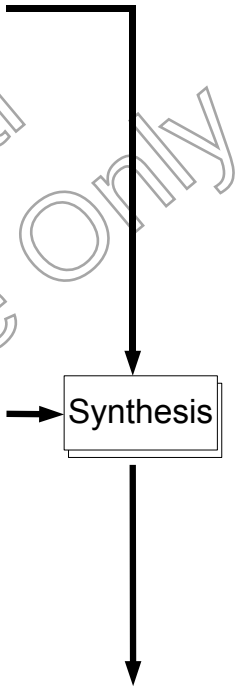
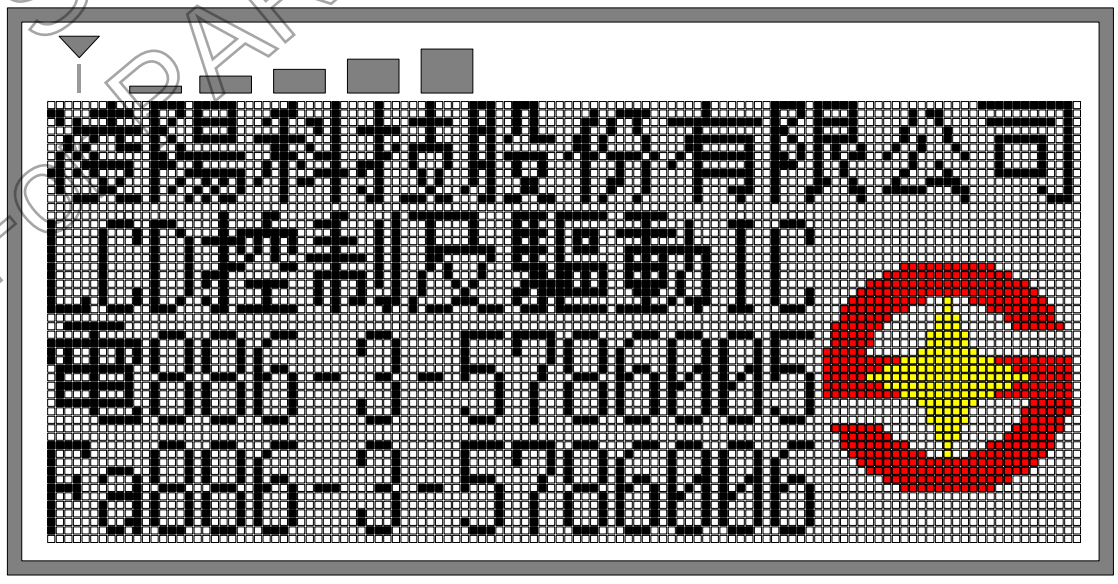
1). Character display pattern



2). Graphics display pattern







Example of Super-imposed Display (SPR=1)

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6.15. Cursor Control (R8)

RW	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	0	CH	LC	BW	C	B

CH: Executes the cursor home instruction and sets DDRAM address 0 into the Address Counter (AC). The contents in DDRAM are not changed. The cursor or blinking goes to the top left of the display.

LC: When LC = '1', a cursor attribute is assigned to the line that contains the Address Counter (AC) value. Cursor mode can be selected with the B/W, C, and B bits.

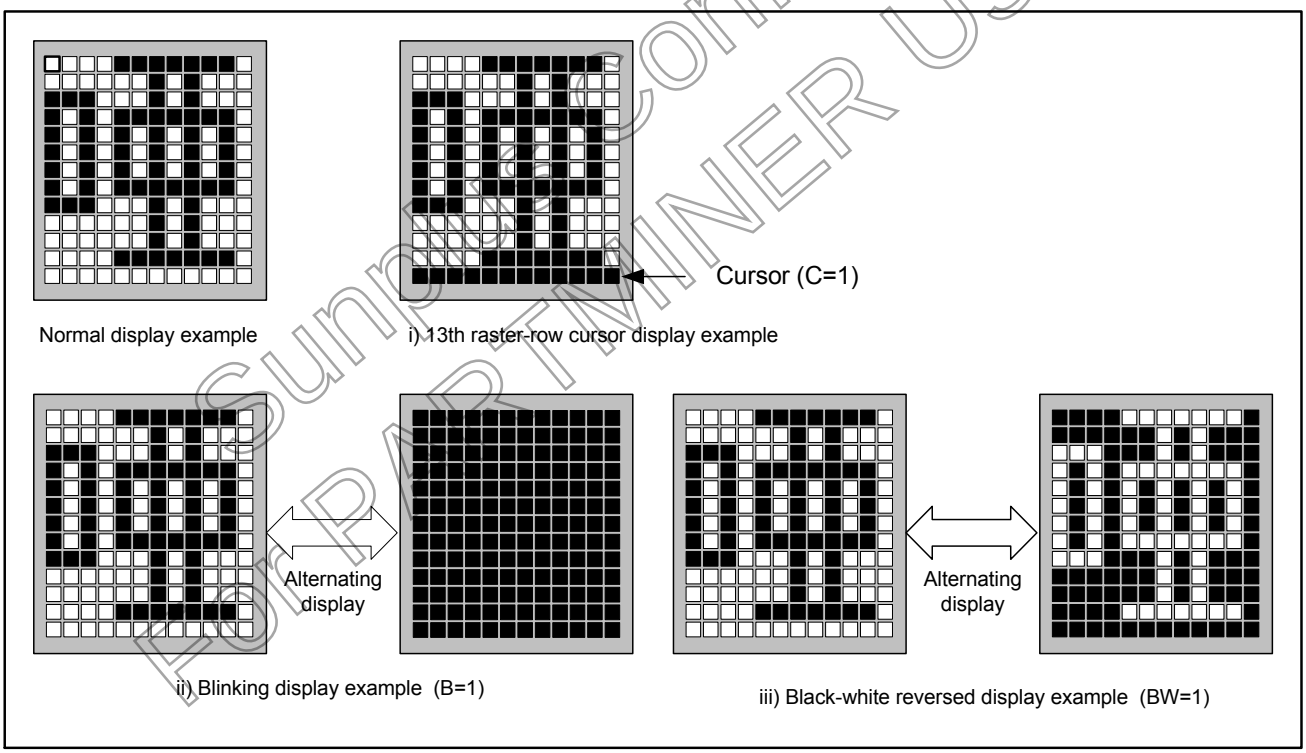
Address counter value and line cursor

Address counter value(AC)	Selected line for line cursor
00_{16} to 13_{16}	Select 1st line
20_{16} to 33_{16}	Select 2nd line
40_{16} to 53_{16}	Select 3rd line
60_{16} to 73_{16}	Select 4th line

B/W: When B/W = '1' and LC = '0', the character at the cursor position is cyclically (every 32 frames) blink-displayed with black-white reversal. When B/W = '1' and LC = '1', all characters including the cursor on the display line appear with black-white reversal. The characters do not blink.

C: The cursor is displayed on the 13th raster-row when C = '1'. The 13-dot cursor is ORed with the character pattern and displayed on the 13th raster-row.

B: The character indicated by the cursor blinks when LC = '0' and B = '1'. The blinking is displayed as switching between all black dots and displayed characters every 32 frames. The cursor and blinking can be set to display simultaneously. When LC = '1', setting B = '1' alternately displays all white dots and character pattern in a line unit. White-dots mean unlit dots, and black-dots mean lit dots.



Character-Cursor control example

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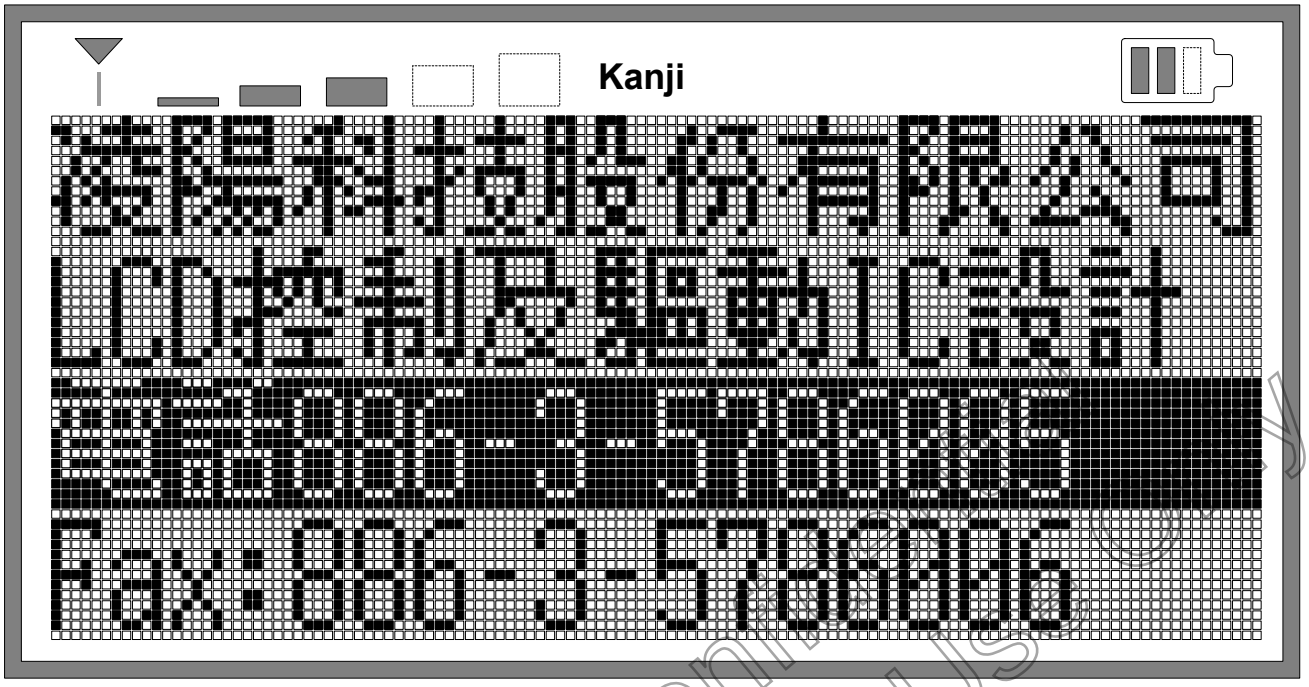
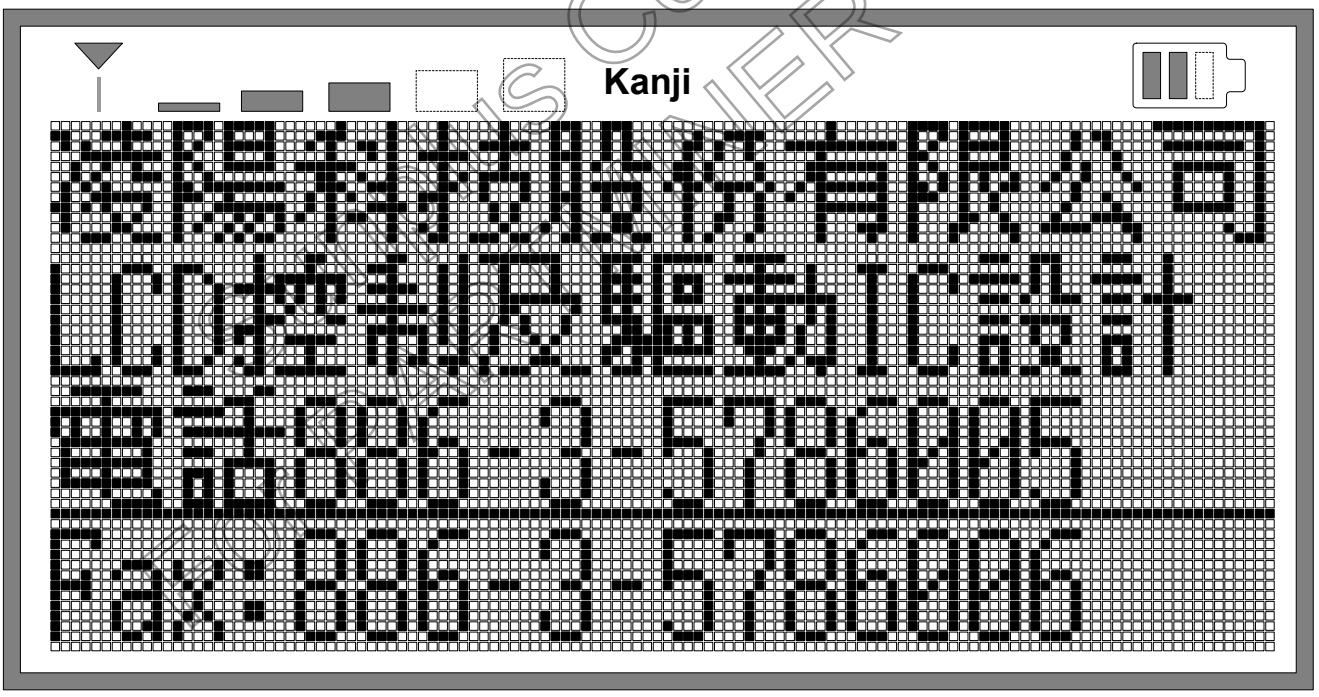


Black-white Reversed Line-Cursor (LC=1, BW=1)



Underline Line-Cursor (LC=1, C=1)

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Blinking Line-Cursor (LC=1, B=1)

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6.16. Display Control (R9)

RW	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	DC	DS	0	0	NC1	NC0

DC: Character/graphics display is on when DC = '1' and off when DC = '0'. When off, the display data remains in the DDRAM and CGRAM, and it can be displayed instantly by setting D = '1'.

DS: Icon mark segments are on when DS = '1' and off when DS = '0'. When off, the display data remains in the SGRAM, and can be displayed again instantly by setting DS = '1'. When DC = DS = '0' and all displays are off, all LCD driver outputs are set to the GND level and the display is off. Because of this, the SPLC701B has the capability to control charging current for the LCD with AC driving.

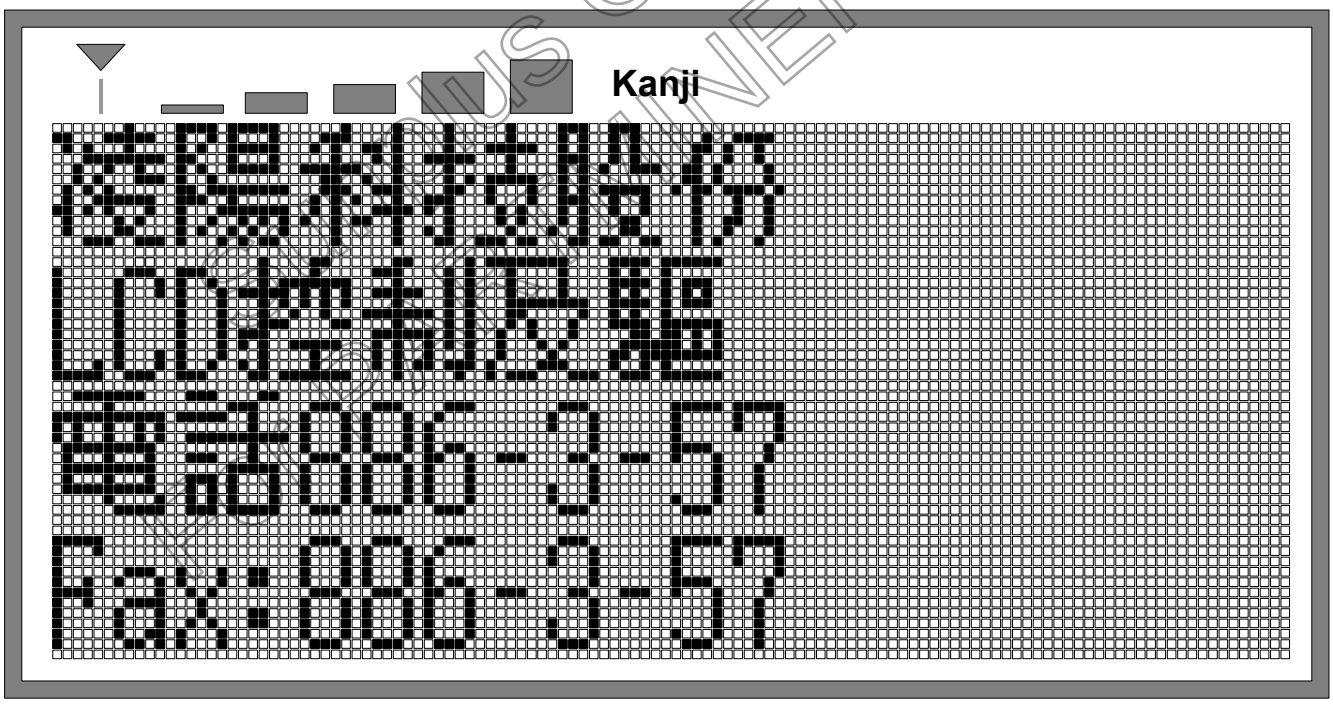
NC1 - 0: Sets the number of display characters per line.

NC1	NC0	Number of Characters	Segment Driver Used
0	0	6	SEG72 - 1
0	1	8	SEG96 - 1
1	0	10	SEG120 - 1
1	1	Inhibited	-

NC bits and Display Characters

Relationship between Drive Duty Ratio and Frame Frequency

	Number of Display Character		
	6-character display (NC = 00)	**8-character** display (NC = 01)	**10-character** display (NC = 10)
	Recommended R-C Oscillating Frequency		
Frame Frequency(Hz)	45KHz	60KHz	76KHz
Segment display (NL = 000)	74	74	74
1-line display (NL = 001)	75	75	74
2-line display (NL = 010)	75	77	76
3-line display (NL = 011)	73	75	75
4-line display (NL = 100)	74	74	74



Example of 6 full-size character display (NC1 = 0, NC0 = 0)

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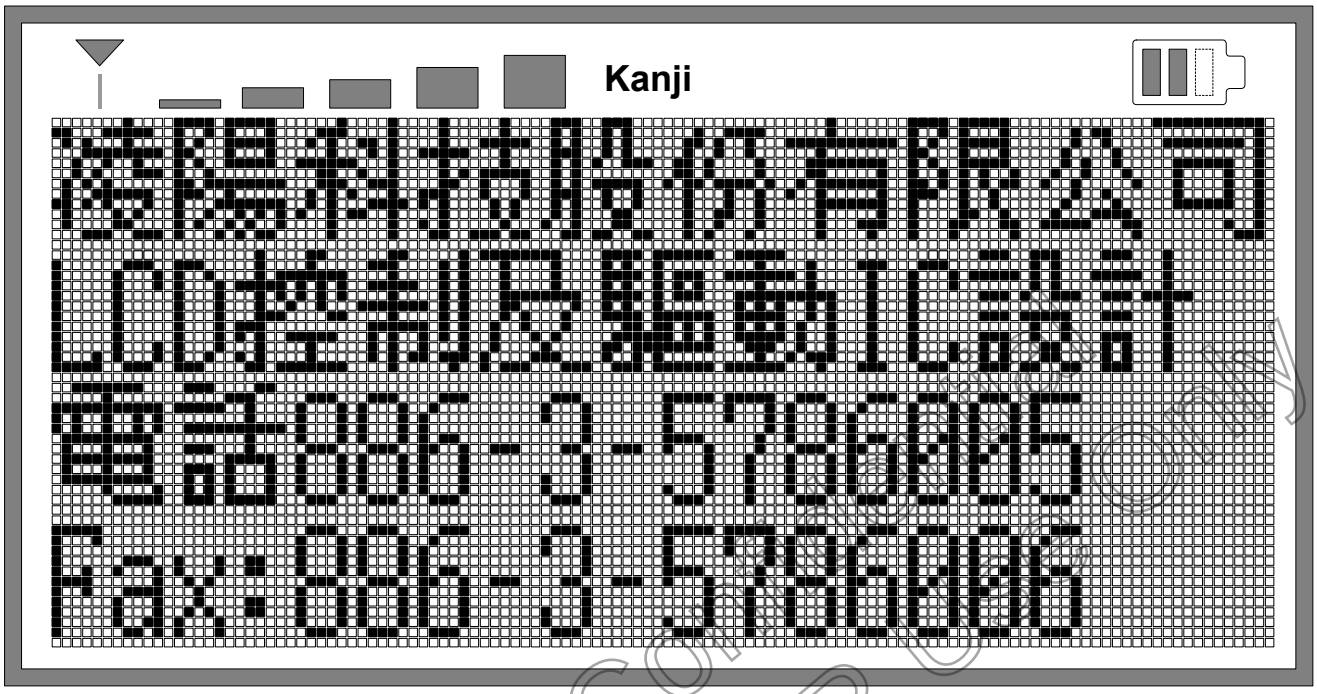

Example of 10 full-size character display (NC1 = 1, NC0 = 0)

6.17. Scroll Control (RA)

RW	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	SN1	SN0	SL3	SL2	SL1	SL0

SN1 - 0: Specify the display start line output from COM1. The data is displayed sequentially from the first line to the fourth line, and repeated from the first line.

SL3 - 0: Select the top raster-row to be displayed (display-start raster-row) in the display-start lines specified by SN1 - 0. Any raster-row from the first to fourth can be selected. This function is used to achieve raster-row-unit vertical smooth scrolling together with SN1 - 0.

SN1	SN0	Display-start line
0	0	1st line
0	1	2nd line
1	0	3rd line
1	1	4th line

SL3	SL2	SL1	SL0	Display-start Raster-row
0	0	0	0	1st raster-row
0	0	0	1	2nd raster-row

SL3	SL2	SL1	SL0	Display-start Raster-row
0	0	0	0	1st raster-row
0	0	0	1	2nd raster-row
0	0	1	0	3rd raster-row
0	0	1	1	4th raster-row
0	1	0	0	5th raster-row
0	1	0	1	6th raster-row
0	1	1	0	7th raster-row
…	…	…	…	…
1	0	1	0	11th raster-row
1	0	1	1	12th raster-row
1	1	0	0	13th raster-row

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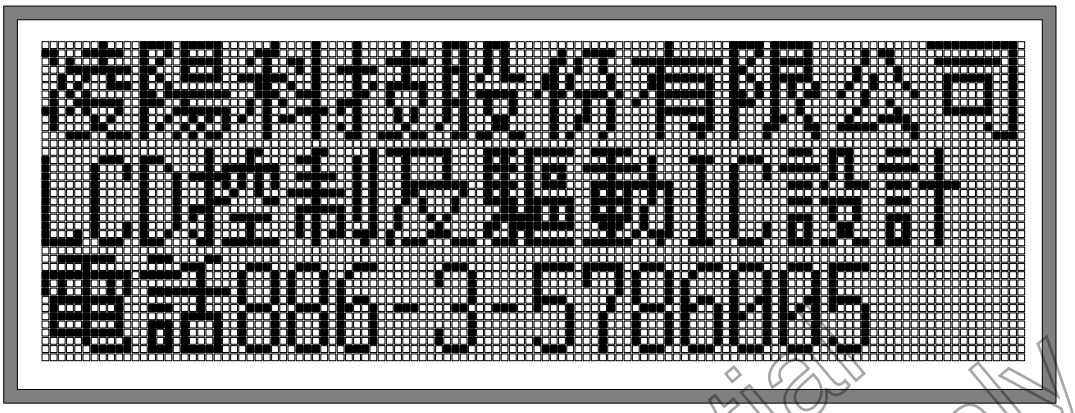
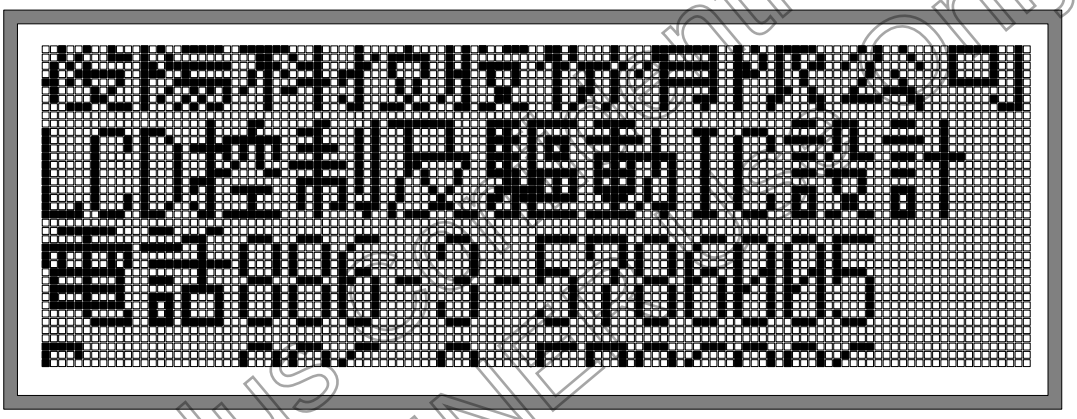
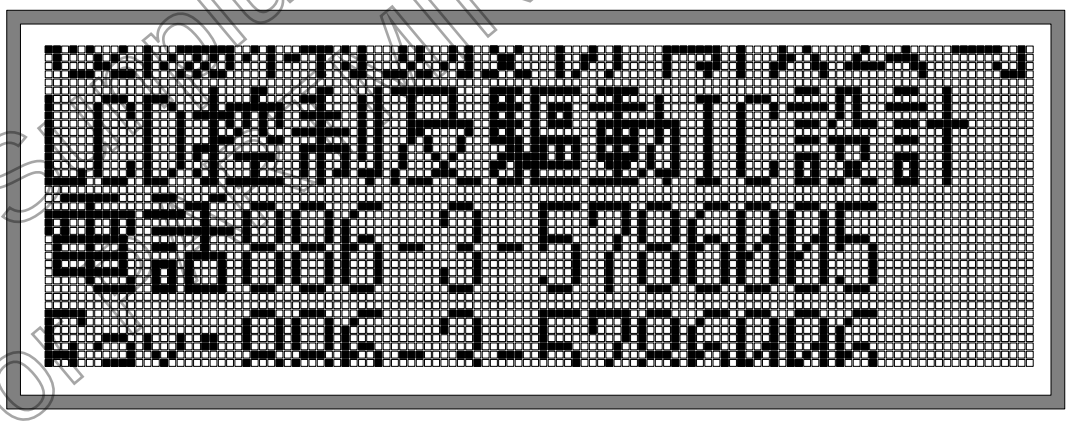
1). Not scrolled
- SN1/0 = 00
- SL3 - 0 = 0000



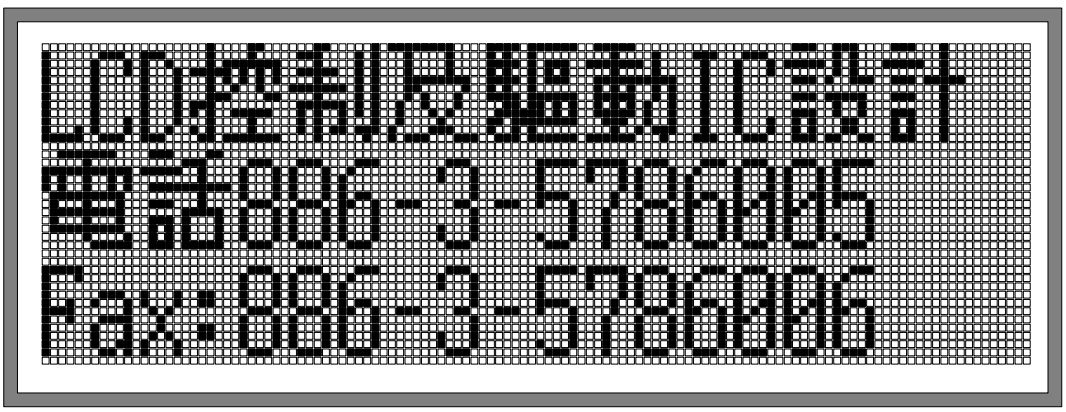
2). 4 raster-row scrolled up
- SN1/0 = 00
- SL3 - 0 = 0100



3). 8 raster-row scrolled up
- SN1/0 = 00
- SL3 - 0 = 1000



4). 13 raster-row scrolled up
- SN1/0 = 01
- SL3 - 0 = 0000



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6.18. Half-Size ROM (HCGROM) Select (RB)

RW	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	0	0	RL4	RL3	RL2	RL1

RL4 - 1: Switch the memory bank of the half-size HCGROM for the specified display line. Each Bank 0 and Bank 1 of the HCGROM incorporate 128 fonts, and display 256 fonts in total. The RL4 - 1 bits select HCGROM bank 0/1 for the display-line unit. When RL1 = '0', the first line selects bank 0. When RL1 = '1', the first line selects bank 1. The RL2, RL3, and RL4 bits select the second- to fourth-line memory banks, respectively.

6.19. Half-Size ROM (HCGROM Display Attribute (RC)

RW	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	A41	A40	A31	A30	A21	A20	A11	A10

A11/10: Designate the attributes of all half-size HCGROM fonts in the first line.

A21/20: Designate the attributes of all half-size HCGROM fonts in the second line.

A31/30: Designate the attributes of all half-size HCGROM fonts in the third line.

A41/40: Designate the attributes of all half-size HCGROM fonts in the fourth line.

The full-size fonts are specified with the two-bit attribute codes in each character code.

(A41, A40) / (A31, A30) / (A21, A20) / (A11, A10)		Half-size Font Display State
0	0	Normal display
0	1	Black-white reversed display
1	0	Blinking display
1	1	Black-white reversed blinking display

6.20. RAM Address (RD)

RW	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	RM1	RM0	0	0	0	AD10	AD9	AD8

6.21. RAM Address (RE)

RW	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

RM1 - 0: Select DDRAM, CGRAM, and SGRAM.

AD10 - 0: Initially set RAM addresses to the address counter (AC). Once the RAM data is written, the AC is automatically updated according to the I/D bit. This allows consecutive writing without resetting addresses. Once the RAM data is read, the AC is automatically updated when RDM = '0', but it is not updated when RDM = '1'. Reading, modifying, and writing are executed for every one-byte data, set RDM = '1'. RAM address setting is not allowed in the sleep mode or standby mode.

RM1	RM0	RAM Selection
0	0	DDRAM
0	1	Inhibited
1	0	CGRAM
1	1	SGRAM

6.22. RAM Write Data (RF)

RW	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0

6.23. RAM Read Data (RF)

RW	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0

WD7 - 0: Write 8-bit data to the DDRAM and CGRAM, and upper 4-bit data to the SGRAM. The DDRAM / CGRAM / SGRAM is selected by the previous specification of the RM 1/0 bit. After a write, the address is automatically incremented or decremented by 1 according to the I/D bit setting in the entry mode set instruction. During the sleep and standby modes, the DDRAM, CGRAM, or SGRAM cannot be accessed.

RD7 - 0: Read 8-bit data from the DDRAM, CGRAM or SGRAM. The DDRAM, CGRAM, or SGRAM is selected by the previous specification of the RM 1/0 bit. **In the parallel bus interface mode, the first-byte data reading will be invalid immediately after the RAM address set, and the consecutive second-byte data will be read normally. In the serial interface mode, two bytes will be invalid immediately after the start byte, and the consecutive third-byte data will be read normally.**

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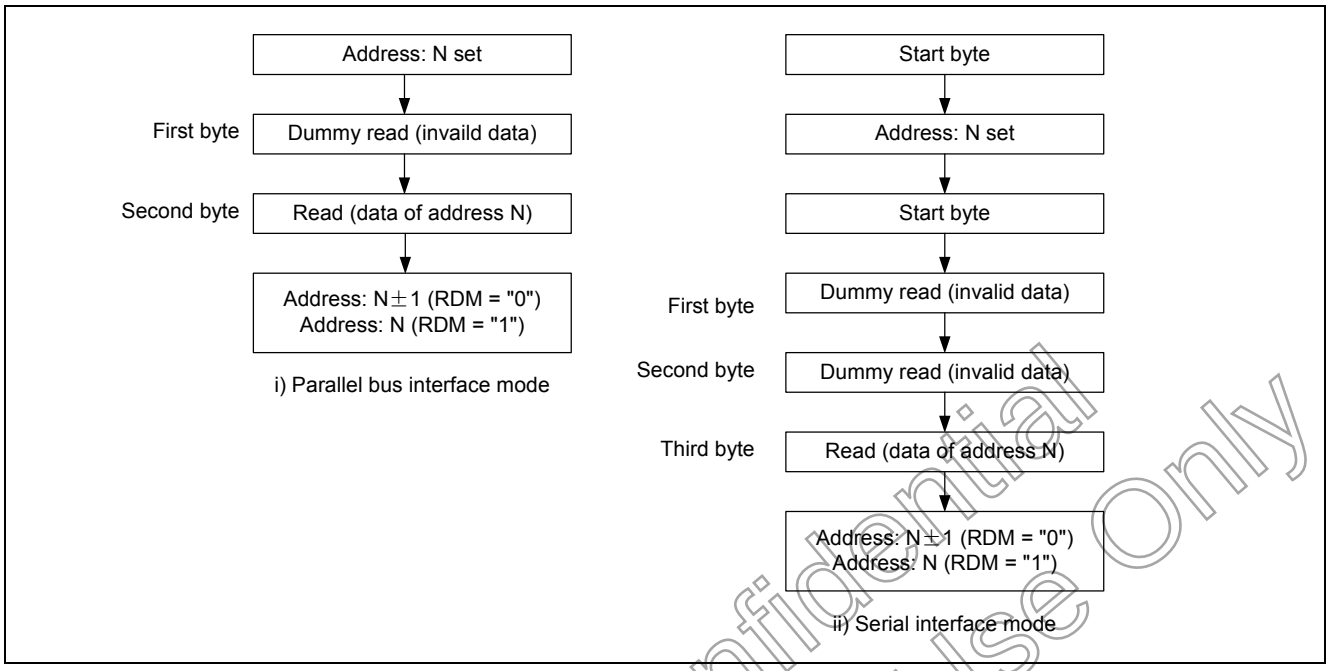

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7. SYSTEM INITIALIZE

The SPLC701B is internally initialized by RESETB input. During initialization, the system executes a display cleared instruction after reset is **cancelled.** The system executes the other instructions during the reset period. Because the busy flag (BF) indicates a busy state (BF = 1) during the reset period and the display cleared instruction is executed following reset **cancellation**, no instruction or RAM data access from the MPU is accepted. The reset input must be held for at least 1 ms. Any initializing instruction must wait for 200 clock cycles after the reset is **canceled** so that execution of the display cleared instruction can be completed.

7.1. Instruction Set Initialization

1). Execute display cleared (writes half-size space code A0H to DDRAM)
2). Start oscillation
3). Driver output control (NL2-0 = 100: 1/54 duty drive, CEN = 0, SGS = 0, CMS = 0, CEN = 0)
4). LCD waveform control (B/C = 0: B-pattern waveform, EOR = 0, NW4-0 = 0000)
5). LCD drive control (BS2 - 0 = 000: 1/8 bias drive, CT4 - 0 = 00000: Weak contrast)
6). Power control (AMP = 0: LCD power off, BT1/0 = 00: Single boost, SLP = 0: Sleep off, STB = 0: Standby off)
7). Key scan control (KSB = 0: Key scan, IRE = 0: Key interrupt (IRQ) disabled, KF1/0 = 00: set to 64 cycles)
8). Port control (PT2/1/0 = 000: PORT2/1/0 output = GND level)
9). Entry mode set (REV = 0, SPR = 0, GR = 0: Character display mode, RDM = 0, I/D = 1: Increment by 1)
10). Cursor control (CH = 0: Cursor home, LC = 0, B/W = 0, C = 0, B = 0)
11). Display control (DC/DS = 00: Display off, NC1/0 = 00: six-character display)
12). Scroll control (SN1/0 = 00, SL3/2/1/0 = 0000: First raster-row displayed at the top of the first line)
13). Half-size ROM control (RL4/3/2/1 = 0000: Bank 0 selection)
14). Half-size display attribute (A41 = A40 = A31 = A30 = A21 = A20 = A11 = A10 = 0:Normal half-size display)
15). RAM address (RM1/0 = 00: DDRAM selection, AD10 - 0 = 000H)

7.2. RAM Data Initialization

7.2.1. DDRAM

All addresses are initialized to A0H by the display cleared instruction after the reset is **canceled**.

7.2.2. CGRAM/SGRAM

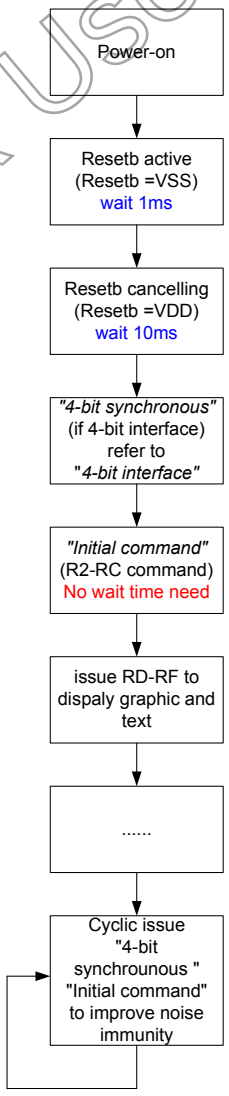
This is not automatically initialized by the reset input. It must be initialized by software while the display is off (DC = DS = 0).

7.3. Output PIN Initialization

1). LCD driver output pins (SEG/COM): Outputs GND level
2). Booster output pins (VLOUT): Outputs VCC level
3). Key strobe pins (KST3 - 0): Output strobe signals at specified time intervals
4). Key scan interrupt pin (IRQB): Outputs VCC level
5). General output ports (PORT2 - 0): Output GND level

8. DESIGN GUIDE

8.1. Power Sequential Procedure



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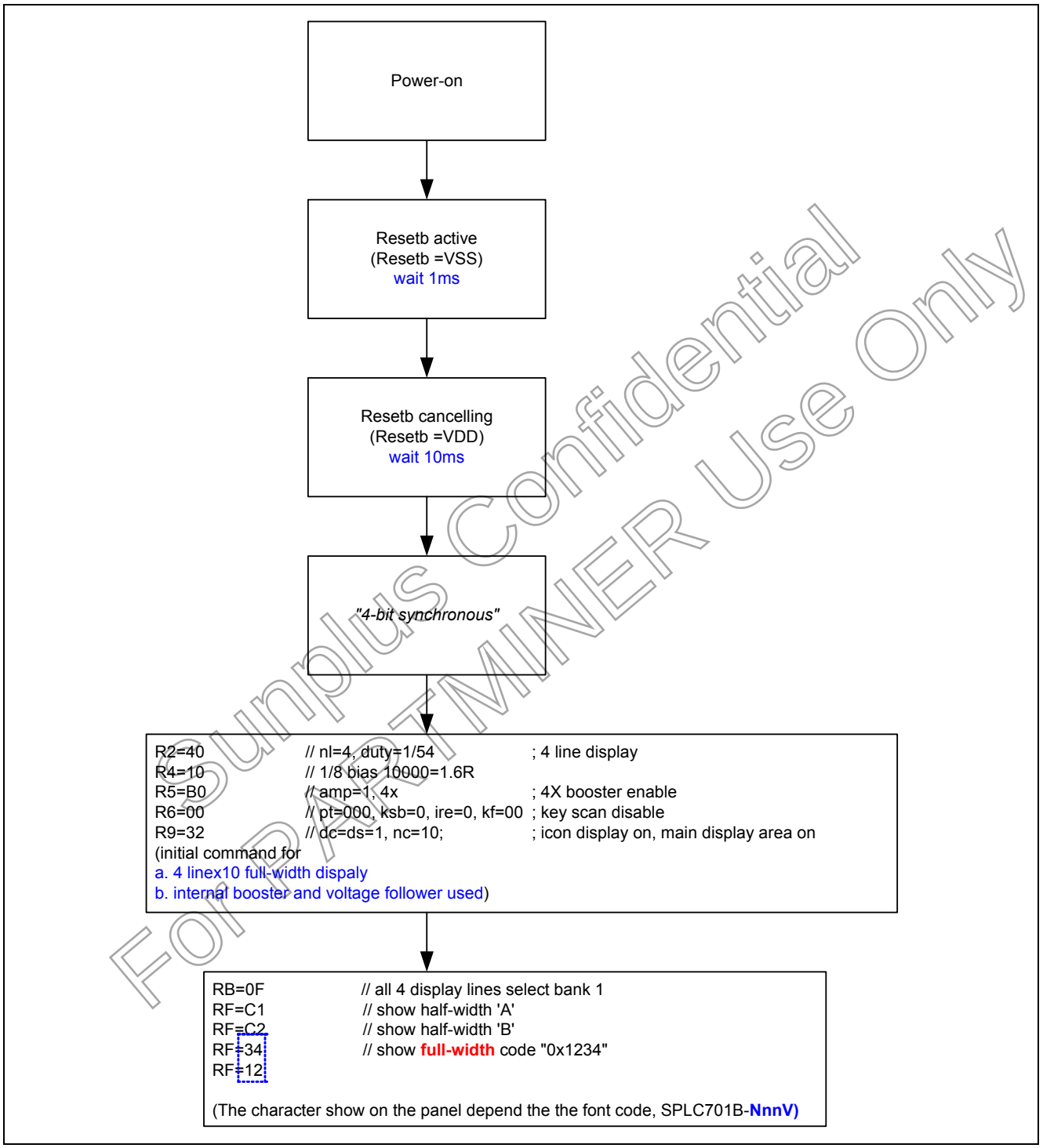
8.2. Example of 4 line x 10 full-width character with booster and voltage follower enable



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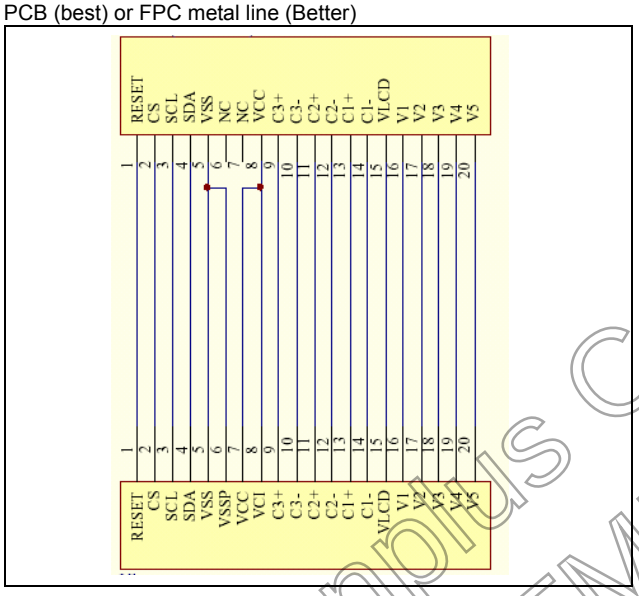
8.3. Wait Time

Address counter value(AC)	Min.
Reset active	1ms
Reset canceling	10ms
Clear display command(R0)	4ms
All other command	0us(no wait is ok)

8.4. FPC Layout

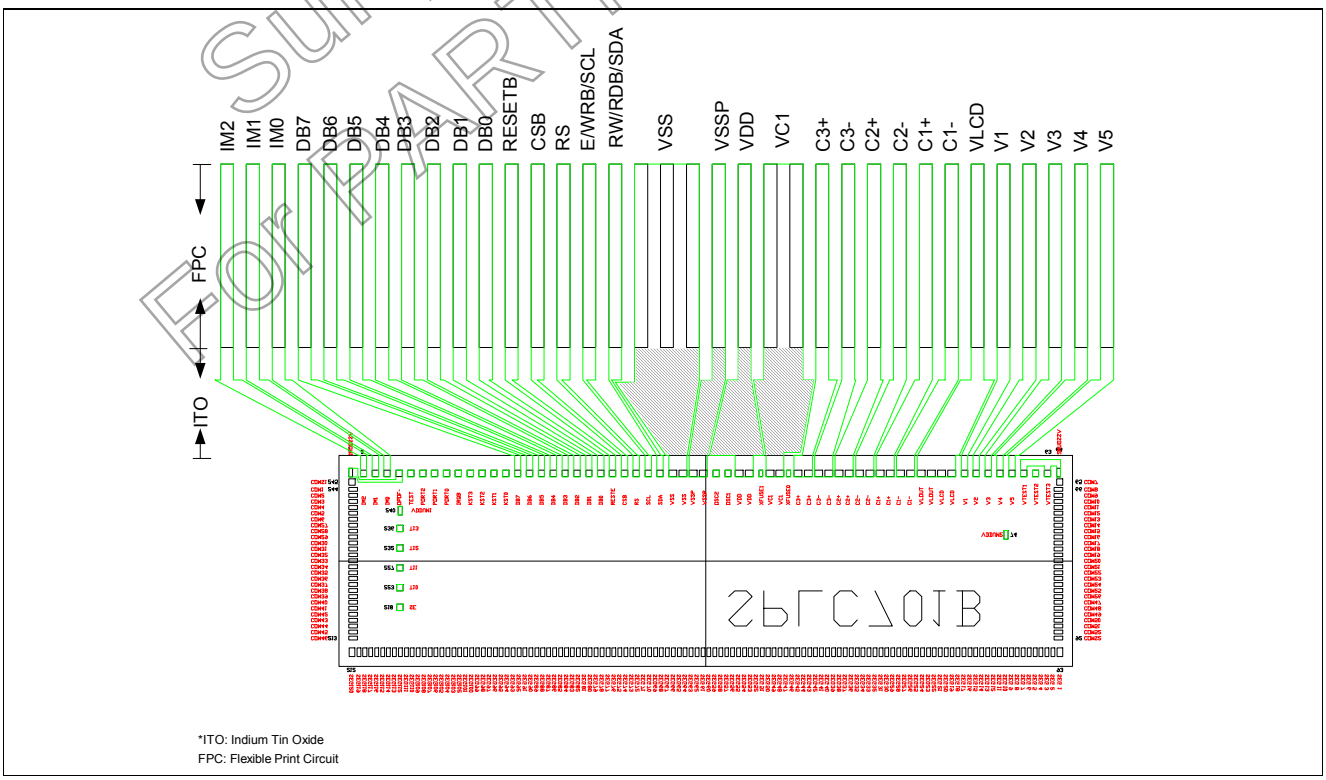
Do not short <VSS, VSSP>, <VDD, VCI> on ITO, please short on PCB (best) or FPC metal line (Better)



8.5. ITO Layout

The ITO Layout areas of VSS, VSSP, VDD and VCI pads should be as large as possible.

Pin name	Reference Resistor Value(ohm)	Priority
VSS	<80	1
VSSP	<80	2
VDD	<200	3
VCI	<200	4
C1+, C1-, C2+, C2-, C3+, C3-	<350	5
VLCD, VLOUT	<350	6
V1-V5	<700	7
CSB, RS, RW, SCL, SDA	<1.5K	8
Common	As uniform as possible	9
Segment pin	As uniform as possible	10
All other pin	<2K	11



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9. SRAM ADDRESS MAPPING

9.1. DDRAM Address Mapping

Display line	Panel Display Character(Half Size)																			
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1st	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
2nd	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33
3rd	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53
4th	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73

4th line 5th column = address **64_{16}**

9.2. Display-Start Lines

Display-line Mode	Duty Ratio	Common pins	1st line (SN = 00)	2nd line (SN = 01)	3rd line (SN = 10)	4th line (SN = 11)
1-line (NL = 100)	1/15	COM13 - 1	00_{16} - 13_{16}	20_{16} - 33_{16}	40_{16} - 53_{16}	60_{16} - 73_{16}
2-line (NL = 100)	1/28	COM13 - 1	00_{16} - 13_{16}	20_{16} - 33_{16}	40_{16} - 53_{16}	60_{16} - 73_{16}
		COM26 - 14	20_{16} - 33_{16}	40_{16} - 53_{16}	60_{16} - 73_{16}	00_{16} - 13_{16}
3-line (NL = 011)	1/41	COM13 - 1	00_{16} - 13_{16}	00_{16} - 13_{16}	40_{16} - 53_{16}	60_{16} - 73_{16}
		COM26 - 14	20_{16} - 33_{16}	20_{16} - 33_{16}	60_{16} - 73_{16}	00_{16} - 13_{16}
		COM39 - 27	40_{16} - 53_{16}	40_{16} - 53_{16}	00_{16} - 13_{16}	20_{16} - 33_{16}
4-line (NL = 100)	1/54	COM13 - 1	00_{16} - 13_{16}	00_{16} - 13_{16}	40_{16} - 53_{16}	60_{16} - 73_{16}
		COM26 - 14	20_{16} - 33_{16}	20_{16} - 33_{16}	60_{16} - 73_{16}	00_{16} - 13_{16}
		COM39 - 27	40_{16} - 53_{16}	40_{16} - 53_{16}	00_{16} - 13_{16}	20_{16} - 33_{16}
		COM52 - 40	60_{16} - 73_{16}	60_{16} - 73_{16}	20_{16} - 33_{16}	40_{16} - 53_{16}

9.3. Combined Display of Full-Size and Half-Size Characters

The SPLC701B creates a display from the left edge of the display area combining 12-dot full-size (font size: 11 x 12 dots) and 6-dot half-size characters (font size: 5 x 12 dots). There will be a one-dot space between these fonts. The most significant bit in the data (8 bits) in the DDRAM is allocated to the designation bit indicating a full-size or half-size character. When this MSB is 0, the full-size character is selected, and when 1, the half-size character is selected.

When the full-size character is selected, two bytes of DDRAM are linked and used as a 16-bit code. In this case, the lower byte is written into the smaller DDRAM address. 13 bits of this 16-bit code are used as character codes. Since up to 8,192 character codes can be specified, symbols can be used as well as the JIS Level-1 and Level-2 Kanji Sets. In addition, two of the remaining bits can be allocated to a display-attribute code and can designate a black-white reversed display for individual characters.

Below table shows the relationship between the 16-bit designated JIS code and the SPLC701B 13-bit character code. The 8-bit data designating half-size characters are used as an 8-bit code. Specifically, 7 bits of the 8-bit half-size characters become the character codes, so that a total of 128 characters can be displayed (alphanumeric characters and symbols can be displayed as half-size characters). These 128 CGROMs (HCGROMs) for half-size fonts have two memory banks and incorporate a total of 256 half-size fonts. These memory banks are switched in a display-line unit by bits RL4 - 1 in the half-size ROM select register (RA). A half-size font display attribute is designated by the half-size display attribute register (RB) in a display-line unit. Note that the same display attribute in a character unit such as the full-size font cannot be specified.

User fonts can be displayed using the CGRAM. Special symbols not included in the internal CGROM can be displayed as needed. Since the display font size of the CGRAM is 12 x 13 dots, CGRAM fonts can be displayed to the right, left, top, or bottom, in order to

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be used to display double-size characters. In the super-imposed display mode, which displays the combined character display mode and graphics display mode, this CGRAM becomes the bit map memory for the graphics display and cannot be used as the user font for characters.

0	A_1	A_0	C_{12}	C_{11}	C_{10}	C_9	C_8	Upper byte
C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0	Lower byte

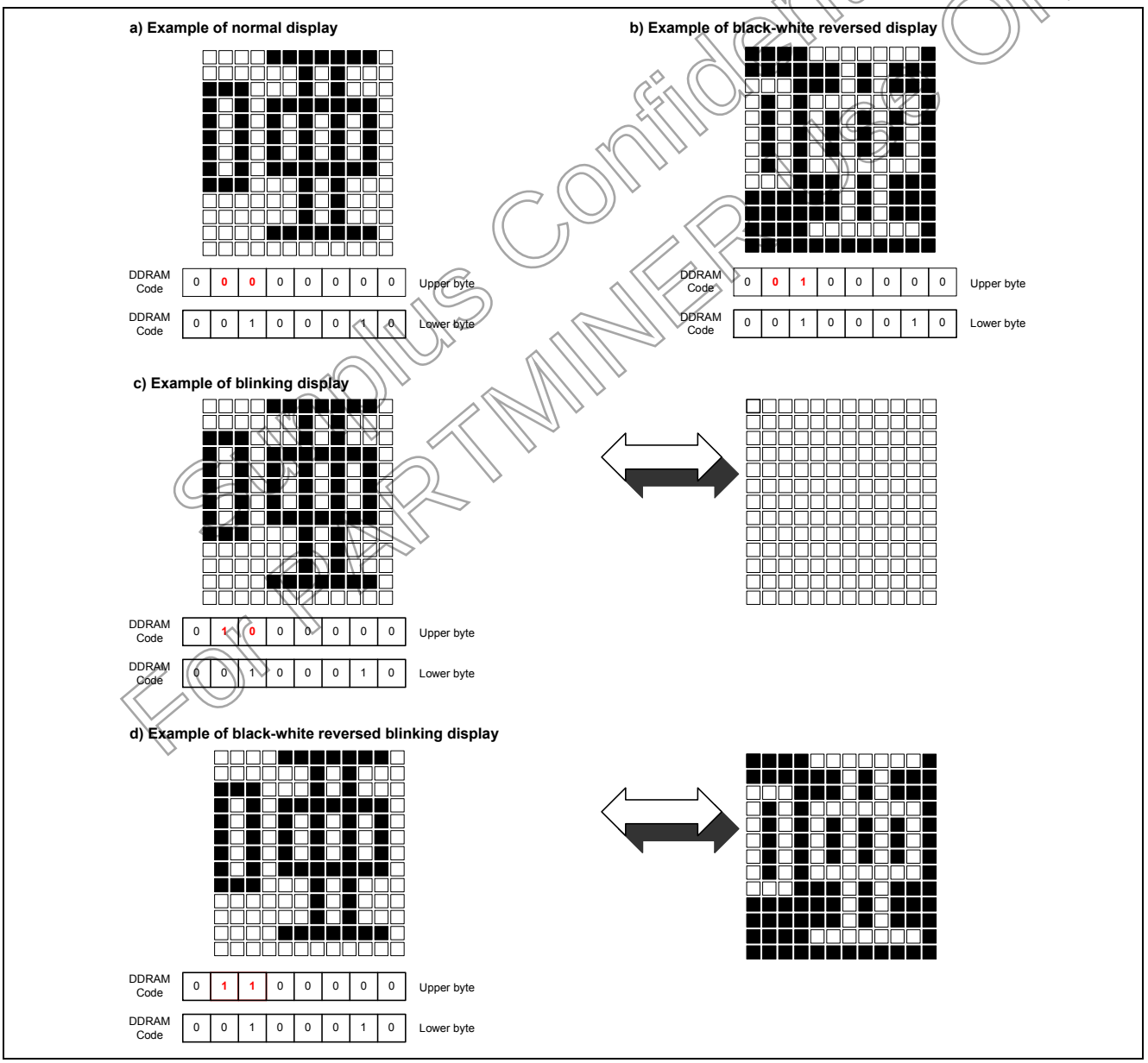
Character code : C_{12} - C_0 (13 bits)

Display attribute code : A_1/A_0 (2 bits)

Full-size Code Format

Attribute code and Display Contents

A1	A0	Full-size Font Display attribute
0	0	Normal display
0	1	Black-white reversed display
1	0	Blinking display
1	1	Black-white reversed blinking display



Example of Full-size Character Display at Display Attribute Designation

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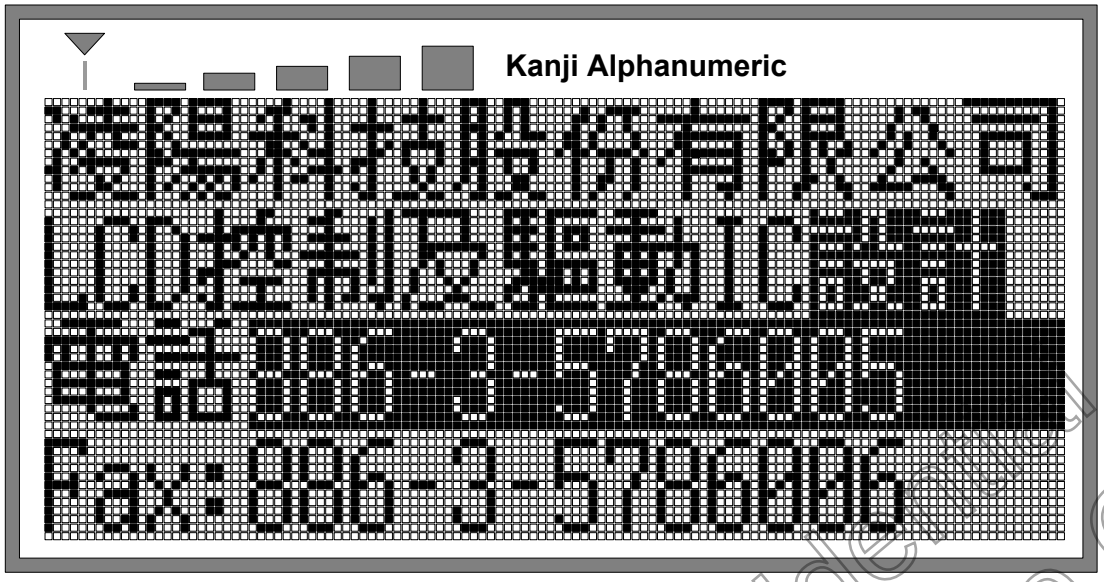


i) Black-white reversed display of full-size "³]-p"
¡DA1 = 0
¡DA0 = 1

ii) Black-white reversed display of half-size characters in the 3rd line
¡DA31 = 0
¡DA30 = 1

iii) Black-white reversed display of full-size "電話"
¡DA1 = 0
¡DA0 = 1

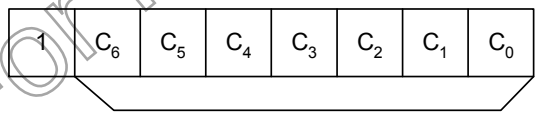
Example of Black-white Reversed Character Display

JIS first byte code: b7 - 1(7bits)

JIS second byte code: b7 - 1(7bits)

CGRAM code for user fonts: u6 - 1(6bits)

JIS Code				SPLC701B Character Code												
	B7	B6	B5	C_{12}	C_{11}	C_{10}	C_9	C_8	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0
Non-kanji	0	1	0	0	A7	A6	B3	B2	B1	0	0	A5	A4	A3	A2	A1
Level-1 Kanji	0	1	1	0	B7	B4	B3	B2	B1	A7	A6	A5	A4	A3	A2	A1
	1	0	0	0	B7	B4	B3	B2	B1	A7	A6	A5	A4	A3	A2	A1
Level-2 Kanji	1	0	1	1	B6	B4	B3	B2	B1	A7	A6	A5	A4	A3	A2	A1
	1	1	0	1	B6	B4	B3	B2	B1	A7	A6	A5	A4	A3	A2	A1
	1	1	1	1	A7	A6	B3	B2	B1	0	0	A5	A4	A3	A2	A1
User Font	-	-	-	U6	0	0	0	0	0	0	0	U5	U4	U3	U2	U1
				Upper byte					Lower byte							



MSB LSB
Character code: C_{6-0} (7bits)

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10. JIS CODE AND SPLC701B CHARACTER CODE

The full-size character display conforms to the JIS code (16 bits). According to the relationship between the 13-bit JIS code, the code is converted from 16 bits to 13 bits, and the data of two bytes/character is written to the DDRAM. Write the lower byte to the smaller DDRAM address. When displaying a half-size character, write the one byte/character data to the DDRAM. Display attribute control is performed for a 12 x 13 dot matrix unit that includes a 11 x 12 dot full-size character and a column of dots to the right and a row of dots at the bottom. The blinking cycle for the blinking display and black-white reversed blinking display is 64 frames. The blinking display is provided by changing the display pattern every 32 frames.

Scan Sequence ←

DDRAM address	00	01	02	03
DDRAM data	1000-0001	0010-1110	0000-0111	1000-0010
Display font	“1”	“八”		“2”

Note: The LCD scan from right to left.

10.1. CGRAM Address Mapping for User Define Font

Character Code		0000	0001	0002	0003	0004	0005	0006	0007	0008	0009
CGRAM Address	DB0	000 | 00B	00C | 017	018 | 023	024 | 02F	030 | 03B	03C | 047	048 | 053	054 | 05F	060 | 06B	06C | 077
	DB1										
	DB2										
	DB3										
	DB4										
	DB5										
	DB6										
	DB7										
	DB0	100 | 10B	10C | 117	118 | 123	124 | 12F	130 | 13B	13C | 147	148 | 153	154 | 15F	160 | 16B	16C | 177
	DB1										
	DB2										
	DB3										
	DB4										
Character Code		**0010**	**0011**	**0012**	**0013**	**0014**	**0015**	**0016**	**0017**	**0018**	**0019**
CGRAM Address	DB5	100 | 10B	10C | 117	118 | 123	124 | 12F	130 | 13B	13C | 147	148 | 153	154 | 15F	160 | 16B	16C | 177
	DB6										
	DB7										
	DB0	200 | 20B	20C | 217	218 | 223	224 | 22F	230 | 23B	23C | 247	248 | 253	254 | 25F	260 | 26B	26C | 277
	DB1										
	DB2										
	DB3										
	DB4										
	DB5										
	DB6										
	DB7										
	DB0	300-30B	30C-317	318-323	324-32F	330-33B	33C-347	348-353	354-35F	360-36B	36C-377
	DB1										

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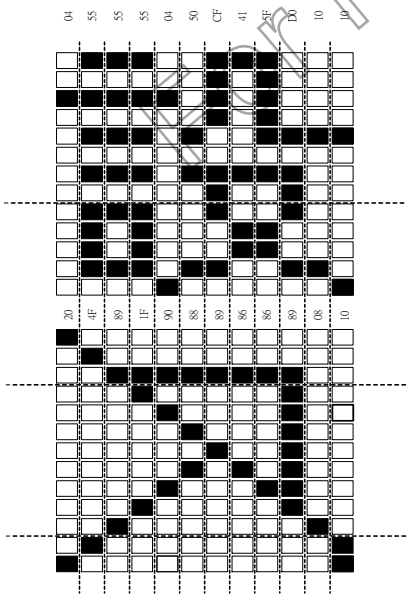
Character Code		1000	1001	1002	1003	1004	1005	1006	1007	1008	1009
CGRAM Address	DB2 DB3 DB4 DB5 DB6 DB7	300 | 30B	30C | 317	318 | 323	324 | 32F	330 | 33B	33C | 347	348 | 353	354 | 35F	360 | 36B	36C | 377
	DB0 DB1 DB2 DB3 DB4 DB5 DB6	400 | 40B	40C | 417	418 | 423	424 | 42F	430 | 43B	43C | 447	448 | 453	454 | 45F	460 | 46B	46C | 477
Character Code		**1010**	**1011**	**1012**	**1013**	**1014**	**1015**	**1016**	**1017**	**1018**	**1019**
CGRAM Address	DB7	400-40B	40C-417	418-423	424-42F	430-43B	43C-447	448-453	454-45F	460-46B	46C-477
	DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7	500 | 50B	50C | 517	518 | 523	524 | 52F	530 | 53B	53C | 547	548 | 553	554 | 55F	560 | 56B	56C | 577
	DB0 DB1 DB2 DB3	600-60B	60C-617	618-623	624-62F	630-63B	63C-647	648-653	654-65F	660-66B	66C-677



Two user define character, 0000_{16} and 0010_{16} , shown on left demonstrating what data should be fill into CGRAM to form the 12*13 full-windows user fonts.

Addr[0_{16}..$0B_{16}$] = {04, 55, 55, 55, 04, 50, CF, 41, 5F, D0, 10, 10} (hexadecimal form)

Addr[100_{16}..$10B_{16}$] = { 20, 4F, 89, 1F, 90, 88, 89, 86, 86, 89, 08, 10} (hexadecimal form)

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10.2. CGRAM Address Mapping for Graphical Mode (SGS=0)

	Segment driver	Seg1	Seg2	Seg3	Seg4	Seg5	Seg6	Seg7	Seg8	Seg9	Seg10	Seg11	Seg12	Seg13	Seg14	Seg15	Seg16	Seg17	Seg18	Seg19	Seg20	Seg21	Seg22	Seg23	Seg24	Seg25	Seg26	Seg27	Seg28	Seg29	Seg30	Seg31	Seg32	Seg33	Seg34	Seg35	… … …	Seg118	Seg119	Seg120	SEG / COM
ADDR 000_{16}~077_{16}	DB0										1	1	1	1	1	1	1	1	1	1	1																				Com1
	DB1								1	1												1	1																			Com2
	DB2						1	1																1	1																	Com3
	DB3				1	1																				1	1														Com4
	DB4			1	1											1											1	1													Com5
	DB5		1	1												1												1	1											Com6
	DB6	1	1													1													1	1										Com7
	DB7	1														1														1	1									Com8
ADDR 100_{16}~177_{16}	DB0	1														1																								Com9
	DB1	1														1																								Com10
	DB2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1										Com11
	DB3															1															1										Com12
	DB4															1															1										Com13
	DB5	1	1													1															1										Com14
	DB6	1	1													1														1	1										Com15
	DB7		1	1												1													1	1											Com16
ADDR 200_{16}~277_{16}	DB0				1	1										1												1	1											Com17
	DB1					1	1																		1	1															Com18
	DB2							1	1														1	1																	Com19
	DB3									1	1	1	1	1	1	1	1	1	1	1	1	1																			Com20
	DB4																																								Com21
	DB5																																								Com22
	DB6																																								Com23
	DB7																																								Com24
ADDR 300_{16}~377_{16}	DB0																																								Com25
	DB1																																								Com26
	DB2																																								Com27
	DB3																																								Com28
	DB4																																								Com29
	DB5																																								Com30
	DB6																																								Com31
	DB7																																								Com32
ADDR 400_{16}~477_{16}	DB0																																								Com33
	DB1																																								Com34
	DB2																																								Com35
	DB3																																								Com36
	DB4																																								Com37
	DB5																																								Com38
	DB6																																								Com39
	DB7																																								Com40
ADDR 500_{16}~577_{16}	DB0																																								Com41
	DB1																																								Com42
	DB2																																								Com43
	DB3																																								Com44
	DB4																																								Com45
	DB5																																								Com46
	DB6																																								Com47
	DB7																																								Com48
ADDR 600_{16}~677_{16}	DB0																																								Com49
	DB1																																								Com50
	DB2																																								Com51
	DB3																																								Com52

Note: Address [600_{16}~677_{16}] are all half-byte only.

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10.3. SGRAM Address Mapping (SGS=0)

	Segment driver	Seg1	Seg2	Seg3	Seg4	Seg5	Seg6	Seg7	Seg8	Seg9	Seg10	Seg11	Seg12	Seg13	Seg14	Seg15	Seg16	Seg17	⋮ ⋮ ⋮	Seg118	Seg119	Seg120	SEG / COM
ADDR 000_{16}–077_{16}	DB0	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
	DB1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
	DB2	*	*	*	*	*	*	*	(Invalid area)					*	*	*	*	*	*	*	*	*	*	*
	DB3	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
	DB4	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	COMS1
	DB5	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	
	DB6	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	COMS2
	DB7	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	

There are 2 common for icon display, 120 segment * 2 common = 240 com-seg intersection for icon. SEG1, SEG4, SEG7, SEG10, SEG13,…, SEG112, SEG115, SEG118, total: 40 segment, are gray-scale icon. Others are mono-blinking icons. And COMS1 and COMS2 are controlled by the same grayscale. So we total have only (120-40)*2+40 = 200 individual icons.

Relationship between SGRAM and Grayscale Segment Display

DB7	DB6	DB5	DB4	Effective voltage for COMS1
0	0	0	0	0(always unlit)
0	0	0	1	1(always lit)
0	0	1	0	0.34(graylevel)
0	0	1	1	0.38(graylevel)
0	1	0	0	0.41(graylevel)
0	1	0	1	0.44(graylevel)
0	1	1	0	0.47(graylevel)
0	1	1	1	0.50(graylevel)
1	0	0	0	(Blink display)
1	0	0	1	0.53(graylevel)
1	0	1	0	0.56(graylevel)
1	0	1	1	0.59(graylevel)
1	1	0	0	0.63(graylevel)
1	1	0	1	0.66(graylevel)
1	1	1	0	0.69(graylevel)
1	1	1	1	0.72(graylevel)

Relationship between SGRAM and Mono-Blinking Segment Display for COMS1 80-blinking Segment

DB5	DB4	LCD display control for coms1 segment
0	0	Always unlit
0	1	Always lit
1	0	Blinking display (32-frame unit)
1	1	Double-speed blinking display (16-frame unit)

Relationship between SGRAM and Mono-Blinking Segment Display for COMS2 80-blinking Segment

DB7	DB6	LCD display control for coms2 segment
0	0	Always unlit
0	1	Always lit
1	0	Blinking display(32-frame unit)
1	1	Double-speed blinking display(16-frame unit)

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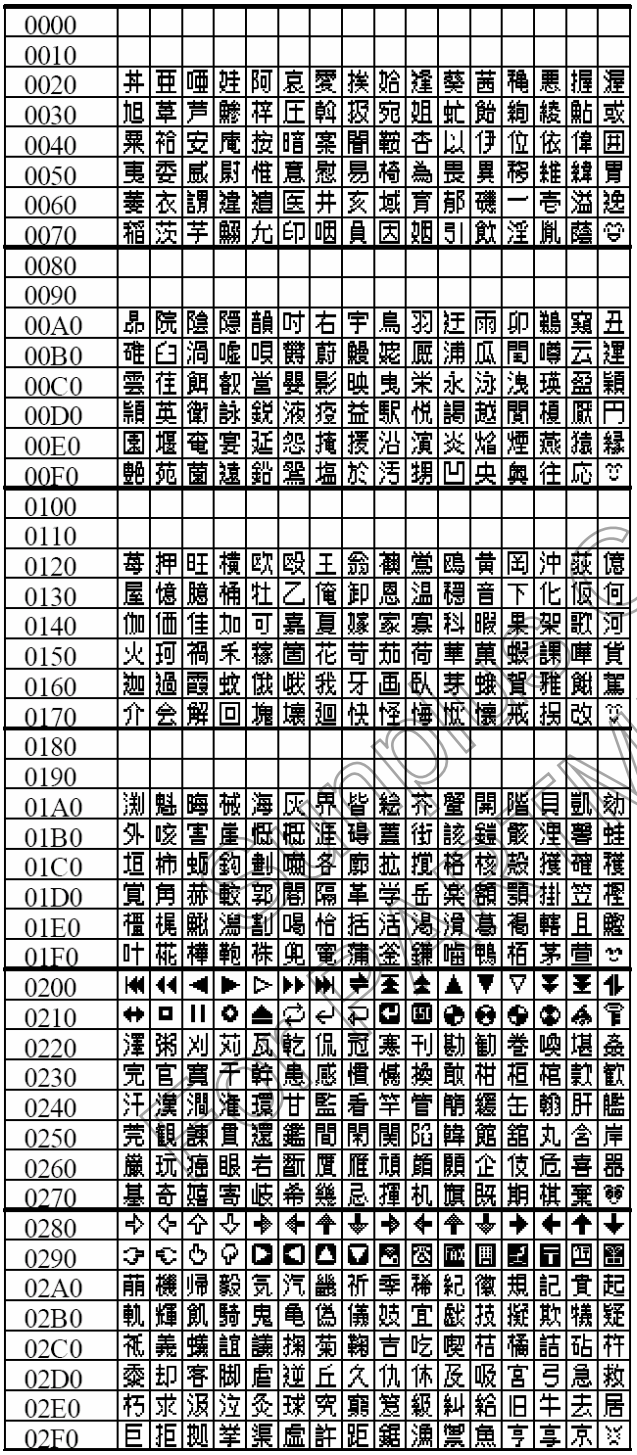
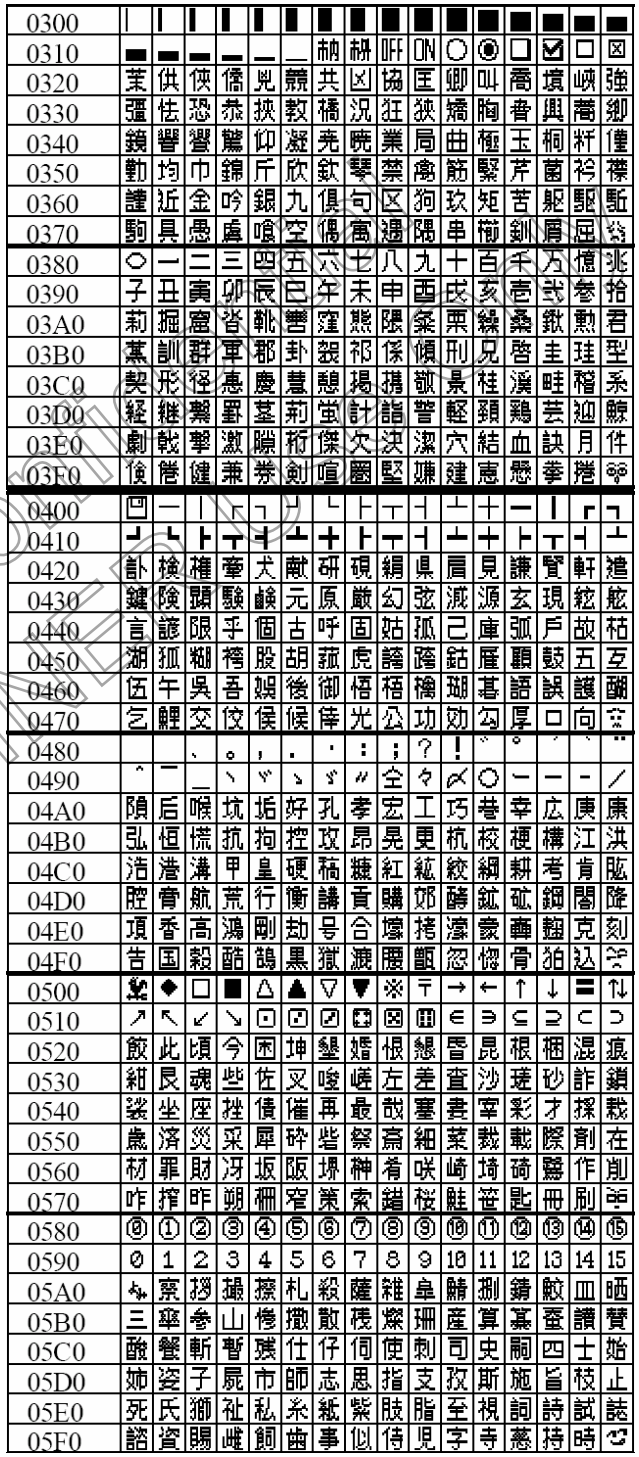
11. Code 003A Example

For better quality, please download the font database and font editor from Sunplus' web site.

11.1. Full-Size Font Pattern





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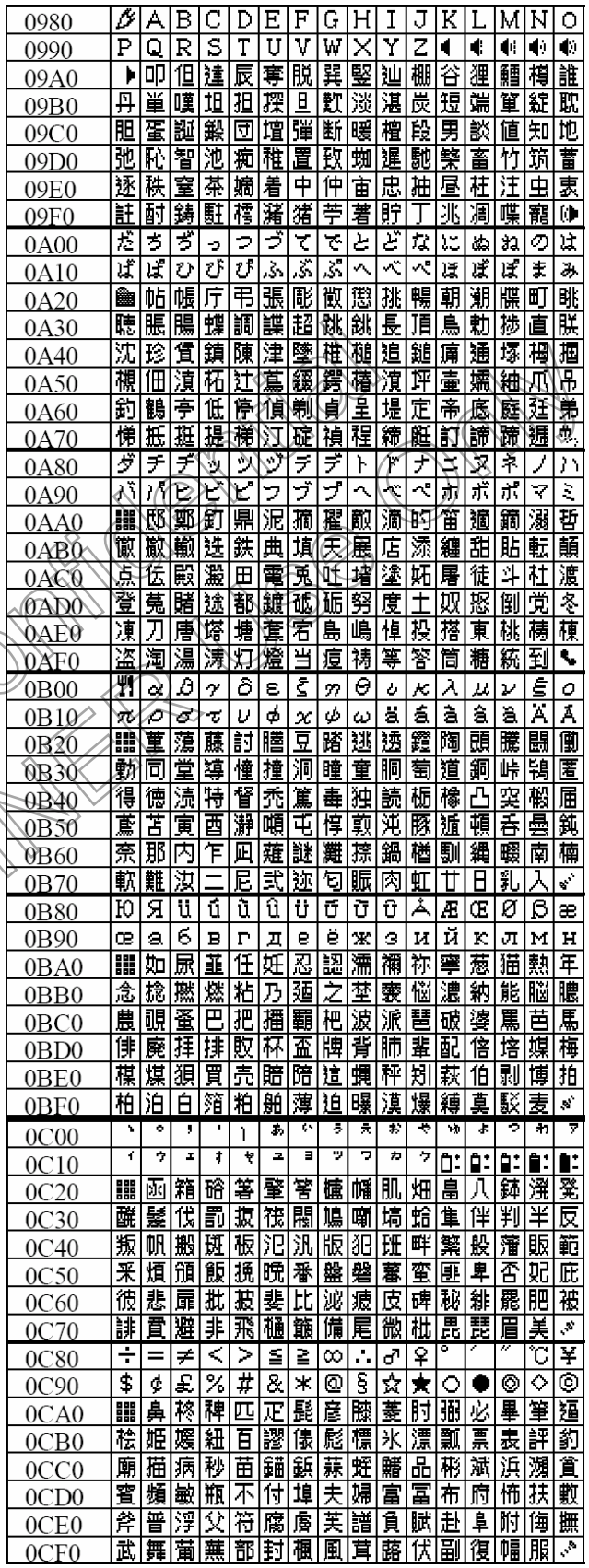

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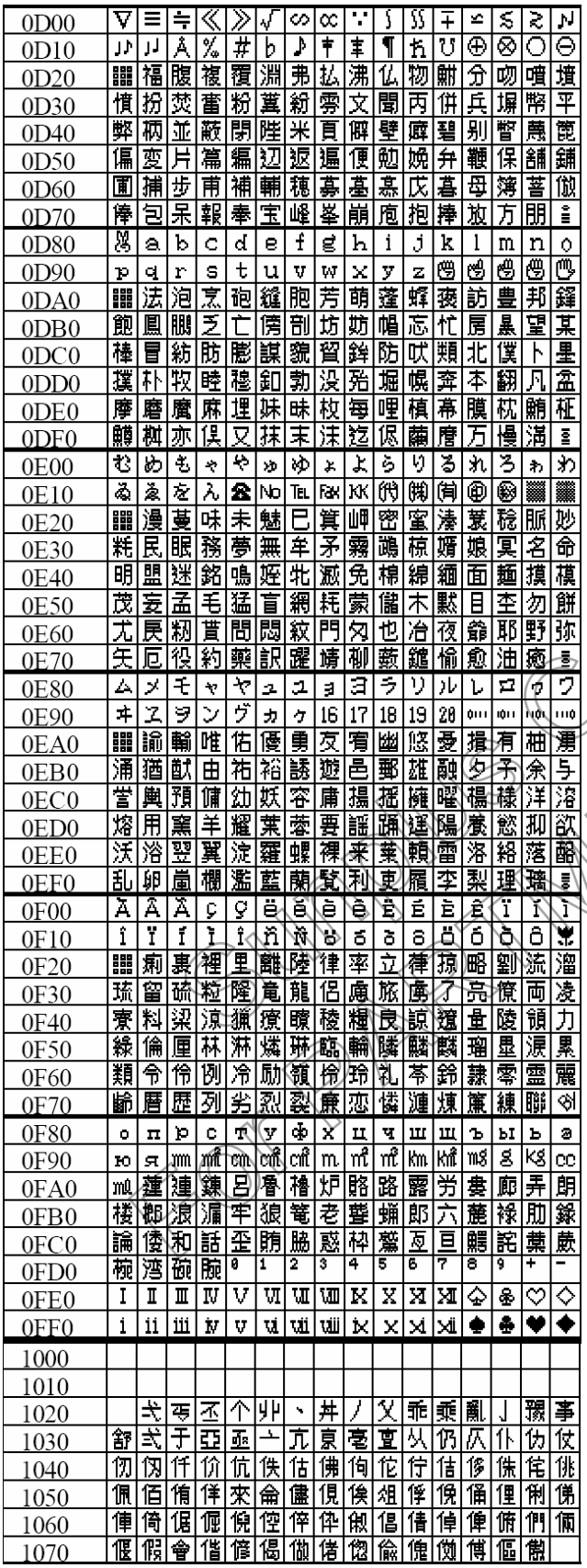

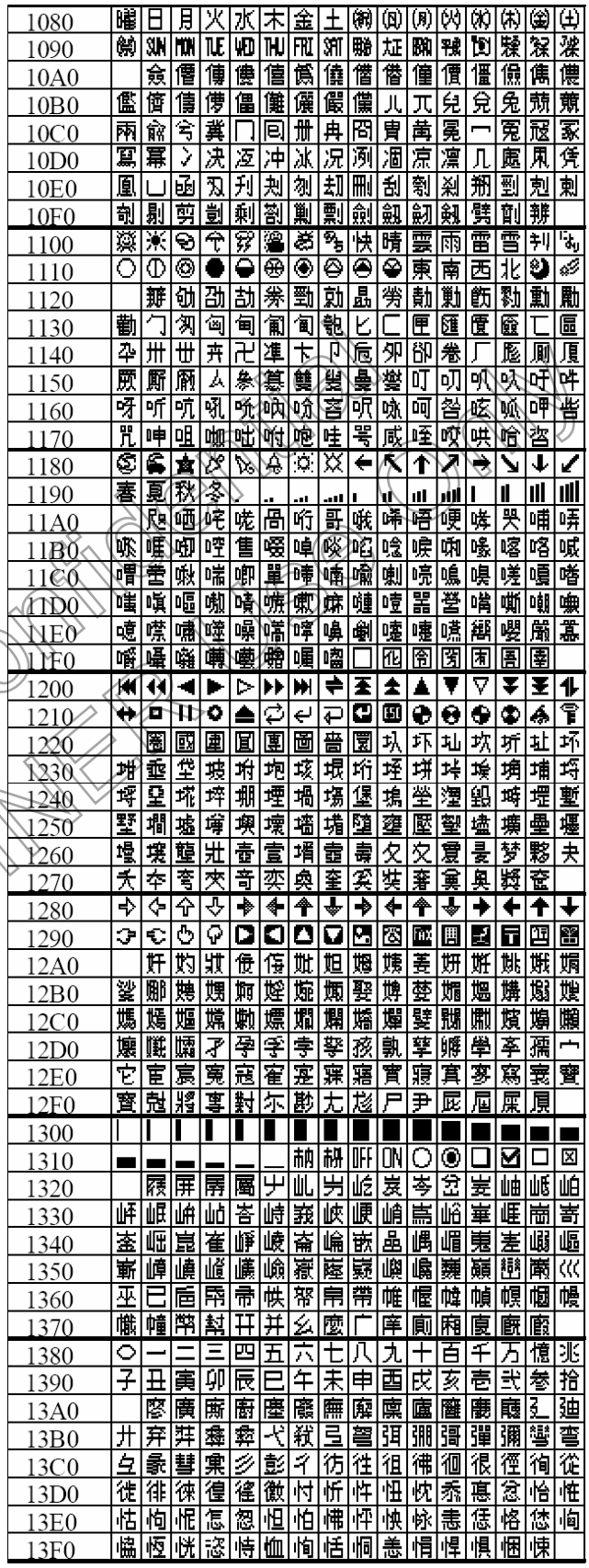

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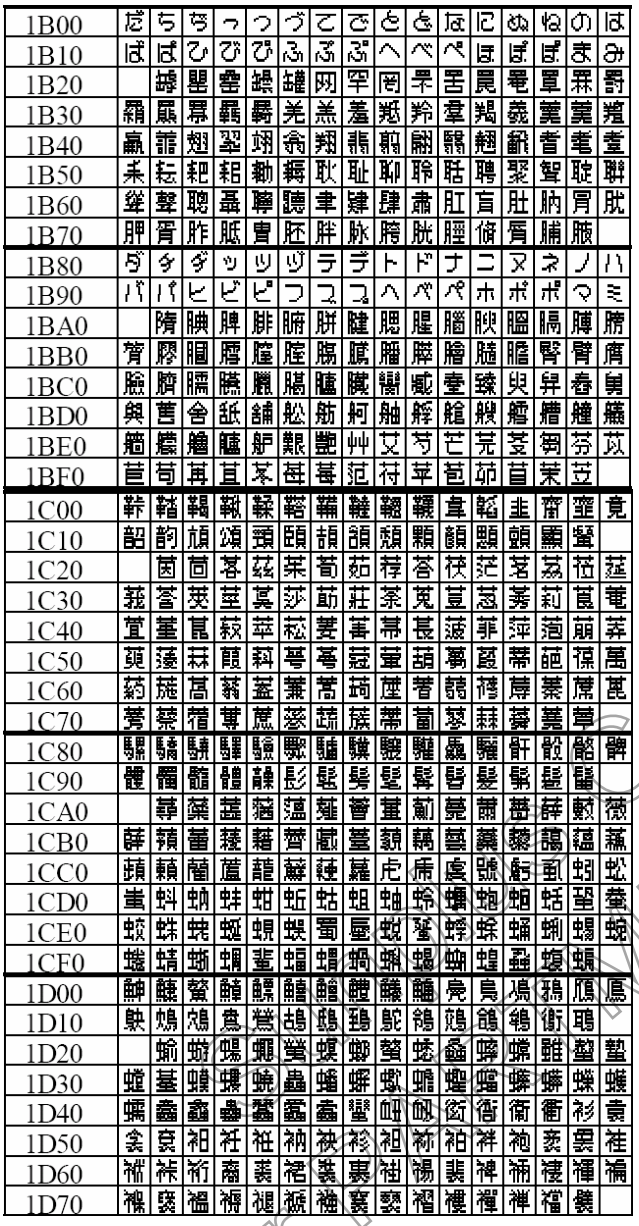
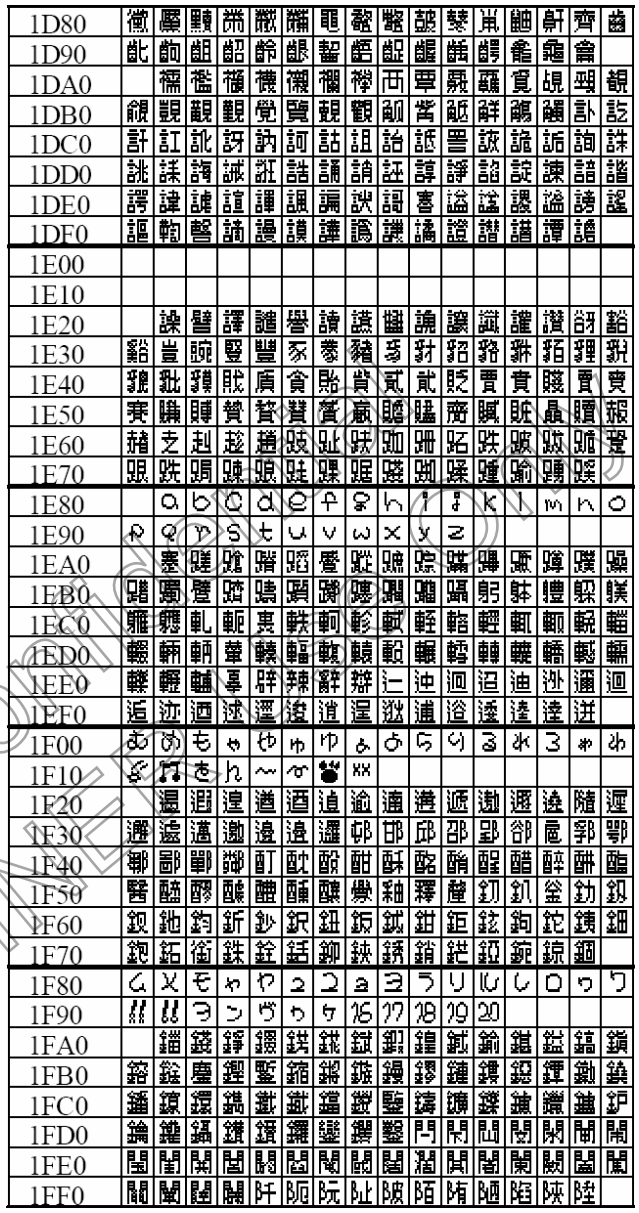
1400		陜	陟	陭	陲	陬	隍	隂	隕	隗	險	隨	隱	隮	隰	隴
1410	隶	隸	隹	雎	雋	雉	雍	襍	雜	霍	雕	雹	霄	霆	霈	霓
1420		悄	悛	悖	悗	悒	悧	悋	惡	悸	惠	惓	悴	忰	悽	惆
1430	悵	惘	慍	愕	愆	惶	惷	愀	惴	惺	愃	愡	惻	惱	愍	愎
1440	慇	愾	慤	愧	慊	愿	愼	愬	愴	愽	慂	慄	慳	慷	慘	慙
1450	慚	慫	慴	慯	慥	慱	慟	慝	慓	慵	憙	憖	憇	憬	憔	憚
1460	憊	憑	憫	憮	懌	懊	應	懷	懈	懃	懆	憺	懋	罹	懍	懦
1470	懣	懶	懺	懴	懿	懽	懼	懾	戀	戈	戉	戍	戌	戔	戛	
1480		顬	顫	顰	颪	颯	颱	颶	飄	飃	飆	飩	飫	餃	餉	餒
1490	餔	餘	餡	餝	餞	餤	餠	餬	餮	餽	餾	饂	饉	饅	饐	饋
14A0		戞	戡	截	戮	戰	戲	戳	扁	扎	扞	扣	扛	扠	扨	扼
14B0	抂	抉	找	抒	抓	抖	拔	抃	抔	拗	拑	抻	拏	拿	拆	擔
14C0	拈	拜	拌	拊	拂	拇	抛	拉	挌	拮	拱	挧	挂	挈	拯	拵
14D0	捐	挾	捍	搜	捏	掖	掎	掀	掫	捶	掣	掏	掉	掟	掵	捫
14E0	捩	掾	揩	揀	揆	揣	揉	插	揶	揄	搖	搴	搆	搓	搦	搶
14F0	攝	搗	搨	搏	摧	摯	摶	摎	攪	撕	撓	撥	撩	撈	撼	
1500		髻	鬆	鬘	鬚	鬟	鬢	鬣	鬥	鬧	鬨	鬩	鬪	鬮	鬯	鬲
1510	魄	魃	魏	魍	魎	魑	魘	魴	鮓	鮃	鮑	鮖	鮗	鮟	鮠	鮨
1520		據	擒	擅	擇	撻	擘	擂	擱	擧	舉	擠	擡	抬	擣	擯
1530	攬	擶	擴	擲	擺	攀	擽	攘	攜	攅	攤	攣	攫	攴	攵	攷
1540	收	攸	畋	效	敖	敕	敍	敘	敞	敝	敲	數	斂	斃	變	斛
1550	斟	斫	斷	旃	旆	旁	旄	旌	旒	旛	旙	无	旡	旱	杲	昊
1560	昃	旻	杳	昵	昶	昴	昜	晏	晄	晉	晁	晞	晝	晤	晧	晨
1570	晟	晢	晰	暃	暈	暎	暉	暄	暘	暝	曁	暹	曉	暾	暼	
1580		鵝	鷙	鵤	鵑	鵐	鵙	鵲	鶉	鶇	鶫	鵯	鵺	鶚	鶤	鶩
1590	鶲	鷄	鷁	鶻	鶸	鶺	鷆	鷏	鷂	鷙	鷓	鷸	鷦	鷭	鷯	鷽
15A0		曄	暸	曖	曚	曠	昿	曦	曩	曰	曵	曷	朏	朖	朞	朦
15B0	朧	霸	朮	朿	朶	杁	朸	朷	杆	杞	杠	杙	杣	杤	枉	杰
15C0	枩	杼	杪	枌	枋	枦	枡	枅	枷	柯	枴	柬	枳	柩	枸	柤
15D0	柞	柝	柢	柮	枹	柎	柆	柧	檜	栞	框	栩	桀	桍	栲	桎
15E0	梳	栫	桙	档	桷	桿	梟	梏	梭	梔	條	梛	梃	檮	梹	桴
15F0	梵	梠	梺	椏	梍	桾	椁	棊	椈	棘	椢	椦	棡	椌	棍	
1600		彝	槇	遙	瑤	凜	熙									
1610																
1620		棔	棧	棕	椶	椒	椄	棗	棣	椥	棹	棠	棯	椨	椪	椚
1630	椣	椡	棆	楹	楷	楜	楸	楫	楔	楾	楮	椹	楴	椽	楙	椰
1640	楡	楞	楝	榁	楪	榲	榮	槐	榿	槁	槓	榾	槎	寨	槊	槝
1650	榻	槃	榧	樮	榑	榠	榜	榕	榴	槞	槨	樂	樛	槿	權	槹
1660	槲	槧	樅	榱	樞	槭	樔	槫	樊	樒	櫁	樣	樓	橄	樌	橲
1670	樶	橸	橇	橢	橙	橦	橈	樸	樢	檐	檍	檠	檄	檢	檣	
1680																
1690	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
16A0		檗	蘗	檻	櫃	櫂	檸	檳	檬	櫞	櫑	櫟	檪	櫚	櫪	櫻
16B0	欅	蘖	櫺	欒	欖	鬱	欟	欸	欷	盜	欹	飮	歇	歃	歉	歐
16C0	歙	歔	歛	歟	歡	歸	歹	歿	殀	殄	殃	殍	殘	殕	殞	殤
16D0	殪	殫	殯	殲	殱	殳	殷	殼	毆	毋	毓	毟	毬	毫	毳	毯
16E0	麾	氈	氓	气	氛	氤	氣	汞	汕	汢	汪	沂	沍	沚	沁	沛
16F0	汾	汨	汳	沒	沐	泄	泱	泓	沽	泗	泅	泝	沮	沱	沾	
1700		ぁ	あ	ぃ	い	ぅ	う	ぇ	え	ぉ	お	か	が	き	ぎ	く
1710	ぐ	け	げ	こ	ご	さ	ざ	し	じ	す	ず	せ	ぜ	そ	ぞ	た
1720		沺	泛	泯	泙	泪	洟	衍	洶	洫	洽	洸	洙	洵	洳	洒
1730	洌	浣	涓	浤	浚	浹	浙	涎	涕	濤	涅	淹	渕	渊	涵	淇
1740	淦	涸	淆	淬	淞	淌	淨	淒	淅	淺	淙	淤	淕	淪	淮	渭
1750	湮	渮	渙	湲	湟	渾	渣	湫	渫	湶	湍	渟	湃	渺	湎	渤
1760	滿	渝	游	溂	溪	溘	滉	溷	滓	溽	溯	滄	溲	滔	滕	溏
1770	溥	滂	溟	潁	漑	灌	滬	滸	滾	漿	滲	漱	滯	漲	滌	

1780		ァ	ア	ィ	イ	ゥ	ウ	ェ	エ	ォ	オ	カ	ガ	キ	ギ	ク
1790	グ	ケ	ゲ	コ	ゴ	サ	ザ	シ	ジ	ス	ズ	セ	ゼ	ソ	ゾ	タ
17A0		漾	漓	滷	澆	潺	潸	澁	澀	潯	潛	濳	潭	澂	潼	潘
17B0	澎	澑	濂	潦	澳	澣	澡	澤	澹	濆	澪	濟	濕	濬	濔	濘
17C0	濱	濮	濛	瀉	瀋	濺	瀑	瀁	瀏	濾	瀛	瀚	潴	瀝	瀘	瀟
17D0	瀰	瀾	瀲	灑	灣	炙	炒	炯	烱	炬	炸	炳	炮	烟	烋	烝
17E0	烙	焉	烽	焜	焙	煥	煕	熈	煦	煢	煌	煖	煬	熏	燻	熄
17F0	熕	熨	熬	燗	熹	熾	燒	燉	燔	燎	燠	燬	燧	燵	燼	
1800	雯	霑	霏	霖	霙	霤	霪	霰	霹	霽	霾	靄	靆	靈	靂	靉
1810	靜	靠	靤	靦	靨	勒	靫	靱	靹	鞅	靼	鞁	靺	鞆	鞋	鞏
1820		燹	燿	爍	爐	爛	爨	爭	爬	爰	爲	爻	爼	爿	牀	牆
1830	牋	牘	牴	牾	犂	犁	犇	犒	犖	犢	犧	犹	犲	狃	狆	狄
1840	狎	狒	狢	狠	狡	狹	狷	倏	猗	猊	猜	猖	猝	猴	猯	猩
1850	猥	猾	獎	獏	默	獗	獪	獨	獰	獸	獵	獻	獺	珈	玳	珎
1860	玻	珀	珥	珮	珞	璢	琅	瑯	琥	珸	琲	琺	瑕	琿	瑟	瑙
1870	瑁	瑜	瑩	瑰	瑣	瑪	瑶	瑾	璋	璞	璧	瓊	瓏	瓔	珱	
1880	饑	饒	饌	饕	馗	馘	馥	馭	馮	馼	駟	駛	駝	駘	駑	駭
1890	駮	駱	駲	駻	駸	騁	騏	騅	駢	騙	騫	騷	驅	驂	驀	驃
18A0		瓠	瓣	瓧	瓩	瓮	瓲	瓰	瓱	瓸	瓷	甄	甃	甅	甌	甎
18B0	甍	甕	甓	甞	甦	甬	甼	畄	畍	畊	畉	畛	畆	畚	畩	畤
18C0	畧	畫	畭	畸	當	疆	疇	畴	疊	疉	疂	疔	疚	疝	疥	疣
18D0	痂	疳	痃	疵	疽	疸	疼	疱	痍	痊	痒	痙	痣	痞	痾	痿
18E0	痼	瘁	痰	痺	痲	痳	瘋	瘍	瘉	瘟	瘧	瘠	瘡	瘢	瘤	瘴
18F0	瘰	瘻	癇	癈	癆	癜	癘	癡	癢	癨	癩	癪	癧	癬	癰	
1900	鮴	鯀	鯊	鮹	鯆	鯏	鯑	鯒	鯣	鯢	鯤	鯔	鯡	鰺	鯲	鯱
1910	鯰	鰕	鰔	鰉	鰓	鰌	鰆	鰈	鰒	鰊	鰄	鰮	鰛	鰥	鰤	鰡
1920		癲	癶	癸	發	皀	皃	皈	皋	皎	皖	皓	皙	皚	皰	皴
1930	皸	皹	皺	盂	盍	盖	盒	盞	盡	盥	盧	盪	蘯	盻	眈	眇
1940	眄	眩	眤	眞	眥	眦	眛	眷	眸	睇	睚	睨	睫	睛	睥	睿
1950	睾	睹	瞎	瞋	瞑	瞠	瞞	瞰	瞶	瞹	瞿	瞼	瞽	瞻	矇	矍
1960	矗	矚	矜	矣	矮	矼	砌	砒	礦	砠	礪	硅	碎	硴	碆	硼
1970	碚	碌	碣	碵	碪	碯	磑	磆	磋	磔	碾	碼	磅	磊	磬	
1980	鷭	鶴	鸞	鹵	鹹	鹽	麁	麈	麋	麌	麒	麕	麑	麝	麥	麩
1990	麸	麪	麭	靡	黌	黎	黏	黐	黔	黜	點	黝	黠	黥	黨	黯
19A0		磧	磚	磽	磴	礇	礒	礑	礙	礬	礫	祀	祠	祗	祟	祚
19B0	祕	祓	祺	祿	禊	禝	禧	齋	禪	禮	禳	禹	禺	秉	秕	秧
19C0	秬	秡	秣	稈	稍	稘	稙	稠	稟	禀	稱	稻	稾	稷	穃	穗
19D0	穉	穡	穢	穩	龝	穰	穹	穽	窈	窗	窕	窘	窖	窩	竈	窰
19E0	窶	竅	竄	窿	邃	竇	竊	竍	竏	竕	竓	站	竚	竝	竡	竢
19F0	竦	竭	竰	笂	笏	笊	笆	笳	笘	笙	笞	笵	笨	笶	筐	
1A00																
1A10																
1A20		筺	笄	筍	笋	筌	筅	筵	筥	筴	筧	筰	筱	筬	筮	箝
1A30	箘	箟	箍	箜	箚	箋	箒	箏	筝	箙	篋	篁	篌	篏	箴	篆
1A40	篝	篩	簑	簔	篦	篥	籠	簀	簇	簓	篳	篷	簗	簍	篶	簣
1A50	簧	簪	簟	簷	簫	簽	籌	籃	籔	籏	籀	籐	籘	籟	籤	籖
1A60	籥	籬	籵	粃	粐	粤	粭	粢	粫	粡	粨	粳	粲	粱	粮	粹
1A70	粽	糀	糅	糂	糘	糒	糜	糢	鬻	糯	糲	糴	糶	糺	紆	
1A80		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
1A90	P	Q	R	S	T	U	V	W	X	Y	Z					
1AA0		紂	紜	紕	紊	絅	絋	紮	紲	紿	紵	絆	絳	絖	絎	絲
1AB0	絨	絮	絏	絣	經	綉	絛	綏	絽	綛	綺	綮	綣	綵	緇	綽
1AC0	綫	總	綢	綯	緜	綸	綟	綰	緘	緝	緤	緞	緻	緲	緡	縅
1AD0	縊	縣	縡	縒	縱	縟	縉	縋	縢	繆	繦	縻	縵	縹	繃	縷
1AE0	縲	縺	繧	繝	繖	繞	繙	繚	繹	繪	繩	繼	繻	纃	緕	繽
1AF0	辮	繿	纈	纉	續	纒	纐	纓	纔	纖	纎	纛	纜	缸	缺	





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11.2. Half-Size Font Pattern

11.2.1. Bank 0

11.2.2. Bank 1

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12. ELECTRICAL SPECIFICATIONS

12.1. Absolute Maximum Rating

Characteristics	Symbol	Value
Power supply voltage(1)	VCC	-0.3V to +4.0V
Power supply voltage(2)	V_{LCD}-GND	-0.3V to +14.0V
Input voltage	V_T	-0.3V to VCC+0.3V
Operating temperature	T_{OPR}	-40℃ to +85℃
Storage temperature	T_{STG}	-55℃ to +110℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

12.2. DC Characteristics (VCC = 2.0V - 3.6V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test condition
		Min.	Typ.	Max.		
Input high voltage	V_{IH}	0.8VCC	-	VCC	V	Pure input pin, I/O pin
Input low voltage	V_{IL}	0	-	0.15VCC	V	
Output high voltage	V_{OH1}	0.75VCC	-	-	V	I_{OH} = -0.4mA @ 3.0V (SDA, DB7 - 0 pin)
Output low voltage	V_{OL1}	-	-	0.2VCC	V	I_{OL} = 0.4mA @ 3.0V (SDA, DB7 - 0 pin)
Output high voltage	V_{OH2}	0.7VCC	-	-	V	I_{OH} = -3.0μA @ 3.0V (KST3 - 0 pin)
Output low voltage	V_{OL2}	-	-	0.2VCC	V	I_{OL} = 1.0mA @ 3.0V (KST3 - 0 pin)
Output high voltage	V_{OH3}	0.75VCC	-		V	I_{OH} = -0.4mA @ 3.0V (PORT2 - 0 pin)
Output low voltage	V_{OL3}	-	-	0.2VCC	V	I_{OL} = 0.4mA @ 3.0V (PORT2 - 0 pin)
Pull-up MOS current	$-I_P$	-	3.0	-	μA	VCC = 3.0V, V_{IN} = 0 (DB7 - 0, SDA pin)
Driver ON resistance	R_{ON}	-	3.0	20	KΩ	±I_D = 50μA, V_{LCD} = 6.0V (com, seg pin)
Current consumption during normal	I_{OP}	-	100	-	μA	VCC = 3.6V, F_{OSC} = 100KHz (VCC ----- GND)
Current consumption during sleep	I_{SL}	-	30	-	μA	F_{OSC} = 100KHz VCC = 3.6V
Current consumption during standby	I_{ST}	-	-	3.0	μA	NO R-C oscillation VCC = 3.0V
LCD driver power supply current	I_{EE}	-	20		μA	V_{LCD} - GND = 8.0V, F_{OSC} = 60KHz, 1/7 bias V_{TEST3} = VCC
LCD driver voltage	V_{LCD}	4.5	-	12	V	V_{LCD} - GND

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12.3. AC Characteristics

12.3.1. Scan timing characteristics (VCC = 2.0V - 3.6V)

Characteristics	Symbol	Limit			Unit	Test condition
		Min.	Typ.	Max.		
Frame rate	t_{fr}	60	80	100	Hz	NL = 100, NC = 10, measure from com1

12.3.2. 68-system bus interface timing characteristics (VCC = 2.0V - 3.6V)

Characteristics	Symbol		Limit			Unit	Test condition
			Min.	Typ.	Max.		
Enable cycle time	Write Read	t_{CYCE}	800 1200	- -	- -	ns	
Enable high-level pulse width	Write Read	PW_{EH}	150 450	- -	- -	ns	
Enable low-level pulse width	Write Read	PW_{EL}	300 450	- -	- -	ns	
Enable rise/fall time	t_{Er},t_{Ef}		-	-	25	ns	
Setup time (RS, R/W to E, CSB)	t_{ASE}		50	-	-	ns	
Address hold time	t_{AHE}		20	-	-	ns	
Write data setup time	t_{DSWE}		60	-	-	ns	
Write data hold time	t_{HE}		20	-	-	ns	
Read data delay time	t_{DDRE}		-	-	400	ns	
Read data hold time	t_{DHRE}		5.0	-	-	ns	

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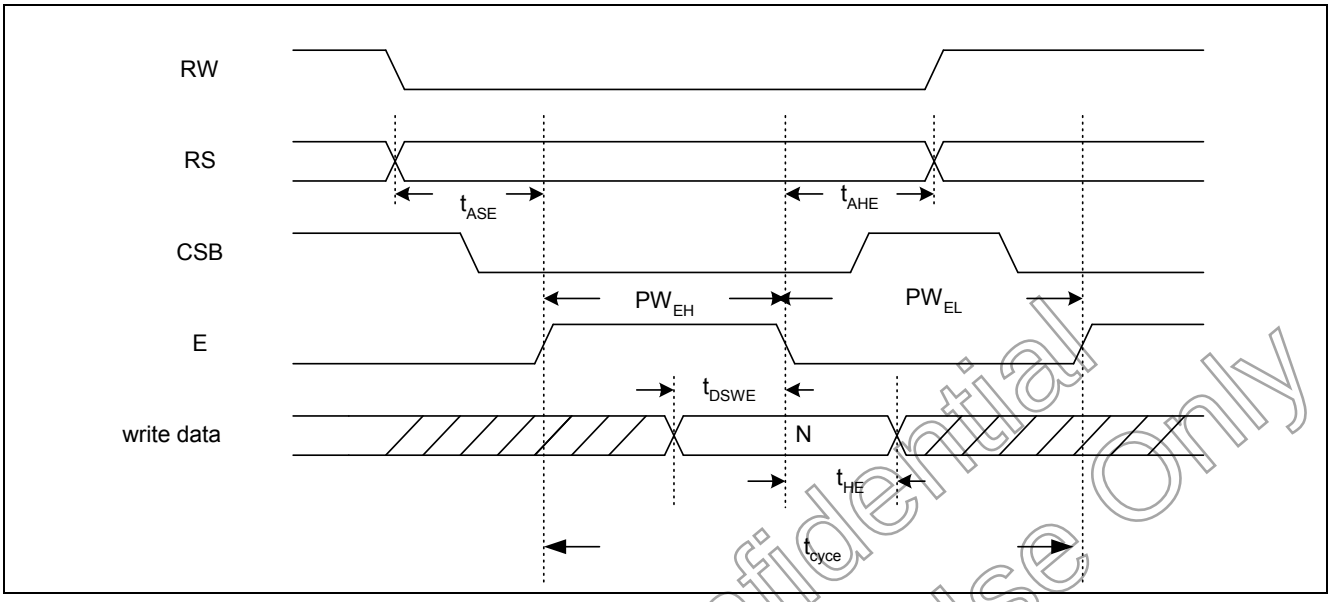
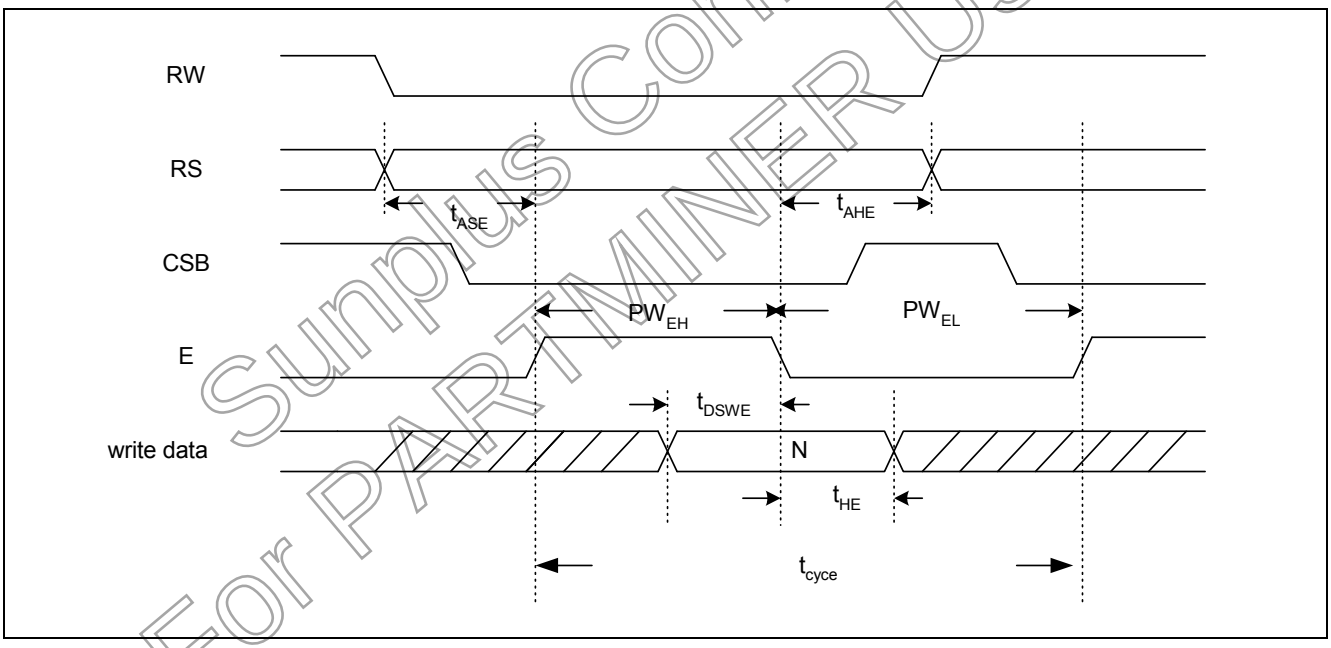
12.3.3. 68-system write timing (Address N Set First)





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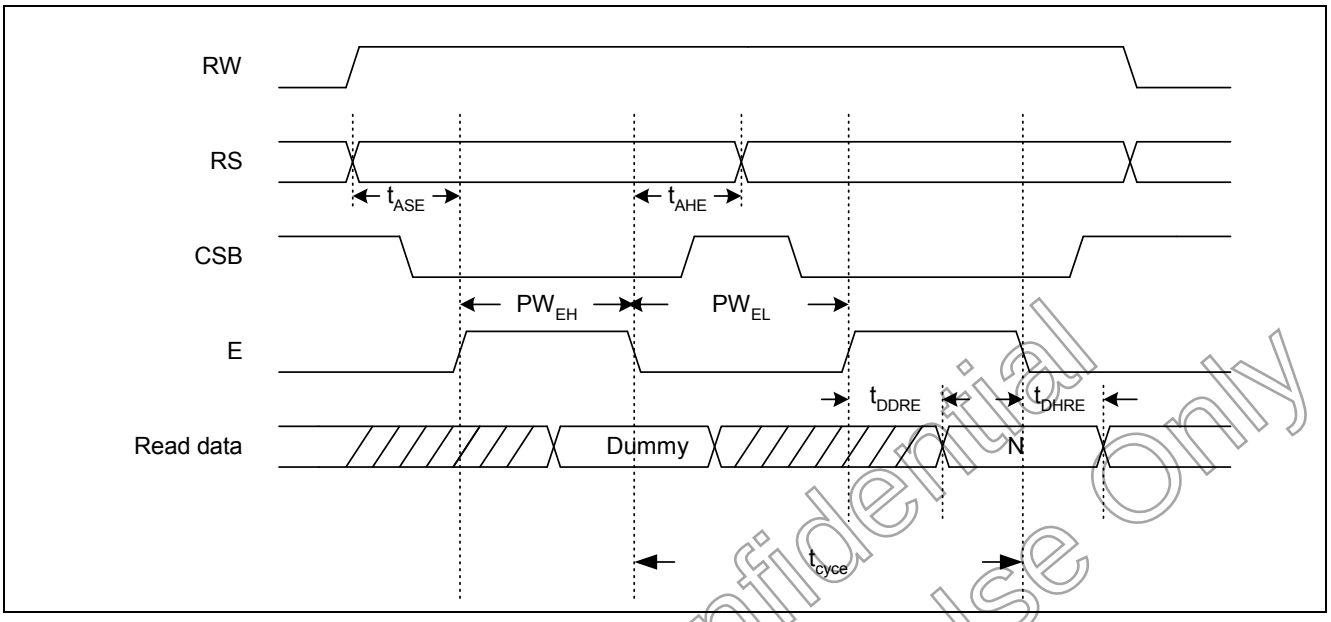
12.3.4. 68-system read timing (Address N Set First)



12.3.5. 80-system bus interface timing characteristics (VCC = 2.0V - 3.6V)

Characteristics	Symbol	Limit			Unit	Test condition
		Min.	Typ.	Max.		
Bus cycle time	Write t_{CYCE}	800	-	-	ns	
	Read	1200	-	-		
Write low-level pulse width	Write PW_{LW}	150	-	-	ns	
Read low-level pulse width	Read PW_{LR}	450	-	-		
Write high-level pulse width	Write PW_{HW}	300	-	-	ns	
Read high-level pulse width	Read PW_{HR}	450	-	-		
Enable rise/fall time	T_{WRr}, t_{WRf}	-	-	25	ns	
Setup time (RS to CSB, WRB, RDB)	t_{AS}	50	-	-	ns	
Address hold time	t_{AH}	20	-	-	ns	
Write data setup time	t_{DSW}	60	-	-	ns	
Write data hold time	t_H	20	-	-	ns	
Read data delay time	t_{DDR}	-	-	400	ns	
Read data hold time	t_{DHR}	5.0	-	-	ns	

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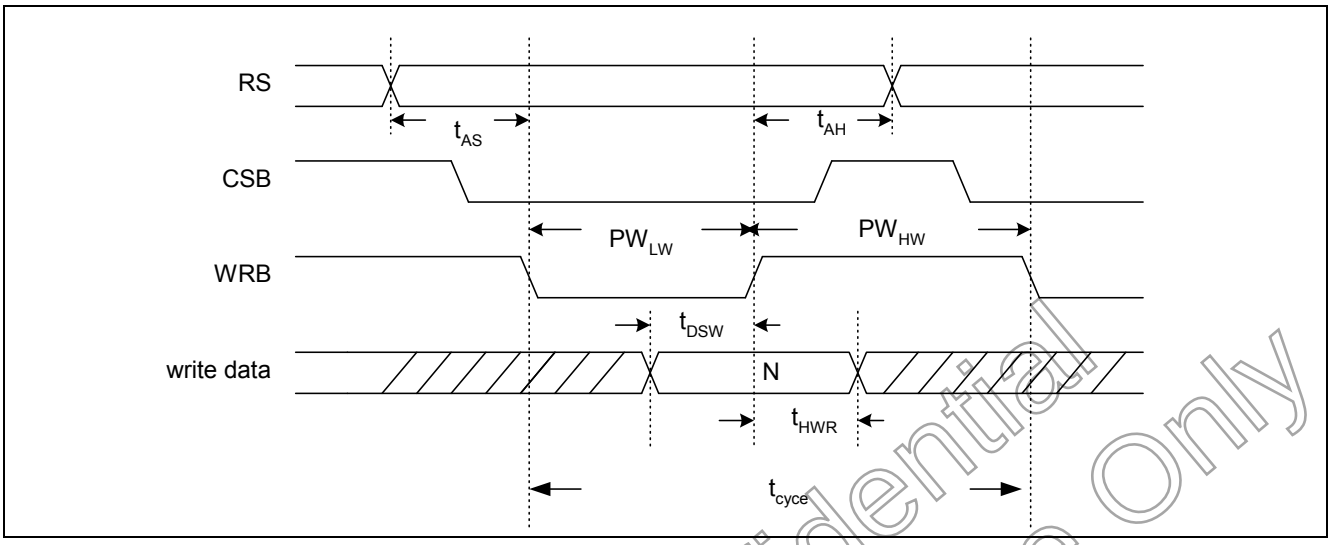
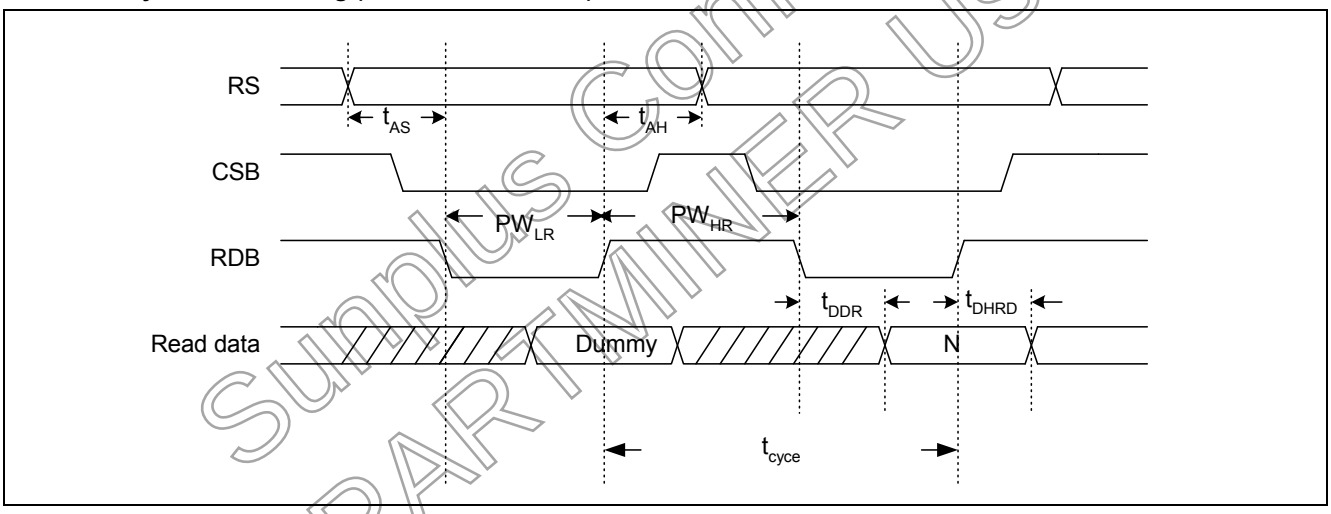
12.3.6. 80-system write timing (Address N Set First)



12.3.7. 80-system read timing (Address N Set First)



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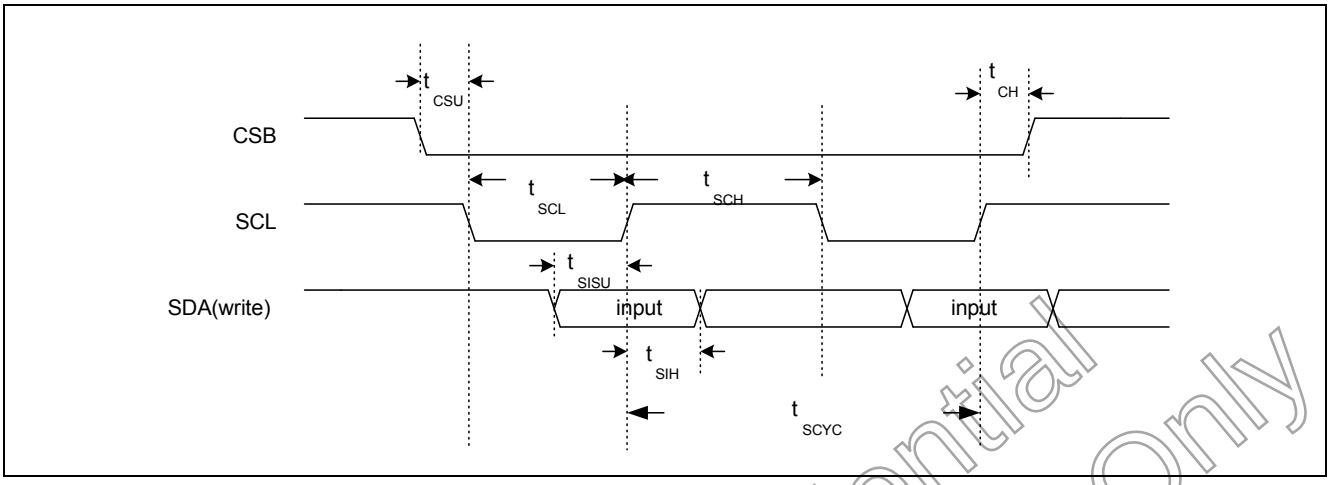
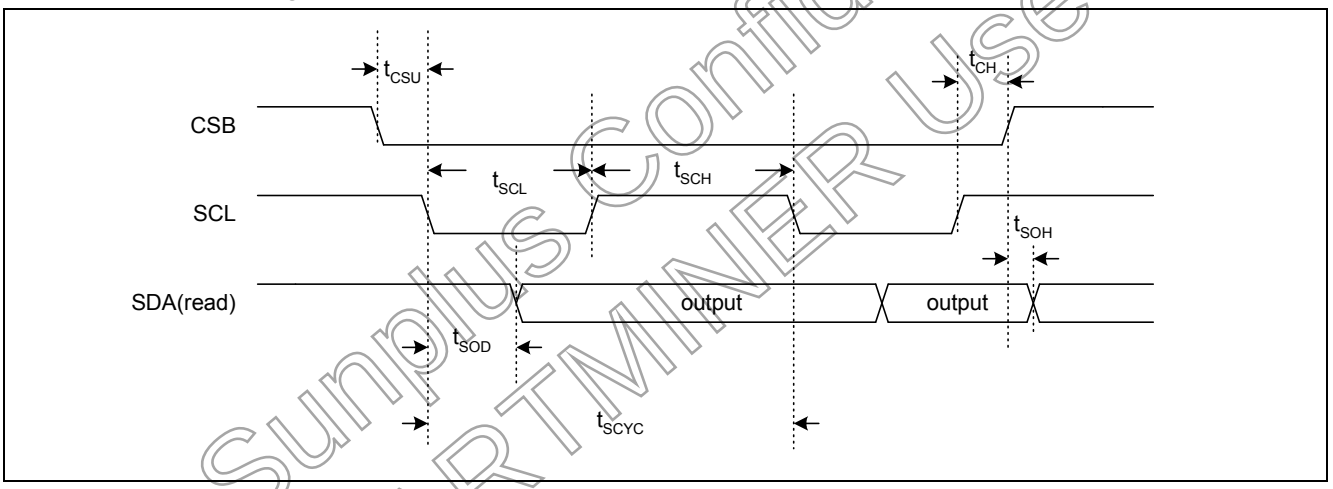
12.3.8. Clock-synchronized serial interface timing characteristics (VCC = 2.0V - 3.6V)

Characteristics	Symbol		Limit			Unit	Test condition
			Min.	Typ.	Max.		
Serial clock cycle time	Write Read	t_{SCYC}	0.5 1.0	- -	20 20	μs	
Clock high-level pulse width	Write Read	t_{SCH}	230 480	- -	- -	ns	
Clock low-level pulse width	Write Read	t_{SCL}	230 480	- -	- -	ns	
Serial clock rise/fall time	t_{SCr},t_{SCf}		-	-	25	ns	
Chip select setup time	t_{CSU}		60	-	-	ns	
Chip select hold time	t_{CH}		200	-	-	ns	
Serial input data setup time	t_{SISU}		100	-	-	ns	
Serial input data hold time	t_{SIH}		100	-	-	ns	
Serial output data delay time	t_{SOD}		-	-	400	ns	
Serial output data hold time	t_{SOH}		5.0	-	-	ns	

12.3.9. Serial write timing



12.3.10. Serial read timing



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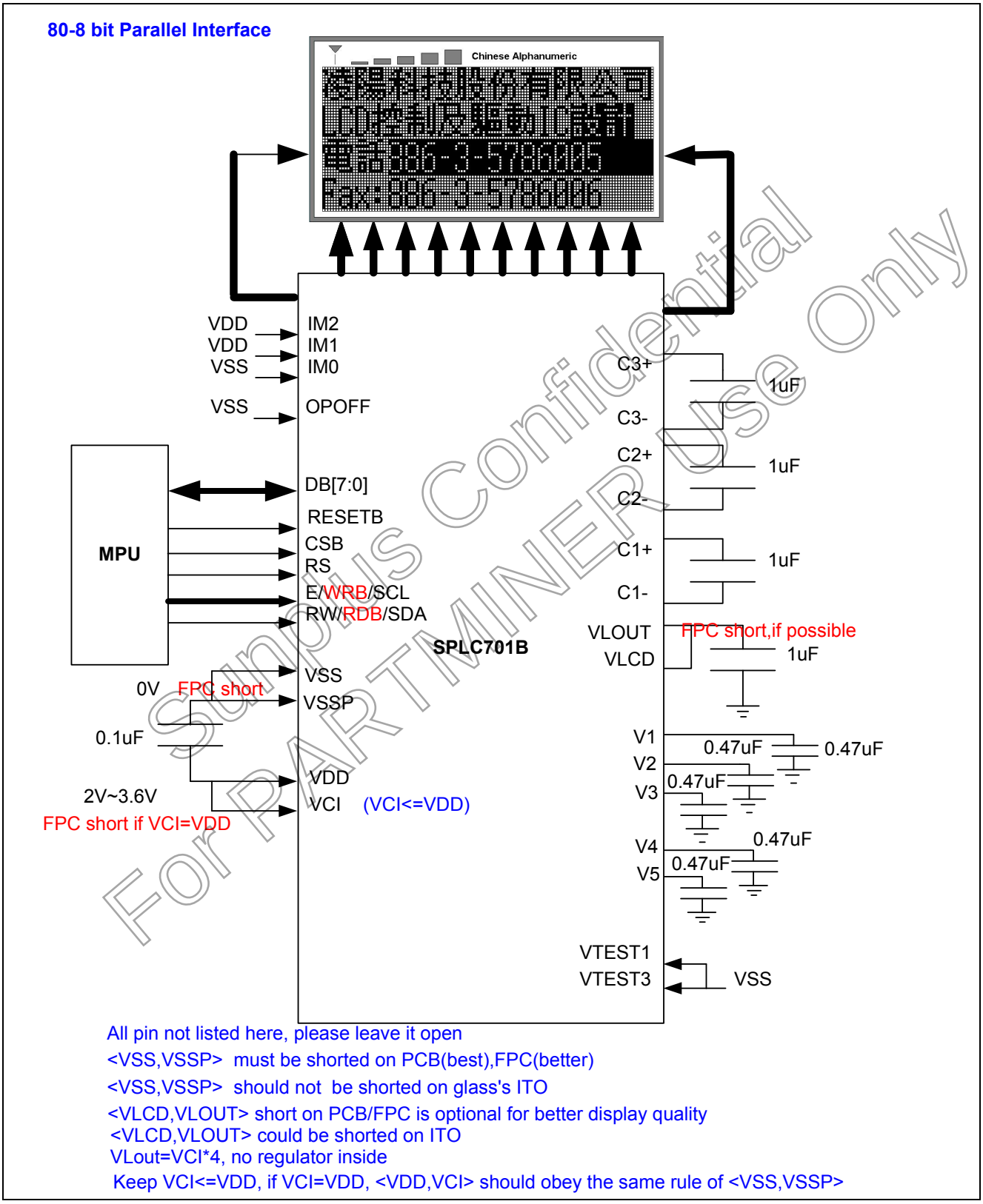
13. APPLICATION CIRCUITS

13.1. 80-8 bit Parallel Interface



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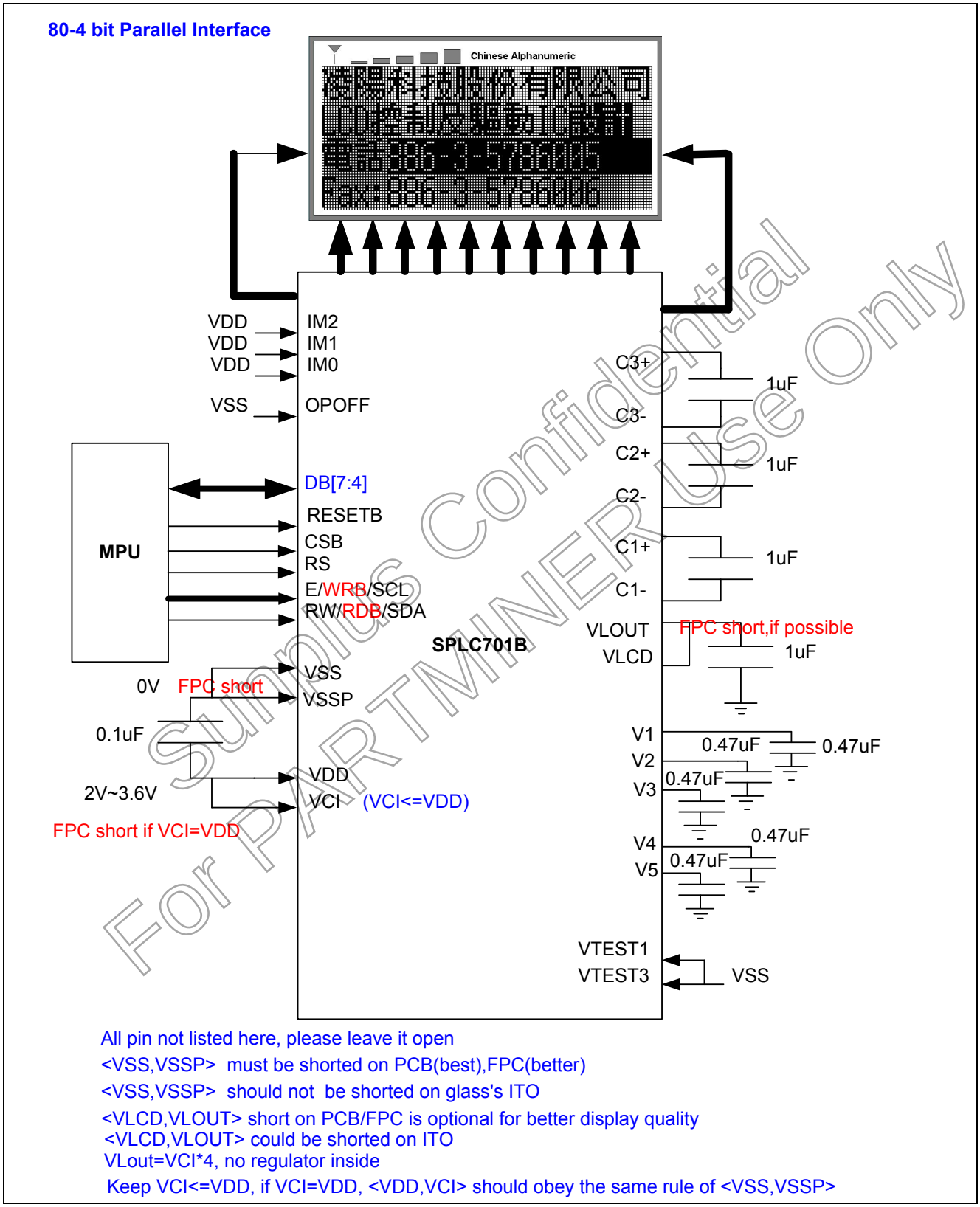
13.2. 80-4 bit Parallel Interface



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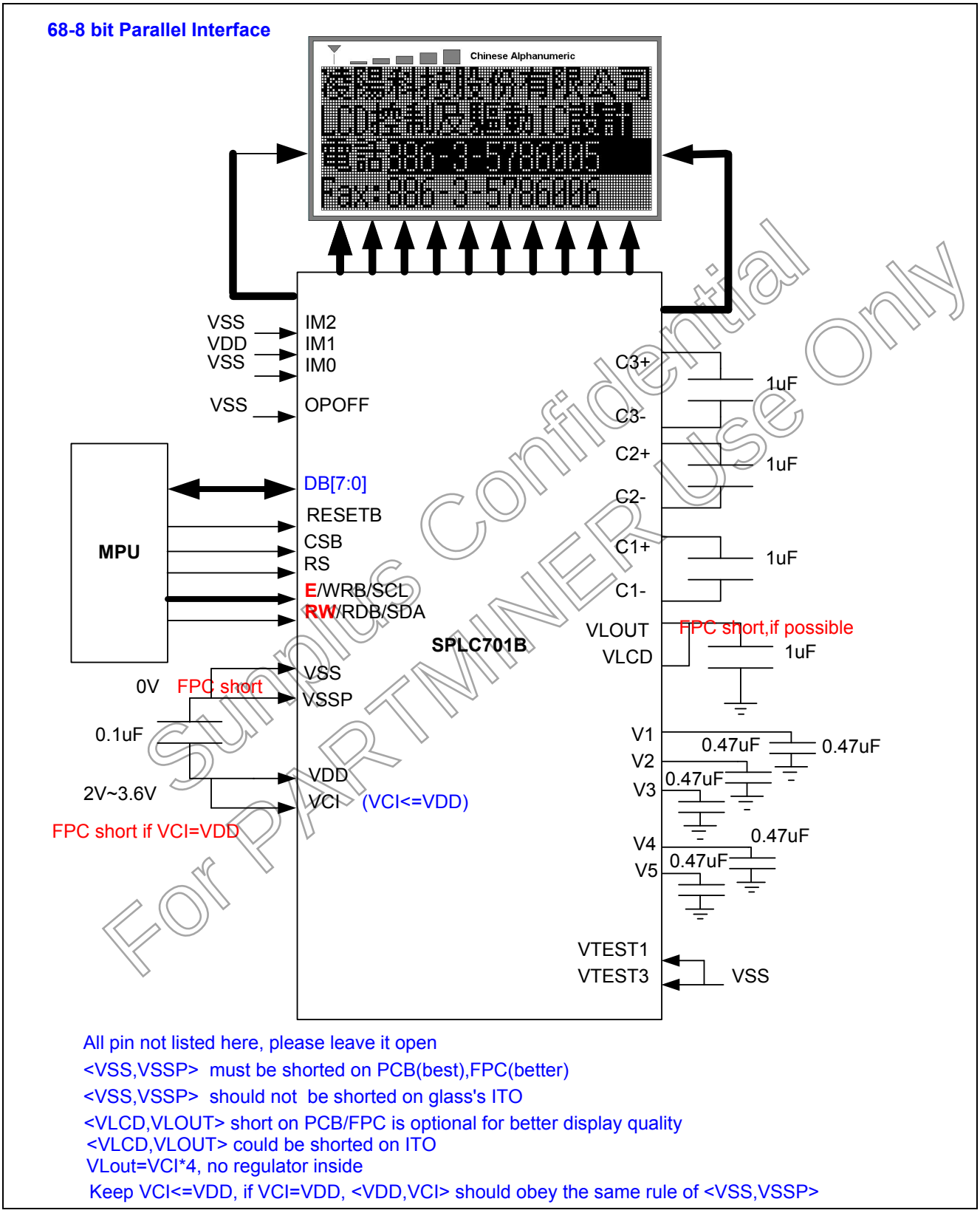
13.3. 68-8 bit Parallel Interface



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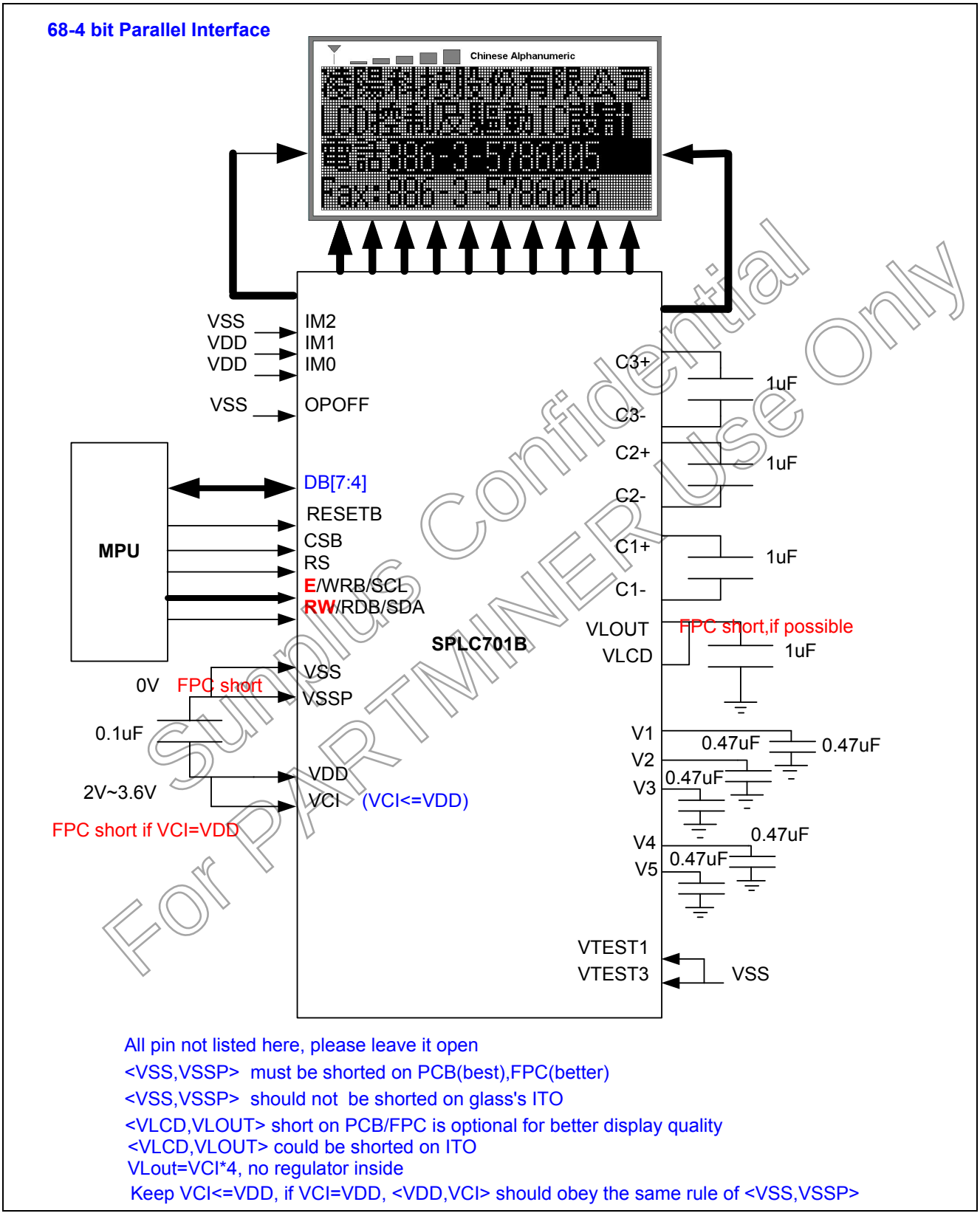
13.4. 68-4 bit Parallel Interface



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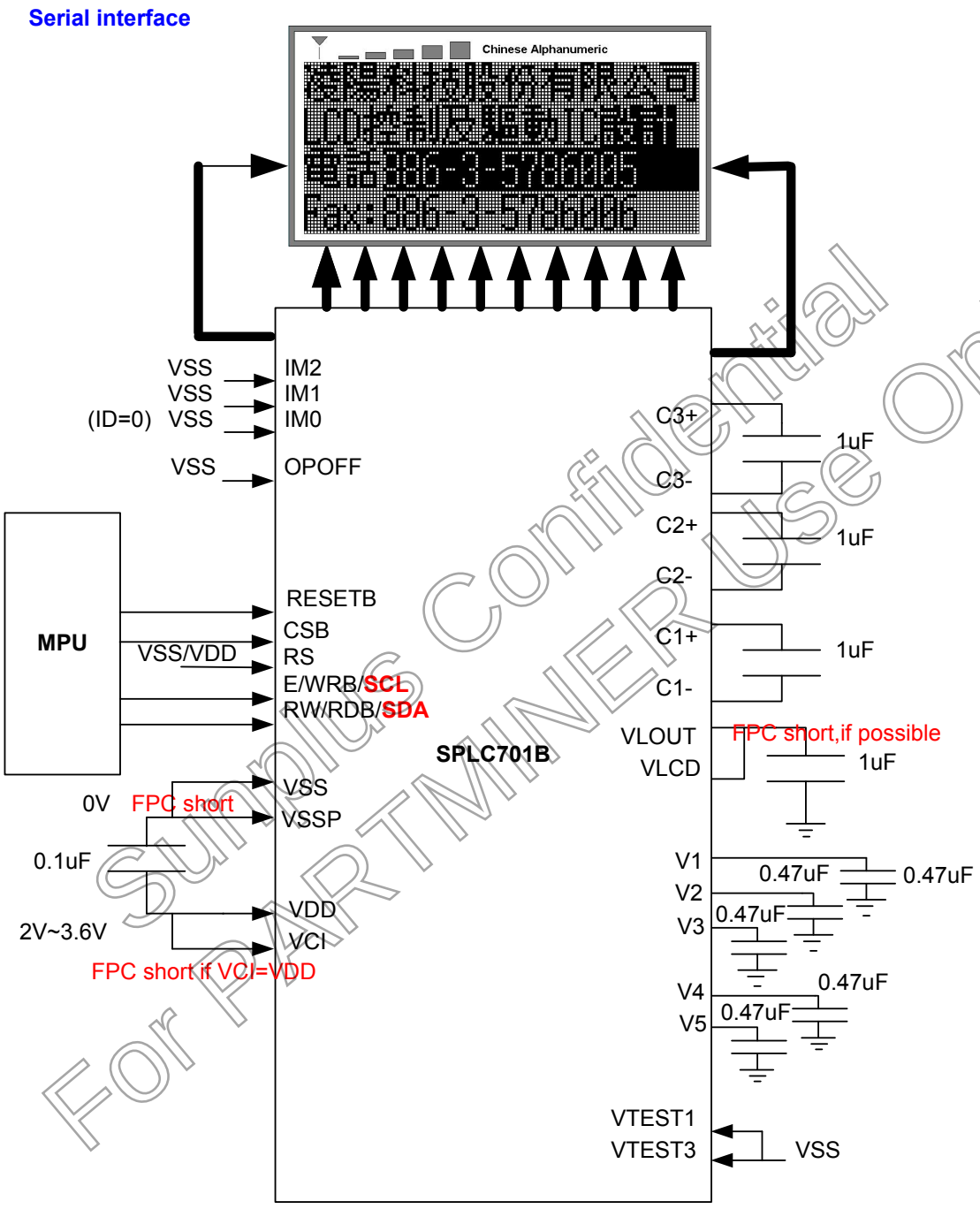
13.5. Serial Interface



All pin not listed here, please leave it open

<VSS,VSSP> must be shorted on PCB(best),FPC(better)

<VSS,VSSP> should not be shorted on glass's ITO

<VLCD,VLOUT> short on PCB/FPC is optional for better display quality

<VLCD,VLOUT> could be shorted on ITO

VLout=VCI*4, no regulator inside

Keep VCI<=VDD, if VCI=VDD, <VDD,VCI> should obey the same rule of <VSS,VSSP>

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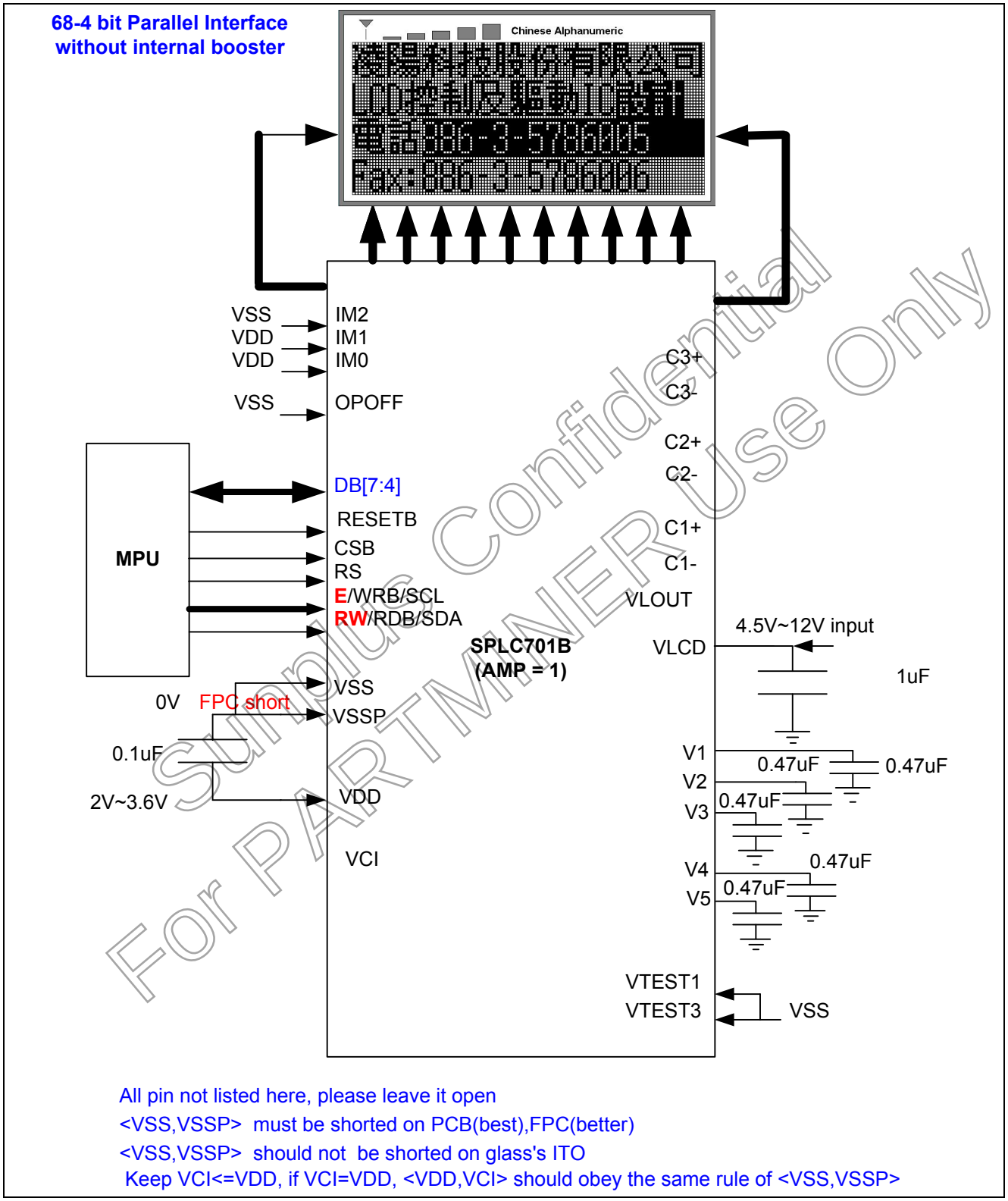
13.6. 68-4 bit without internal booster



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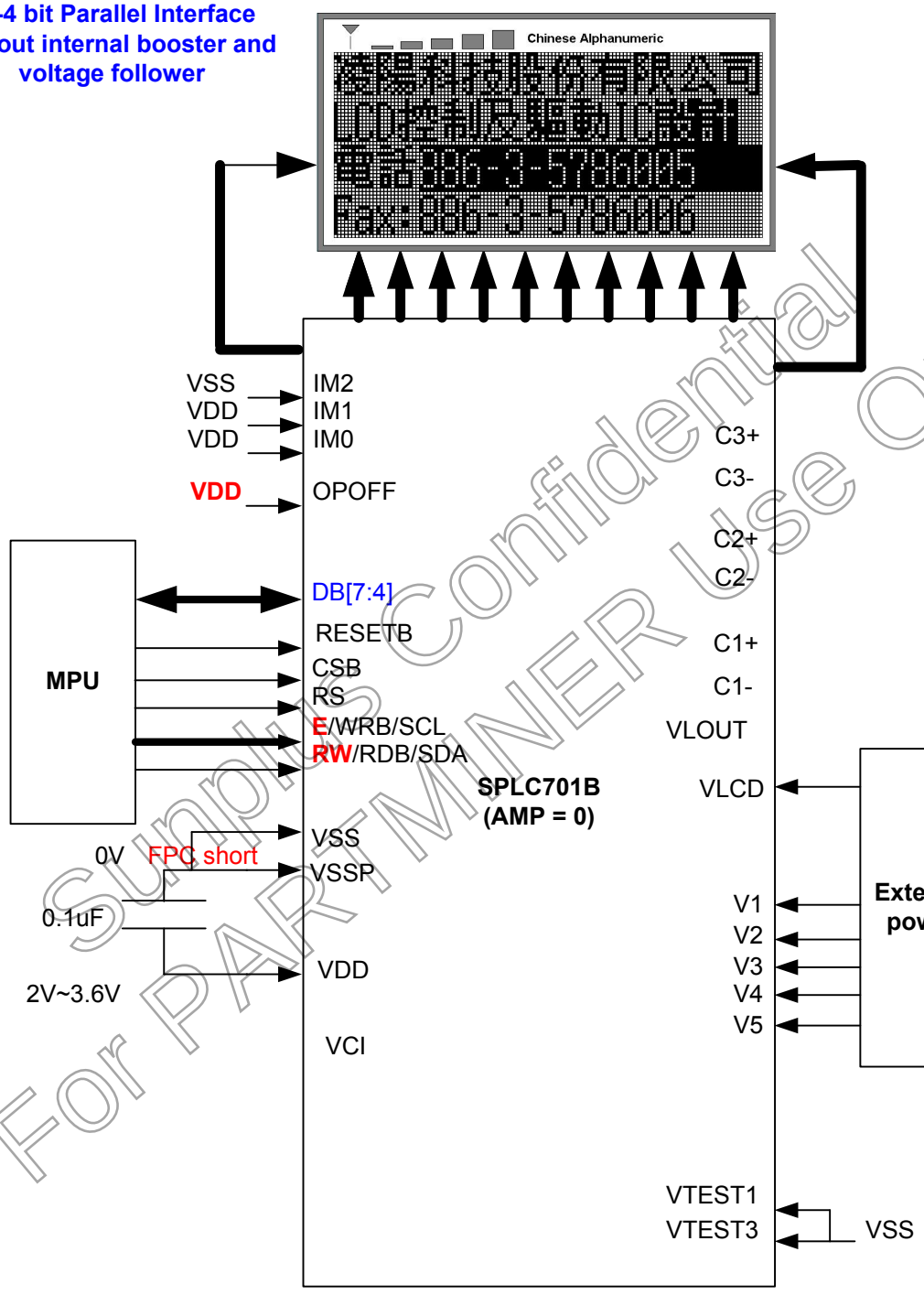
13.7. 68-4 bit without internal booster and voltage follower



All pin not listed here, please leave it open
<VSS,VSSP> must be shorted on PCB(best),FPC(better)
<VSS,VSSP> should not be shorted on glass's ITO

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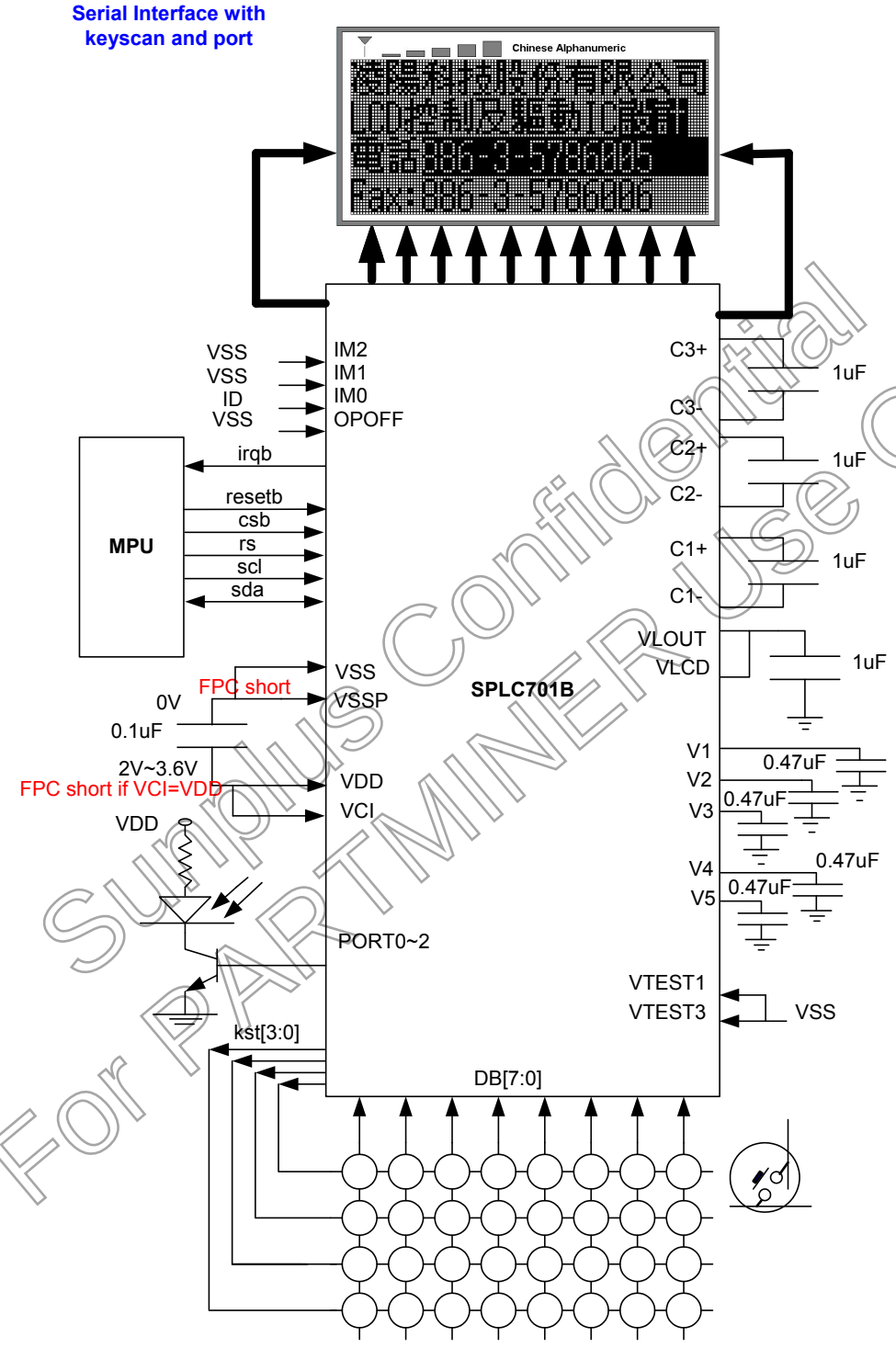
13.8. Serial Interface with keyscan and port



All pin not listed here, please leave it open

<VSS,VSSP> must be shorted on PCB(best),FPC(better)

<VSS,VSSP> should not be shorted on glass's ITO

<VLCD,VLOUT> short on PCB/FPC is optional for better display quality

<VLCD,VLOUT> could be shorted on ITO

VLout=VCI*4, no regulator inside

Keep VCI<=VDD, if VCI=VDD, <VDD,VCI> should obey the same rule of <VSS,VSSP>

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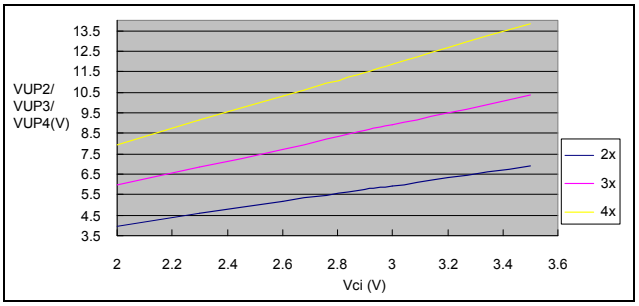
14. REFERENTIAL DATA

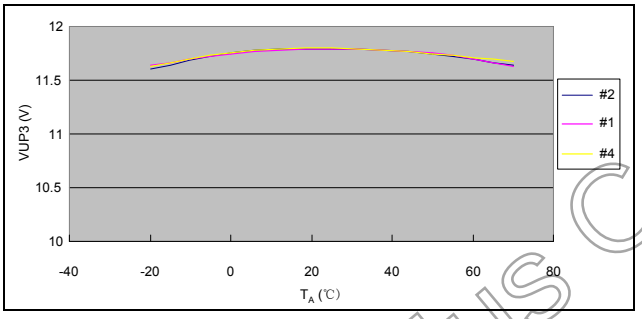
VUP2 = V_{LOUT} – GND; VUP3 = V_{LOUT} – GND; VUP4 = V_{LOUT} – GND

(1) Relation between the obtained voltage and input voltage



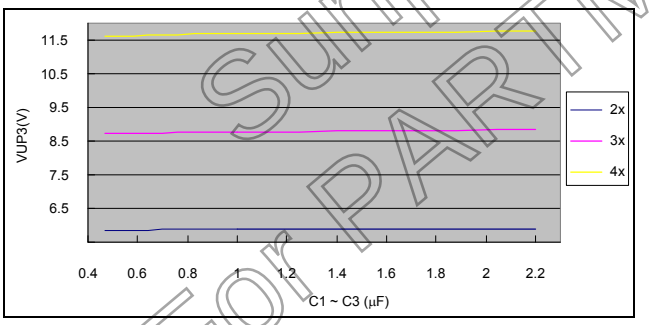
V_{CI} = VCC, fcp = 60 kHz, T_A = 25℃

(2) Relation between the obtained voltage and temperature



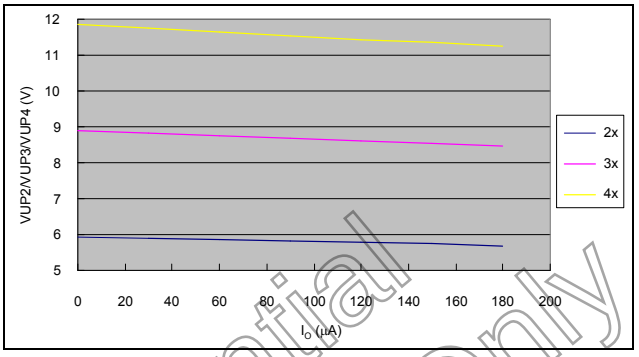
V_{CI} = VCC = 3.0V, fcp = 60 kHz, I_O = 50μA

(3) Relation between the obtained voltage and capacitance



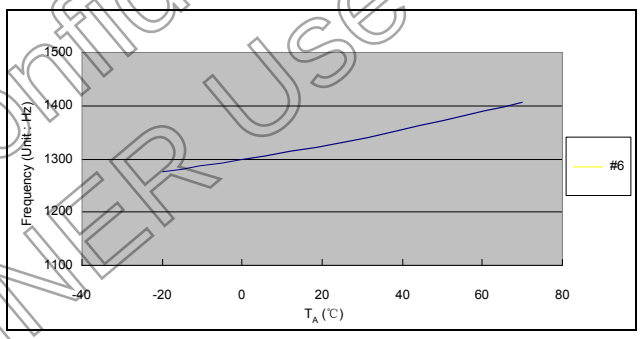
V_{CI} = VCC = 3.0V, f_{OSC} = 60 kHz, I_O = 50μA

(4) Relation between the obtained voltage and current



V_{CI} = VCC = 3.0V, f_{OSC} = 60 kHz, T_A = 25℃

(5) Relation between the Internal frequency & temperature



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15. PACKAGE/PAD LOCATIONS

15.1. Package/PAD Locations\

Please contact Sunplus sales representatives for more information.

15.2. Ordering Information

Product Number	Package Type
SPLC701B-NnnV-C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

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17. REVISION HISTORY

Date	Revision #	Description	Page
MAY. 17, 2005	1.5	Correct "*SIGNAL DESCRIPTIONS"*	8
MAR. 29, 2005	1.4	Change Resetb active wait time from 10ms to 1ms	33 - 35
JAN. 05, 2005	1.3	1. Add "*BLOCK DIAGRAM*" 2. Add "*REFERENTIAL DATA*" 3. Correct some typing error	38 63
JUN. 30, 2004	1.2	1. Updated "*SIGNAL DESCRIPTIONS*" 2. Add "*CODE INFORMATION*" 3. Updated "*APPLICATION CIRCUIT*" 4. Correct some typing error	
MAY. 28, 2003	1.1	1. Exchange IM[2], IM[1] 2. Remove "*13. PACKAGE/PAD LOCATIONS*"	8 54
FEB. 12, 2003	1.0	Original	

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