



SPN05T10

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN05T10 is the N-Channel logic enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. The SPN05T10 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

FEATURES

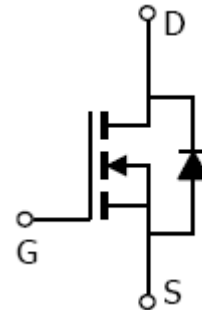
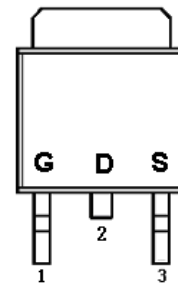
- ◆ 100V/2A, $R_{DS(ON)}=250m\Omega@V_{GS}=10V$
- ◆ 100V/1A, $R_{DS(ON)}=280m\Omega@V_{GS}=4.5V$
- ◆ High density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-252-2L package design

APPLICATIONS

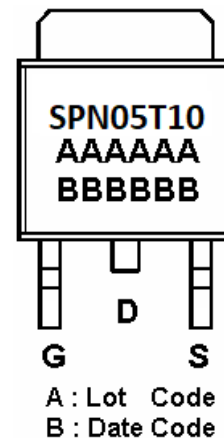
- High Frequency Small Power Switching for MB/NB/VGA
- Network DC/DC Power System
- Load Switch

PIN CONFIGURATION

TO-252-2L



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN05T10T252RGB	TO-252-2L	SPN05T10

※ SPN05T10T252RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

($T_A=25^{\circ}\text{C}$ Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V_{DSS}	100	V
Gate –Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current($T_J=150^{\circ}\text{C}$)	I_D	6	A
		4.6	
Pulsed Drain Current	I_{DM}	9	A
Power Dissipation	P_D	40	W
Operating Junction Temperature	T_J	-55/150	$^{\circ}\text{C}$
Storage Temperature Range	T_{STG}	-55/150	$^{\circ}\text{C}$
Thermal Resistance-Junction to Ambient	$R_{\theta JA}$	62	$^{\circ}\text{C}/\text{W}$



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ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	100			V	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	2.0	2.5	V	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=80V, V_{GS}=0V$			1	uA	
		$V_{DS}=80V, V_{GS}=0V$ $T_J=55^\circ C$			5		
On-State Drain Current	$I_{D(on)}$	$V_{DS}\geq 5V, V_{GS}=10V$	2.2			A	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=2A$		0.22	0.25	Ω	
		$V_{GS}=4.5V, I_D=1A$		0.25	0.28	Ω	
Forward Transconductance	g_{fs}	$V_{DS}=5V, I_D=2A$		2.4		S	
Diode Forward Voltage	V_{SD}	$I_S=1A, V_{GS}=0V$			1.2	V	
Dynamic							
Total Gate Charge	Q_g	$V_{DS}=50V, V_{GS}=10V$ $I_D=2A$		9	13	nC	
Gate-Source Charge	Q_{gs}			2			
Gate-Drain Charge	Q_{gd}			1.4			
Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V$ $f=1MHz$		508		pF	
Output Capacitance	C_{oss}			29			
Reverse Transfer Capacitance	C_{rss}			16.5			
Turn-On Time	$t_{d(on)}$	$V_{DD}=50V, I_D=2A,$ $V_{GEN}=10V, R_G=3.3\Omega$		2		nS	
	t_r			21.5			
Turn-Off Time	$t_{d(off)}$				11.2		
	t_f				18.8		



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