SPN09T10
N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN09T10 is the N-Channel logic enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. The SPN09T10 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

APPLICATIONS

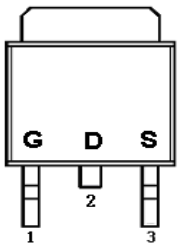
- Powered System
- DC/DC Converter
- Load Switch

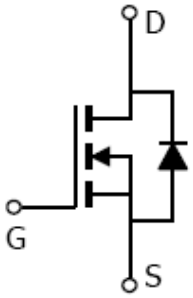
FEATURES

- 100V/8A,$R_{DS(ON)}$=160mΩ@ V_{GS}=10V
- High density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-252-2L package design

PIN CONFIGURATION

TO-252-2L





PART MARKING

SPN09T10
N-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN09T10T252RGB	TO-252-2L	SPN09T10

※ SPN09T10T252RGB : Tape Reel ; Pb – Free ; Halogen – Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_D	14	A
	T_A=70℃		9.0	
Pulsed Drain Current		I_{DM}	45	A
Avalanche Current		I_{AS}	14	A
Power Dissipation	T_A=25℃	P_D	40	W
Avalanche Energy with Single Pulse (Tj=25℃, L = 0.14mH , I_{AS} = 20A , V_{DD} = 20V.)		E_{AS}	28	mJ
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	100	℃/W

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ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	1		3	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=80V,V_{GS}=0V			25	uA
		V_{DS}=80V,V_{GS}=0V T_J=125℃			250	
On-State Drain Current	$I_{D(on)}$	V_{DS}≥5V,V_{GS}=10V	9			A
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=10A		0.110	0.160	Ω
Forward Transconductance	gfs	V_{DS}=10V,I_D=5A		5.6		S
Diode Forward Voltage	V_{SD}	I_S=9A,V_{GS}=0V			1.3	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=80V,V_{GS}=10V I_D=5A		10	16	nC
Gate-Source Charge	Q_{gs}			2.5		
Gate-Drain Charge	Q_{gd}			4.5		
Input Capacitance	C_{iss}	V_{DS}=25,V_{GS}=0V f=1MHz		430		pF
Output Capacitance	C_{oss}			56		
Reverse Transfer Capacitance	C_{rss}			35		
Turn-On Time	$t_{d(on)}$	V_{DD}=50V,R_L=10Ω I_D=5A,V_{GEN}=10V R_G=3.3Ω		6.5		nS
	t_r			10		
Turn-Off Time	$t_{d(off)}$			13		
	t_f			3.4		

TYPICAL CHARACTERISTICS

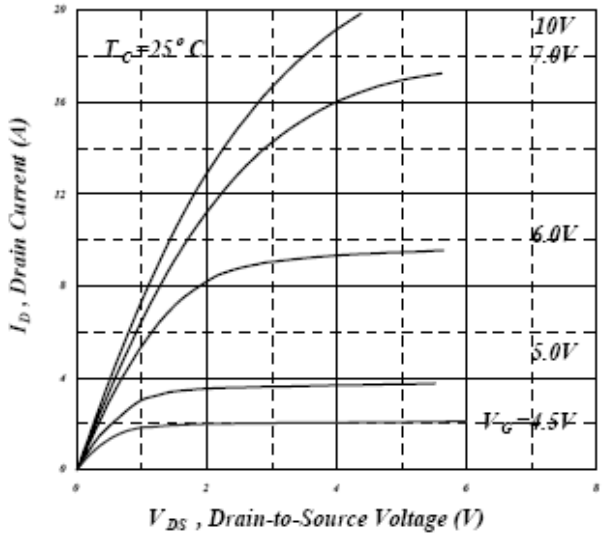

Fig 1. Typical Output Characteristics

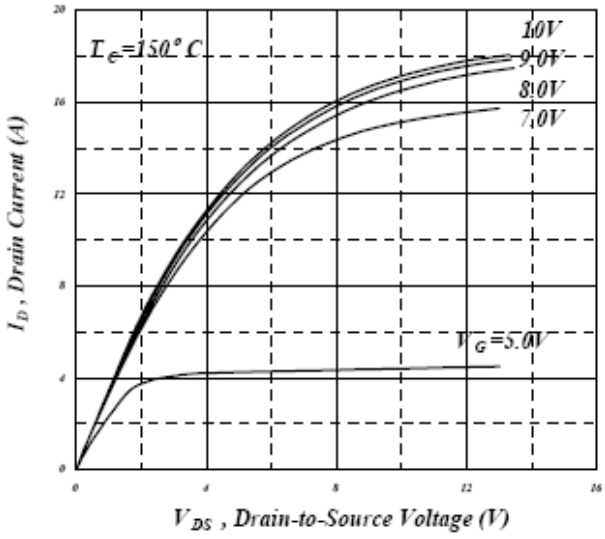

Fig 2. Typical Output Characteristics

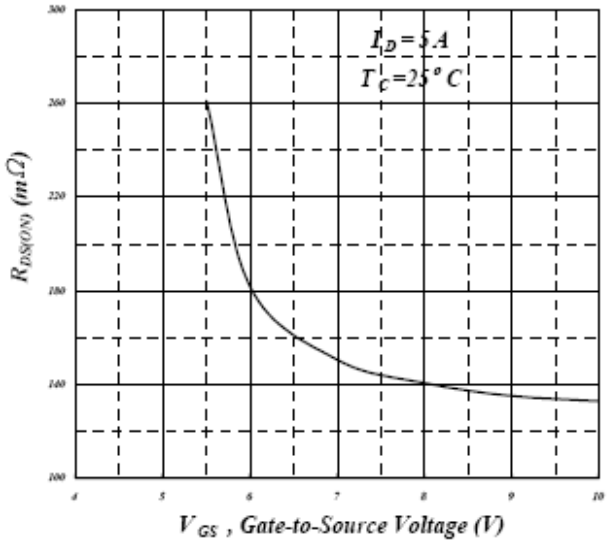

Fig 3. On-Resistance v.s. Gate Voltage

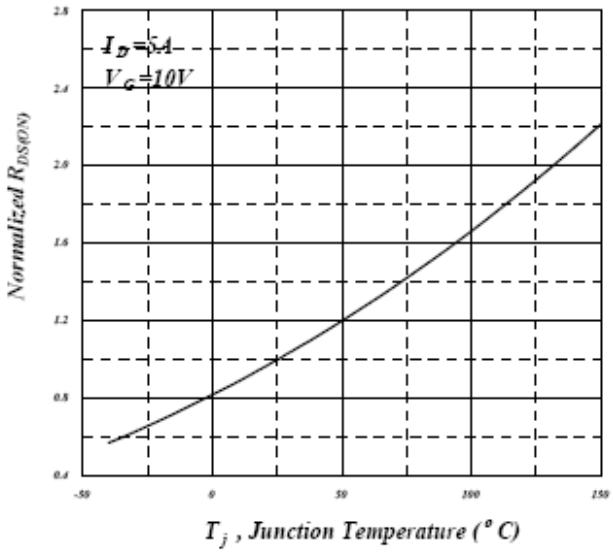

Fig 4. Normalized On-Resistance v.s. Junction Temperature

TYPICAL CHARACTERISTICS

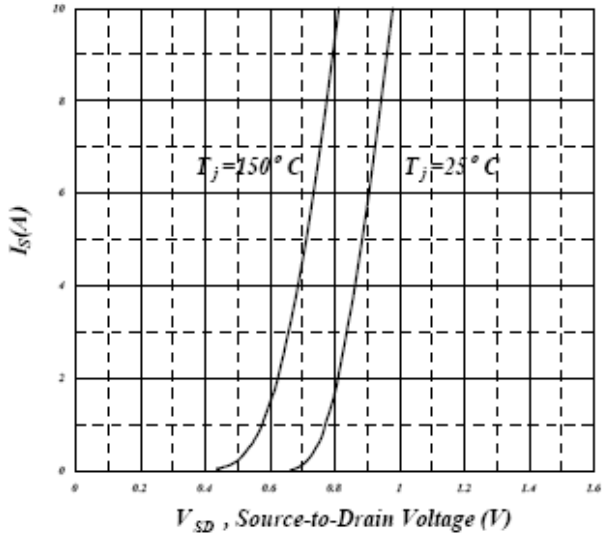

Fig 5. Forward Characteristic of Reverse Diode

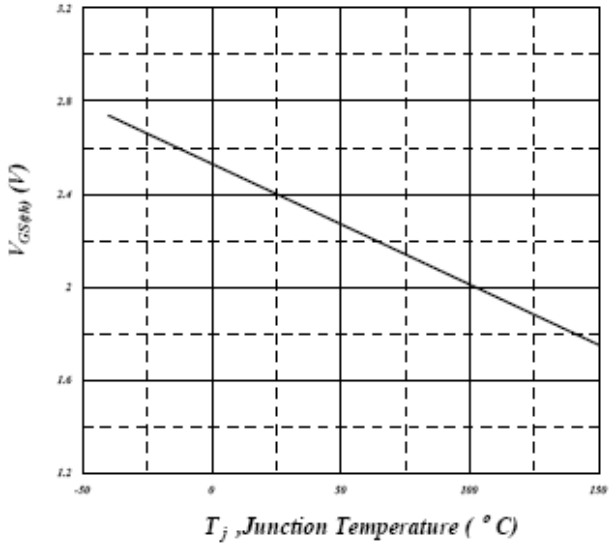

Fig 6. Gate Threshold Voltage v.s. Junction Temperature

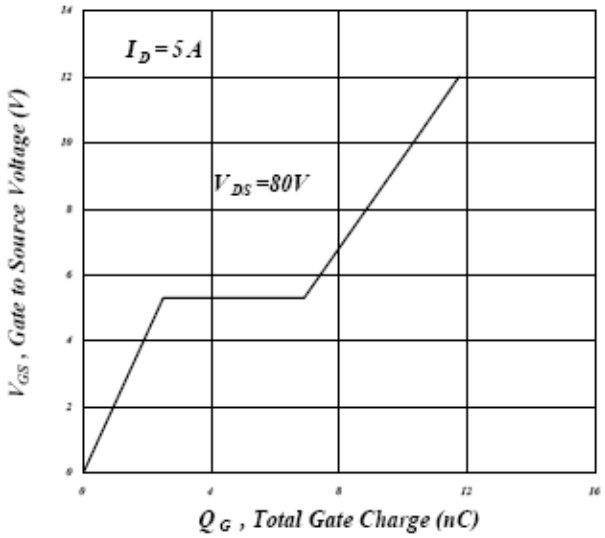

Fig 7. Gate Charge Characteristics

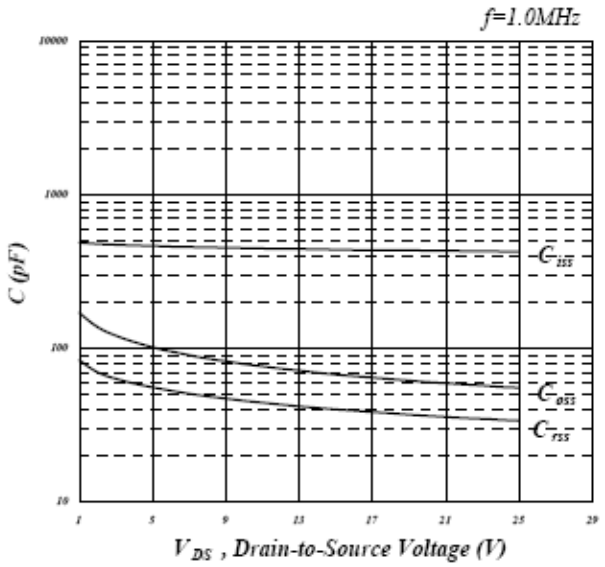

Fig 8. Typical Capacitance Characteristics

TYPICAL CHARACTERISTICS

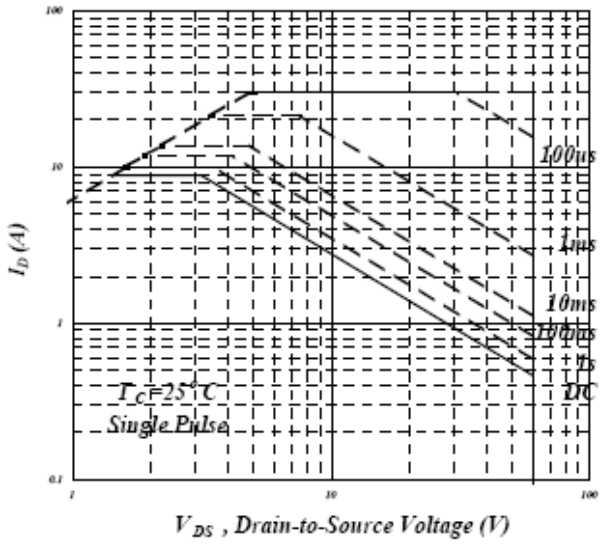

Fig 9. Maximum Safe Operating Area

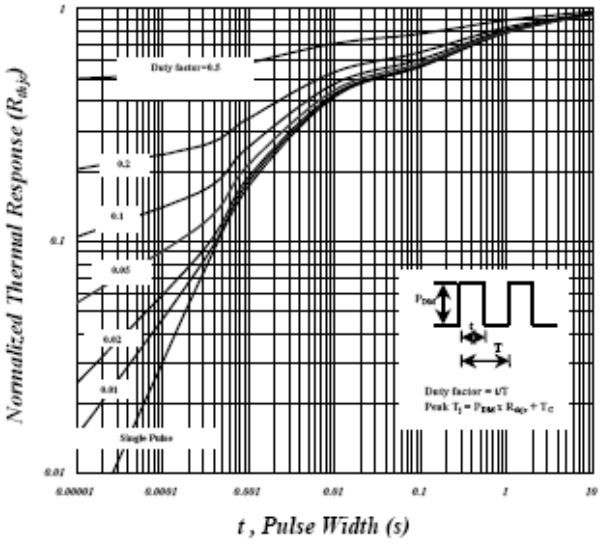

Fig 10. Effective Transient Thermal Impedance

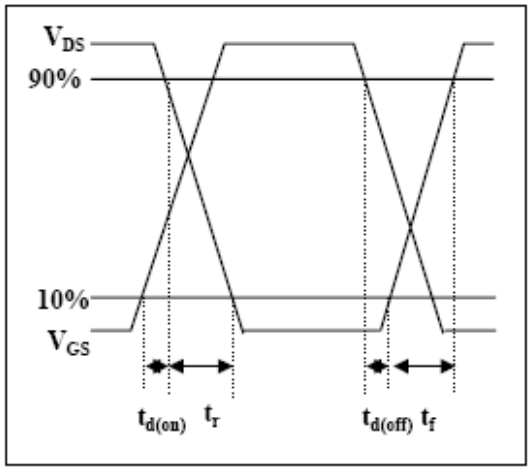

Fig 11. Switching Time Waveform

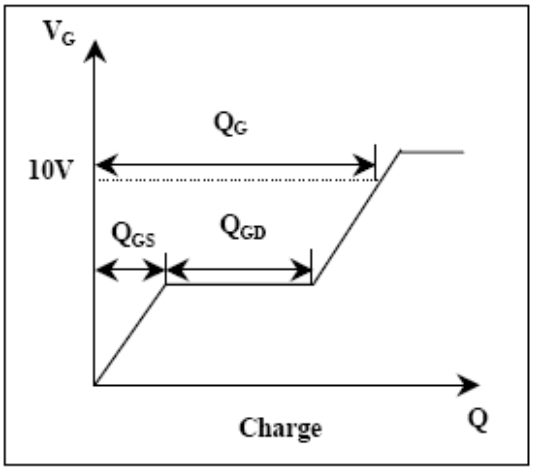

Fig 12. Gate Charge Waveform

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