SPN100T12
N-Channel Enhancement Mode MOSFET

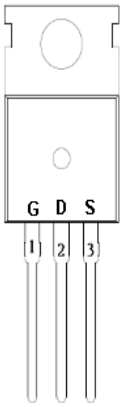
DESCRIPTION
The SPN100T12 is the N-Channel enhancement mode power field effect transistor which is produced using high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suitable for synchronous rectifier application, Motor control power management and other Power Tool circuits. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

APPLICATIONS
- DC/DC Converter
- Load Switch
- SMPS Secondary Side Synchronous Rectifier
- Power Tool
- Motor Control

FEATURES
- 120V/100A , $R_{DS(ON)}$=10mΩ@V_{GS}=10V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-220-3L/TO-220F-3L/PPAK5x6-8L package design

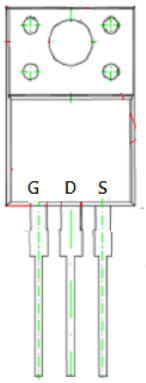
PIN CONFIGURATION

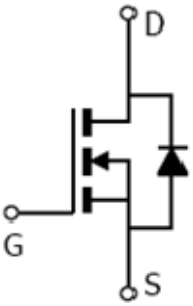
TO-220-3L

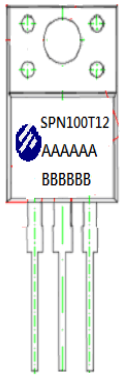


A : Lot Code
B : Date Code

TO-220F-3L

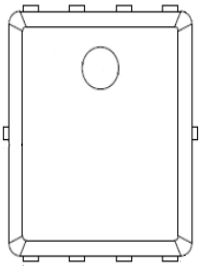






A: Lot Code
B: Date Code
(YYMMDD)

PPAK5x6-8L



A : Lot Code
B : Date Code
(YY / MM / DD)

PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

PPAK5x6 PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN100T12T220TGB	TO-220-3L	SPN100T12
SPN100T12T220FTGB	TO-220F-3L	SPN100T12
SPN100T12DN8RGB	PPAK5x6-8L	SPN100T12

※ SPN100T12T220TGB : Tube ; Pb – Free ; Halogen – Free
※ SPN100T12T220FTGB : Tube ; Pb – Free ; Halogen - Free
※ SPN100T12DN8RGB : Tape Reel ; Pb – Free ; Halogen – Free

SPN100T12
N-Channel Enhancement Mode MOSFET

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	120	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current (Silicon Limited)	T_C=25℃	I_D	100	A
	T_C=70℃		72	
Continuous Drain Current(Silicon Limited) (PPAK5x6)	T_C=25℃	I_D	92	A
	T_C=70℃		60	
Pulsed Drain Current		I_{DM}	300	A
Power Dissipation@ T_C=25℃ (TO-220)		P_D	104	W
Power Dissipation@ T_C=25℃ (TO-220F)			93	
Power Dissipation@ T_C=25℃ (PPAK5x6)			83	
Avalanche Energy with Single Pulse (T_C=25℃, L = 0.4mH.)		E_{AS}	468	mJ
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient (TO-220/TO-220F)		$R_{\theta JC}$	1.2	℃/W
Thermal Resistance-Junction to Ambient (PPAK5x6)		$R_{\theta JC}$	1.5	℃/W

Note :

The maximum current rating is package limited at 120A for TO-220-3L
The maximum current rating is package limited at 78A for TO-220F-3L
The maximum current rating is package limited at 80A for PPAK5x6-8L

ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	120			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	2	3	4	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=120V,V_{GS}=0V T_J = 25°C			1	uA
		V_{DS}=120V,V_{GS}=0V T_J = 100°C			100	
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=20A		7.8	10	mΩ
Diode Forward Voltage	V_{SD}	I_F=20A,V_{GS} =0V		0.9	1.2	V
Forward Transconductance	gfs	V_{DS}=5V,I_D=20A		65		S
Gate Resistance	R_G	V_{GS}=0V,V_{DS}Open, f=1MHz		3.5		Ω
Dynamic						
Total Gate Charge	Q_g	V_{DS}=60V,V_{GS}=10V I_D=20A		56		nC
Gate-Source Charge	Q_{gs}			18		
Gate-Drain Charge	Q_{gd}			6		
Input Capacitance	C_{iss}	V_{DD}=60V,V_{GS}=0V f=1MHz		4470		pF
Output Capacitance	C_{oss}			235		
Reverse Transfer Capacitance	C_{rss}			9.5		
Turn-On Time	$t_{d(on)}$	V_{DD}=60V, I_D=20A,V_{GS}=10V R_G=10Ω		16		nS
	t_r			21		
Turn-Off Time	$t_{d(off)}$			38		
	t_f			19		
Reverse Recovery Time	trr	V_R=60V, I_F=20A, d I_F/dt=500A/uS		70		nS
Reverse Recovery Charge	Qrr			600		nC

TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

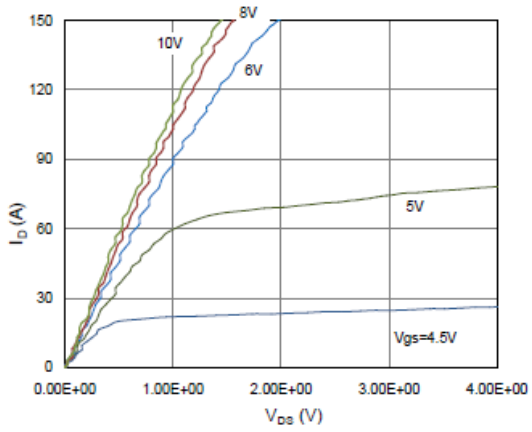


Figure 2. On-Resistance vs. Gate-Source Voltage

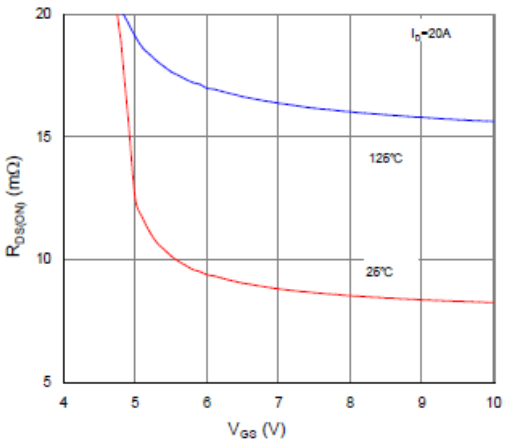


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

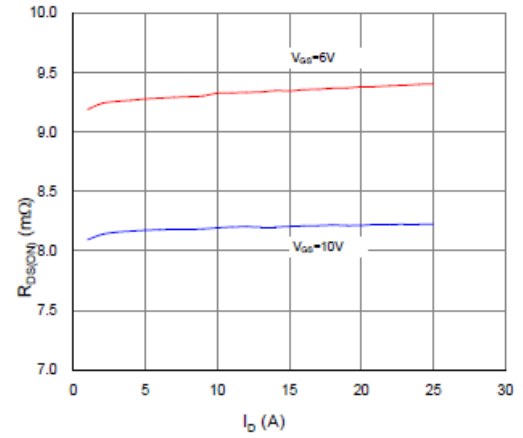


Figure 4. Normalized On-Resistance vs. Junction Temperature

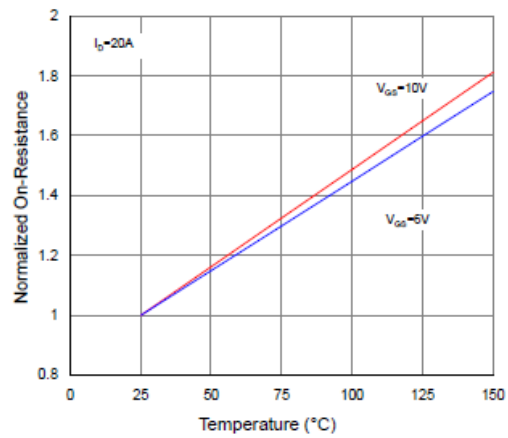


Figure 5. Typical Transfer Characteristics

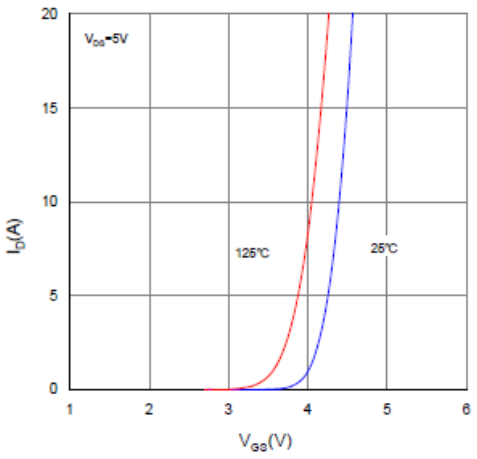
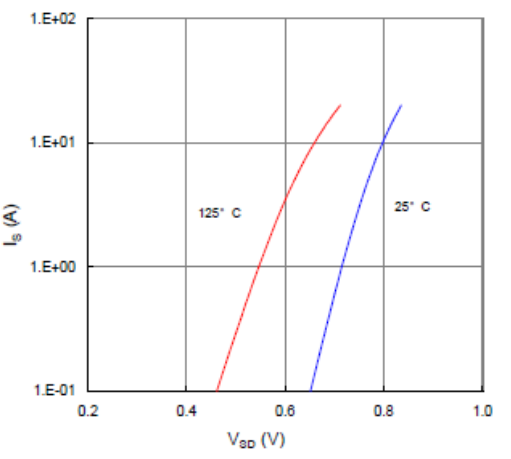


Figure 6. Typical Source-Drain Diode Forward Voltage



TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

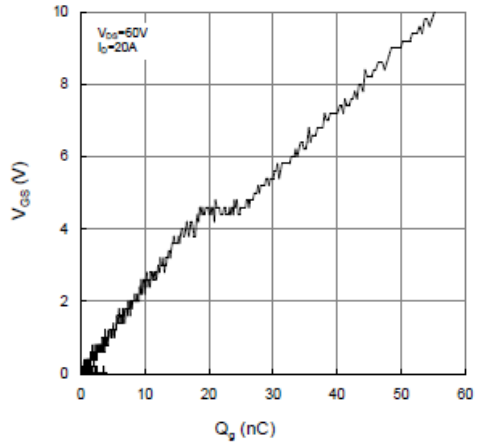


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

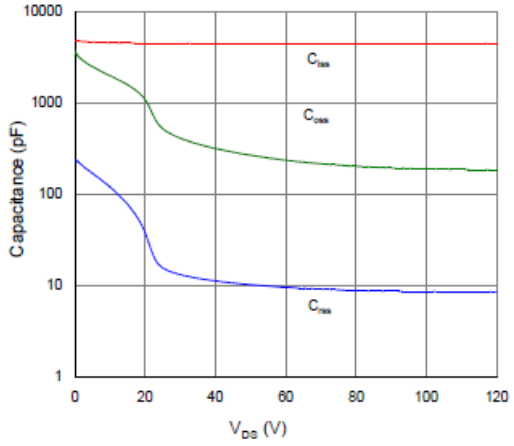


Figure 9. Maximum Safe Operating Area

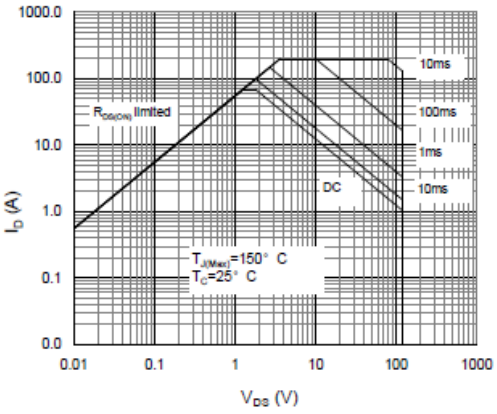


Figure 10. Maximun Drain Current vs. Case Temperature

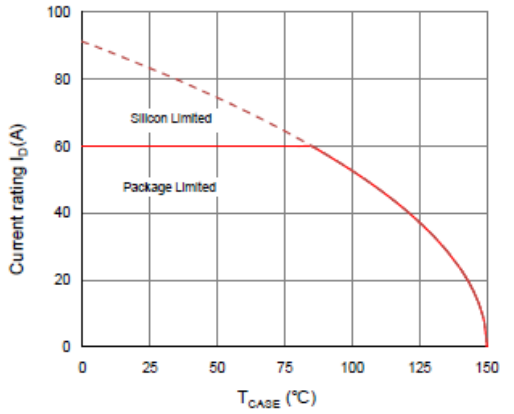
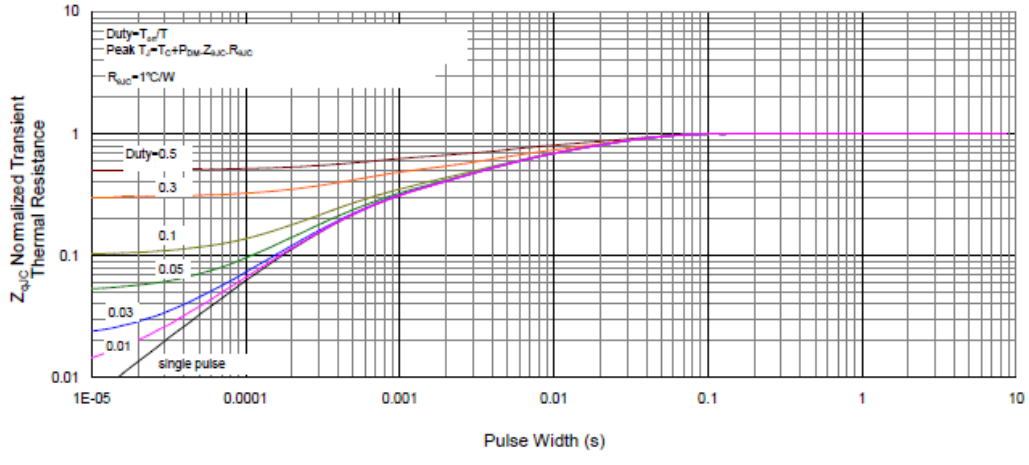


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case



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