



SPN1032

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN1032 is the N-Channel enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where high-side switching, low in-line power loss, and resistance to transients are needed.

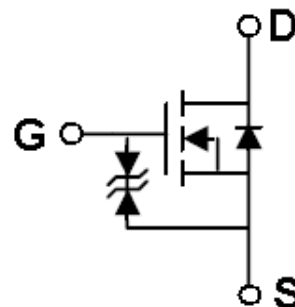
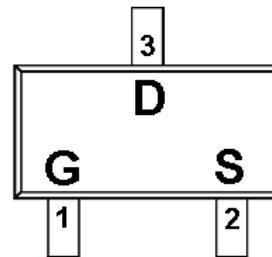
FEATURES

- N-Channel
30V/0.95A, $R_{DS(ON)}=550m\Omega@V_{GS}=4.5V$
30V/0.75A, $R_{DS(ON)}=650m\Omega@V_{GS}=2.5V$
30V/0.65A, $R_{DS(ON)}=850m\Omega@V_{GS}=1.8V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- ESD protected
- SOT-523 (SC-89-3L) package design

APPLICATIONS

- Drivers : Relays/Solenoids/Lamps/Hammers
- Power Supply Converter Circuits
- Load/Power Switching Cell Phones, Pagers

PIN CONFIGURATION (SOT-523 / SC-89-3L)



PART MARKING



Y : year
W: week



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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN1032S52RGB	SOT-523	B2

※ SPN1032S52RGB : Tape Reel ; Pb – Free, Halogen – Free

ABSOLUTE MAXIMUM RATINGS

($T_A=25^{\circ}\text{C}$ Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V_{DSS}	30	V	
Gate –Source Voltage	V_{GSS}	± 12	V	
Continuous Drain Current($T_J=150^{\circ}\text{C}$)	I_D	$T_A=25^{\circ}\text{C}$	1.2	A
		$T_A=125^{\circ}\text{C}$	1.0	
Pulsed Drain Current (*)	I_{DM}	2.5	A	
Thermal Resistance-Junction to Ambient	$R_{\theta JA}$	375	$^{\circ}\text{C}/\text{W}$	
Power Dissipation	P_D	1.35	W	
Operating Junction Temperature	T_J	-55/150	$^{\circ}\text{C}$	
Storage Temperature Range	T_{STG}	-55/150	$^{\circ}\text{C}$	

(*) Pulse width limited by safe operating area



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ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

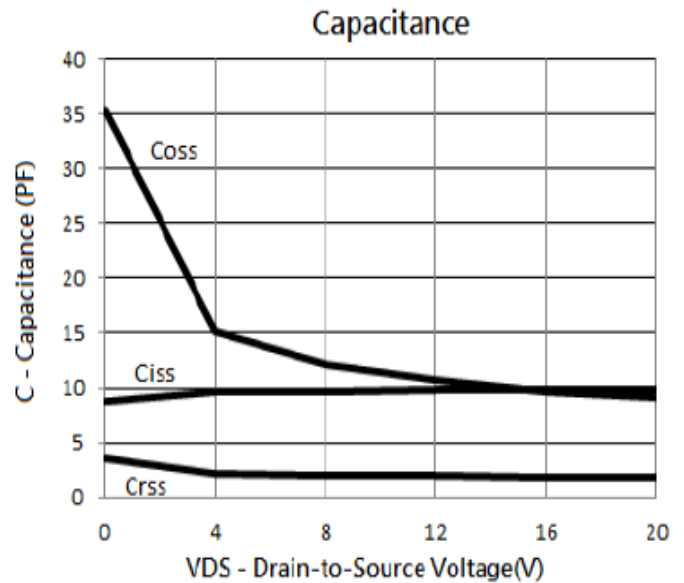
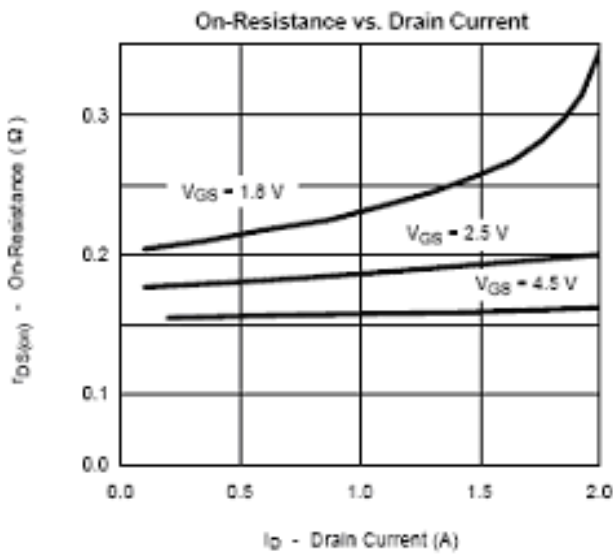
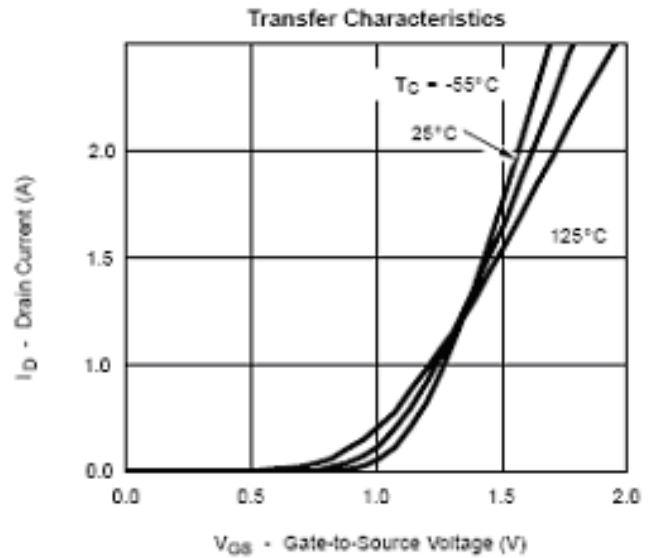
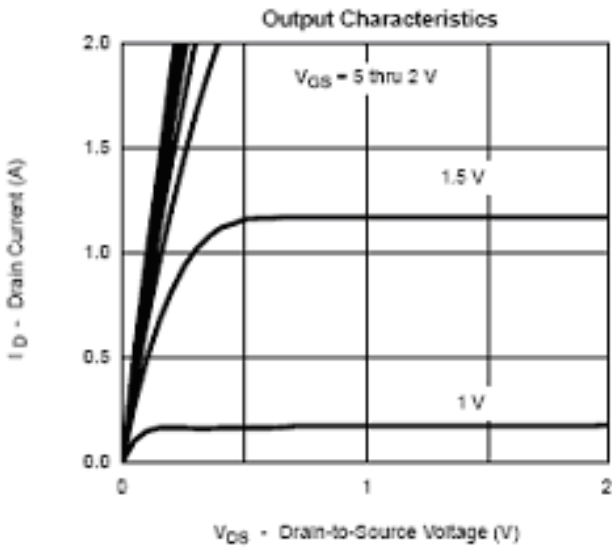
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.35		1.0	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 12V$			± 10	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=24V, V_{GS}=0V, T_J=25^\circ C$			1	μA
		$V_{DS}=24V, V_{GS}=0V, T_J=55^\circ C$			100	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\geq 4.5V, V_{GS}=5V$	0.7			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=0.95A$		0.26	0.55	Ω
		$V_{GS}=2.5V, I_D=0.75A$		0.38	0.65	
		$V_{GS}=1.8V, I_D=0.65A$		0.52	0.85	
Forward Transconductance	g_{fs}	$V_{DS}=10V, I_D=0.4A$		1.0		S
Diode Forward Voltage	V_{SD}	$I_S=0.15A, V_{GS}=0V$		0.8	1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=10V, V_{GS}=4.5V, I_D=0.6A$		1.2	1.5	nC
Gate-Source Charge	Q_{gs}			0.2		
Gate-Drain Charge	Q_{gd}			0.3		
Input Capacitance	C_{iss}	$V_{DS}=10V, f=1MHz, V_{GS}=0V$		7.2		pF
Output Capacitance	C_{oss}			13.5		
Reverse Transfer Capacitance	C_{rss}			1.6		
Turn-On Time	$t_{d(on)}$	$V_{DD}=10V, R_L=10\Omega, I_D=0.5A, V_{GEN}=4.5V, R_G=6\Omega$		5	10	nS
	t_r			8	15	
Turn-Off Time	$t_{d(off)}$			10	18	
	t_f			1.2	2.8	



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TYPICAL CHARACTERISTICS

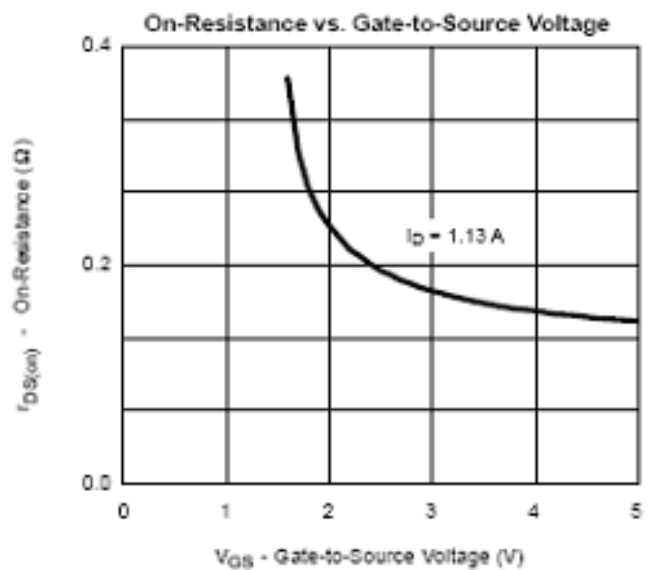
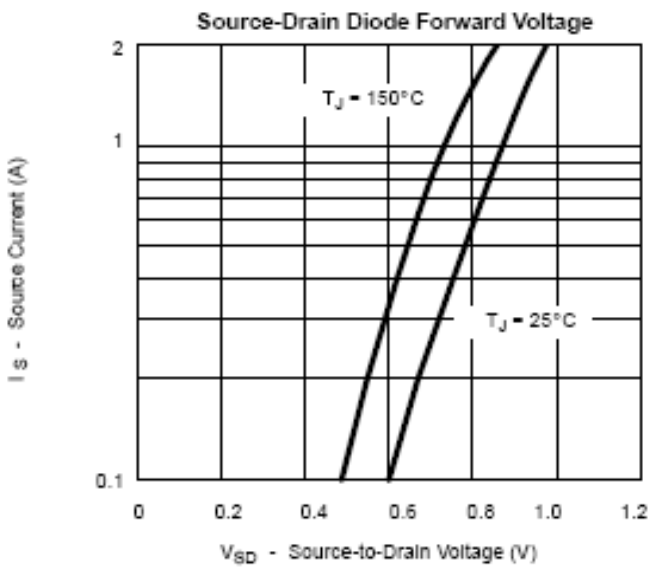
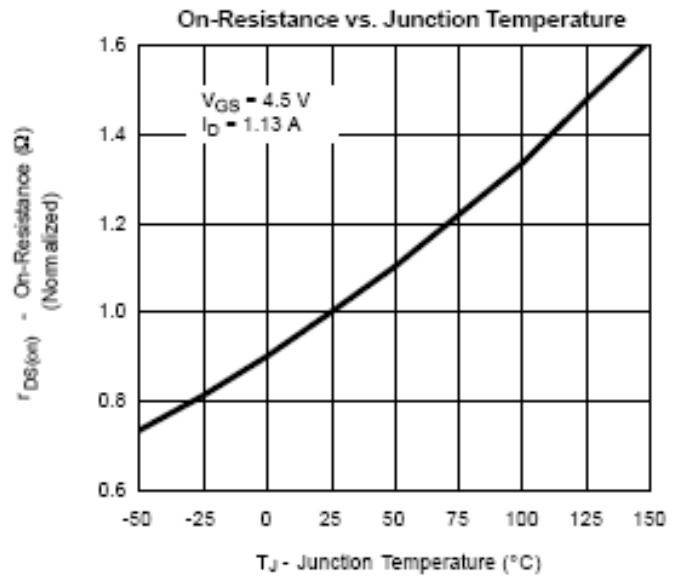
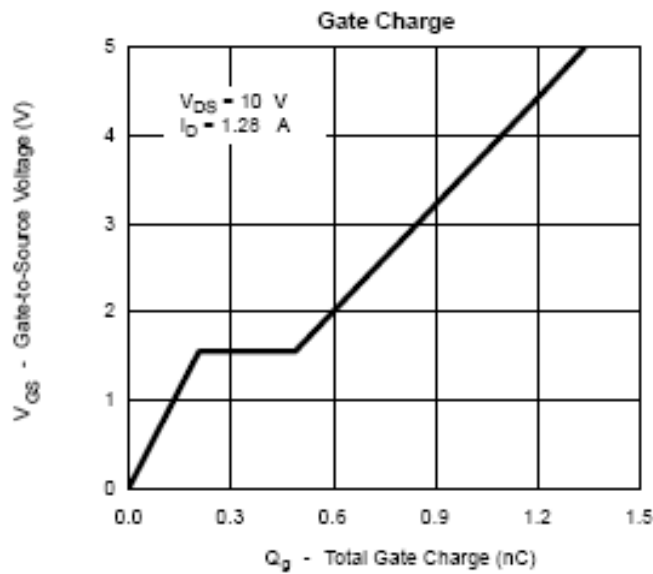




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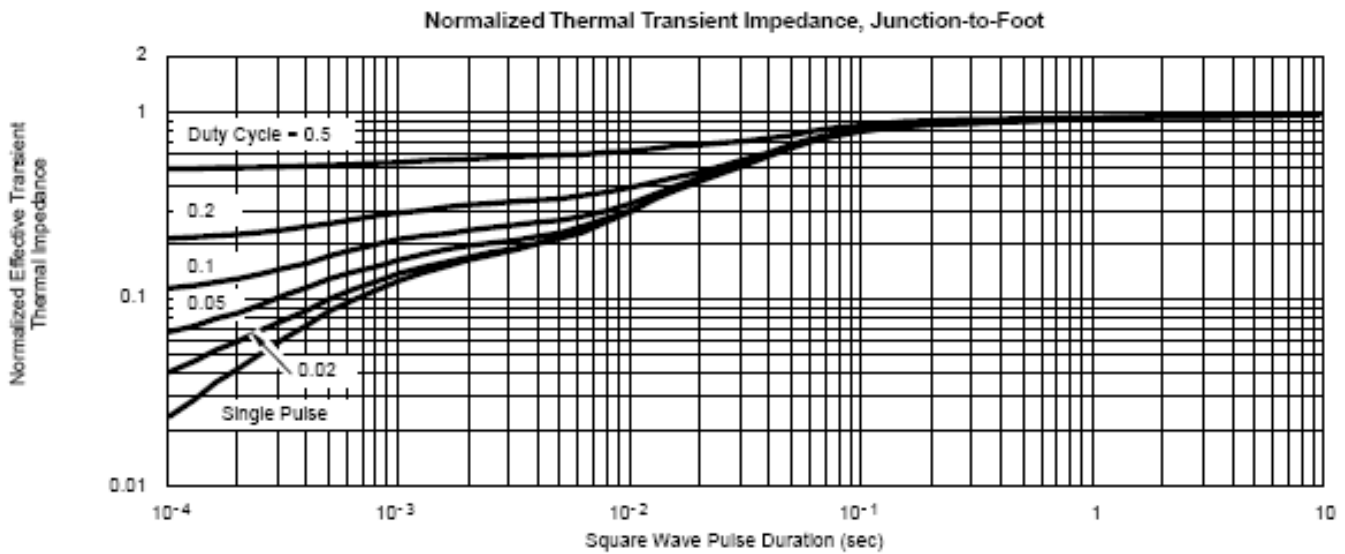
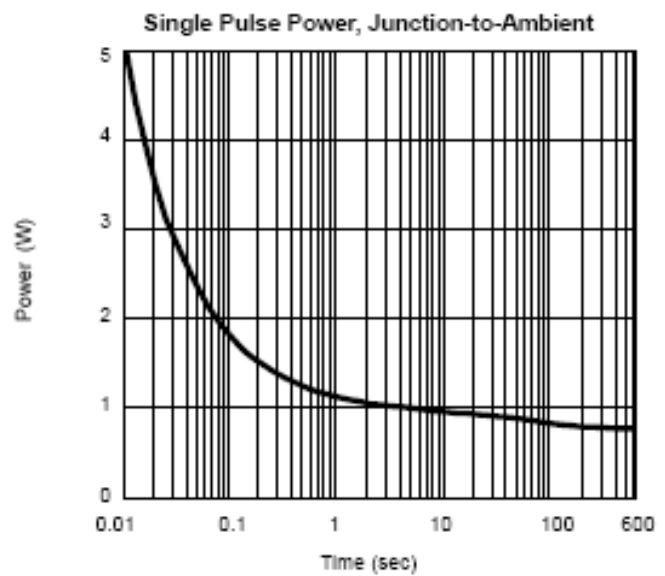
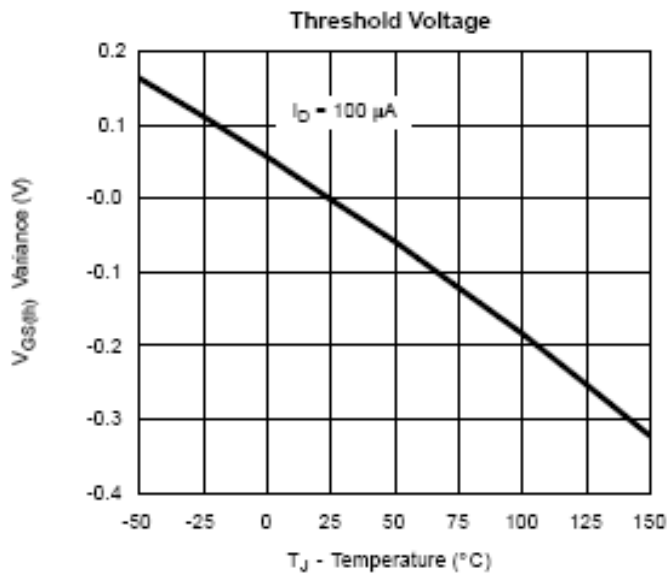




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TYPICAL CHARACTERISTICS





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