



SPN120T06

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN120T06 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching.

FEATURES

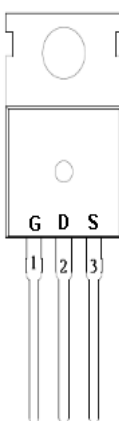
- ◆ 60V/108A, $R_{DS(ON)}=4.9m\Omega@V_{GS}=10V$
- ◆ 60V/108A, $R_{DS(ON)}=7.5m\Omega@V_{GS}=4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-220-3L/TO-220F-3L/TO-252-2L package design

APPLICATIONS

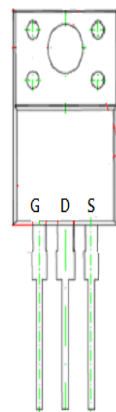
- DC/DC Converter
- Load Switch
- Synchronous Buck Converter
- UPS
- Motor Control
- Power Tool

PIN CONFIGURATION

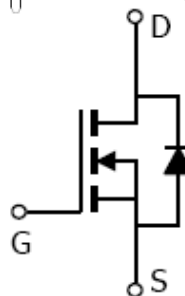
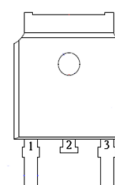
TO-220



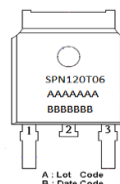
TO-220F



TO-252-2L



PART MARKING



A : Lot Code
B : Date Code



A: Lot Code
B: Date Code
(YYMMDD)



A : Lot Code
B : Date Code
(YY / MM / DD)



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TO-220/TO-220F PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN120T06T220TGB	TO-220-3L	SPN120T06
SPN120T06T220FTGB	TO-220F-3L	SPN120T06
SPN120T06T252RGB	TO-252-2L	SPN120T06

- ※ SPN120T06T220TGB : Tube ; Pb – Free ; Halogen – Free
- ※ SPN120T06T220FTGB : Tube ; Pb – Free ; Halogen – Free
- ※ SPN120T06T252RGB : Tape&Reel ; Pb – Free ; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	60	V
Gate –Source Voltage	V _{GSS}	±20	V
Continuous Drain Current (Silicon Limited)	I _D	108	A
		77	
Pulsed Drain Current	I _{DM}	340	A
Avalanche Energy Single Pulse(L=0.1mH, Tc=25°C)	E _{AS}	31	mJ
Power Dissipation@ Tc=25°C	TO-220	104	W
	TO-252/TO-220F	93	
Operating Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Case (TO-220)	R _{θJC}	1.2	°C/W
Thermal Resistance-Junction to Case (TO-252/TO-220F)	R _{θJC}	1.35	°C/W

Note :

The maximum current rating is package limited at 120A for TO-220-3L

The maximum current rating is package limited at 78A for TO-220F-3L

The maximum current rating is package limited at 70A for TO-252-2L



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ELECTRICAL CHARACTERISTICS

(T_A=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250μA	60			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.0	1.6	2.4	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =48V, V _{GS} =0V T _J =25°C			1	μA
		V _{DS} =48V, V _{GS} =0V T _J =100°C			100	
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =20A		4.2	4.9	mΩ
		V _{GS} =4.5V, I _D =10A		6.3	7.5	
Forward Transconductance	g _{fs}	V _{DS} =5V, I _D =20A		60		S
Gate Resistance	R _G	V _{GS} =0V, V _{DS} Open, f=1MHz		1.3		Ω
Diode Forward Voltage	V _{SD}	I _S =30A, V _{GS} =0V		0.9	1.2	V
Dynamic						
Total Gate Charge(10V)	Q _g	V _{DS} =30V, V _{GS} =10V I _D =20A		41		nC
Total Gate Charge(4.5V)	Q _g			25		
Gate-Source Charge	Q _{gs}			5		
Gate-Drain Charge	Q _{gd}			11		
Input Capacitance	C _{iss}	V _{DS} =30V, V _{GS} =0V f=1MHz		1978		pF
Output Capacitance	C _{oss}			870		
Reverse Transfer Capacitance	C _{rss}			56		
Turn-On Time	t _{d(on)}	V _{DD} =30V, I _D =20A, V _{GEN} =10V R _G =10Ω		10		nS
	t _r			8		
Turn-Off Time	t _{d(off)}			34		
	t _f			10		



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TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

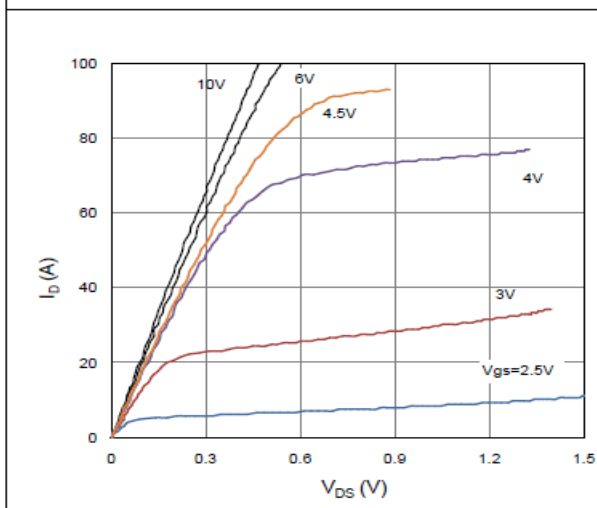


Figure 2. On-Resistance vs. Gate-Source Voltage

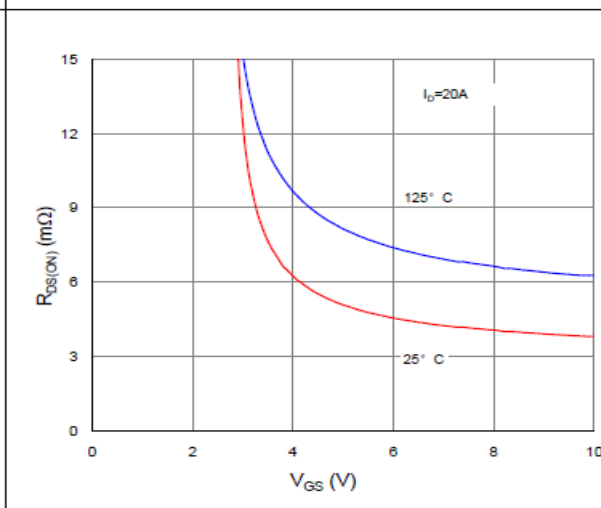


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

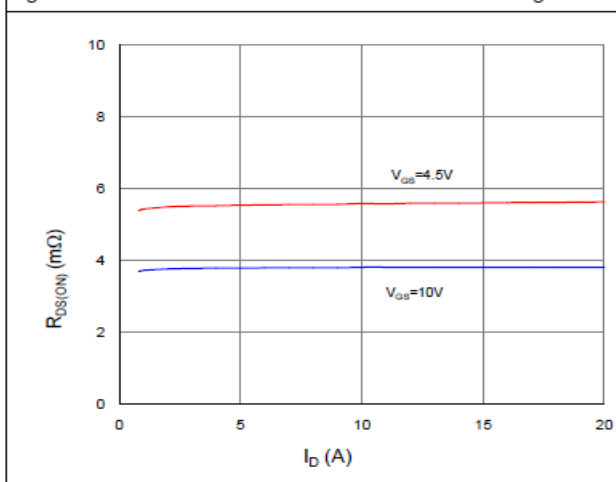


Figure 4. Normalized On-Resistance vs. Junction Temperature

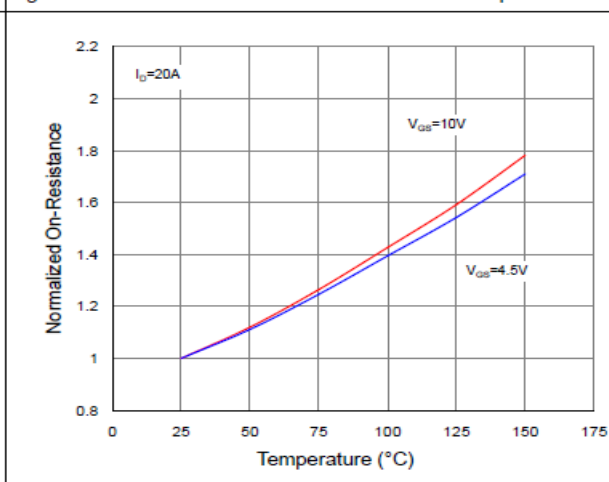


Figure 5. Typical Transfer Characteristics

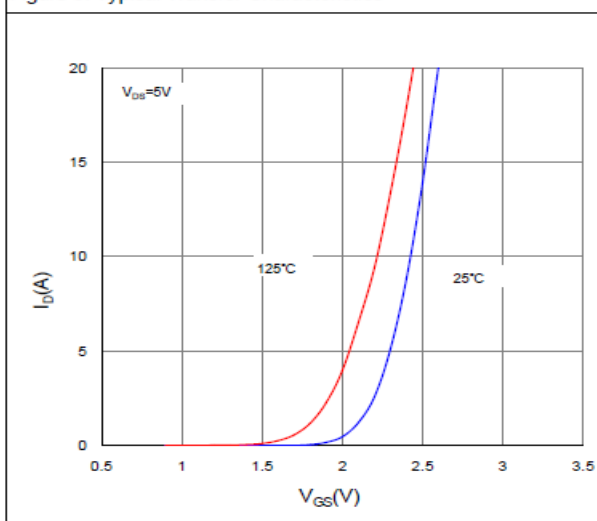
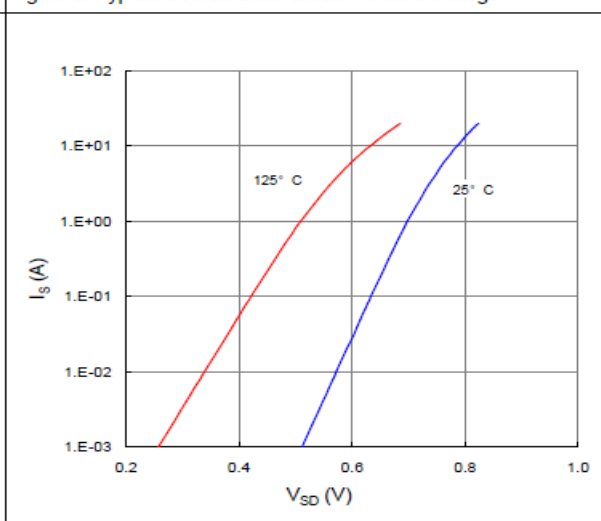


Figure 6. Typical Source-Drain Diode Forward Voltage





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TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

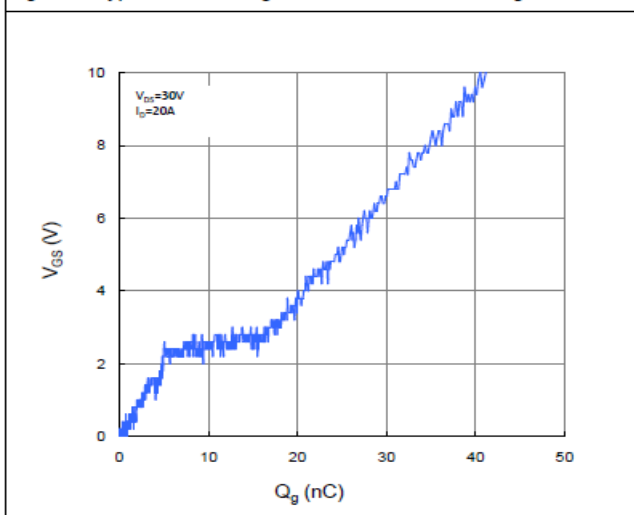


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

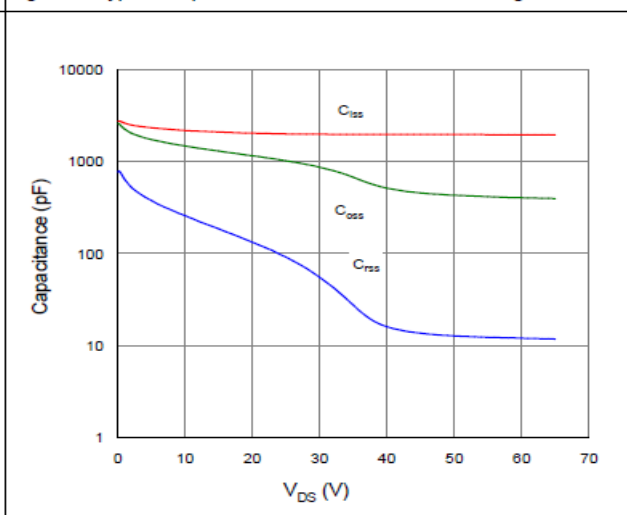


Figure 9. Maximum Safe Operating Area

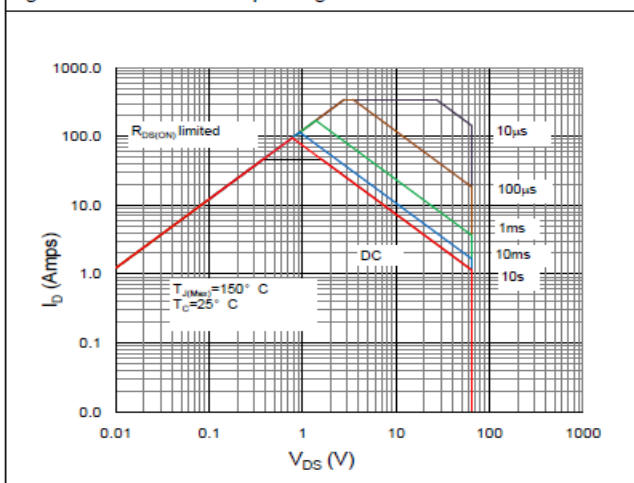


Figure 10. Maximum Drain Current vs. Case Temperature

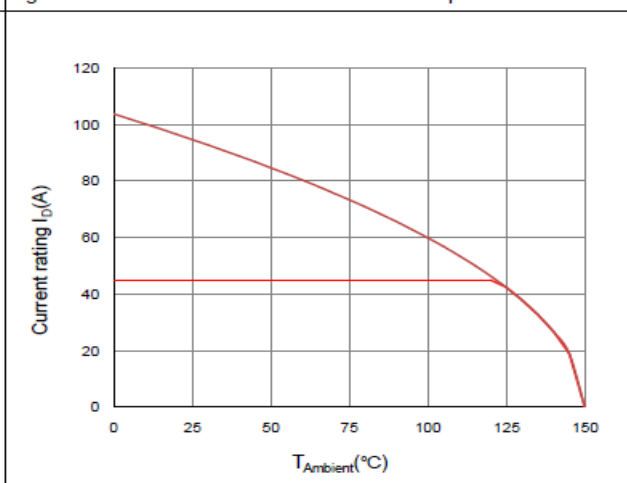
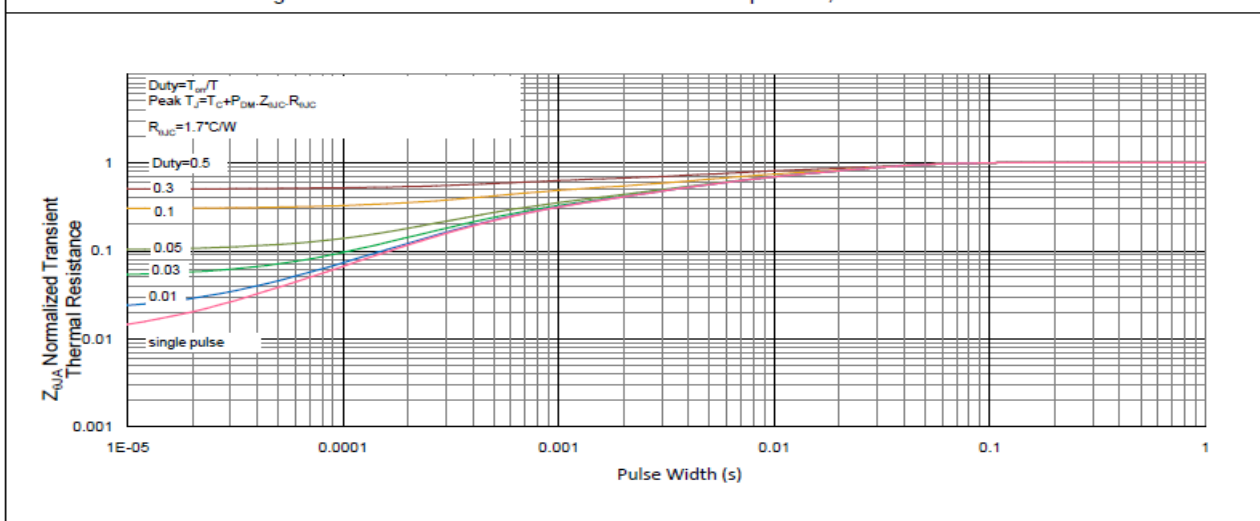


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient





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