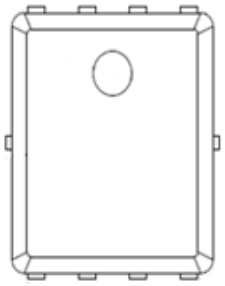
SPN138N08
N-Channel Enhancement Mode MOSFET

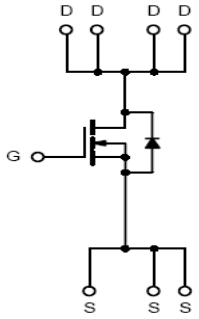
DESCRIPTION
The SPN138N08 is the N-Channel enhancement mode power field effect transistor which is produced using high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suitable for synchronous rectifier application, Motor control power management and other Power Tool circuits. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

APPLICATIONS
- DC/DC Converter
- Load Switch
- SMPS Secondary Side Synchronous Rectifier
- Power Tool
- Motor Control

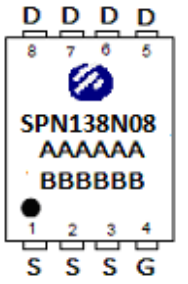
FEATURES
- 80V/138A,$R_{DS(ON)}$=3.6mΩ@V_{GS}=10V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- PPAK5x6-8L package design

PIN CONFIGURATION (PPAK5x6-8L)





PART MARKING



A : Lot Code
B : Date Code
(YY / MM / DD)

SPN138N08
N-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN138N08DN8RGB	PPAK5x6-8L	SPN138N08

※ SPN138N08DN8RGB : 13" Tape Reel ; Pb – Free ; Halogen – Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	80	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(Silicon Limited)	T_C=25℃	I_D	138	A
	T_C=100℃		88	
Pulsed Drain Current		I_{DM}	400	A
Avalanche Energy with Single Pulse (T_c=25℃, L = 0.4mH)		E_{AS}	320	mJ
Power Dissipation	T_C=25℃	P_D	83	W
	T_A=70℃		1.6	
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Case		$R_{\theta JC}$	1.5	℃/W

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ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250uA	80			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250uA	2.0		4.0	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=80V,V_{GS}=0V T_J=25℃			1	uA
		V_{DS}=80V,V_{GS}=0V T_J=100℃			100	
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=20A		3.0	3.5	mΩ
Forward Transconductance	gfs	V_{DS}=5V, I_D=20A		64		S
Gate Resistance	R_G	V_{GS}=0V,V_{DS}=Open, f=1MHz		1.2		Ω
Dynamic						
Total Gate Charge	Q_g	V_{DS}=40V,V_{GS}=10V I_D=20A		68		nC
Gate-Source Charge	Q_{gs}			13		
Gate-Drain Charge	Q_{gd}			17		
Input Capacitance	C_{iss}	V_{DS}=40V,V_{GS}=0V f=1MHz		4350		pF
Output Capacitance	C_{oss}			704		
Reverse Transfer Capacitance	C_{rss}			28		
Turn-On Time	$t_{d(on)}$	V_{DD}=40V, I_D=20A, V_{GS}=10V, R_G=10Ω		16		nS
	t_r			12		
Turn-Off Time	$t_{d(off)}$			50		
	t_f			19		
Reverse Recovery						
Diode Forward Voltage	V_{SD}	I_F=20A,V_{GS}=0V		0.9	1.2	V
Reverse Recovery Time	T_{rr}	V_R=40I_F=20A, dI_F/dt=100A/uS		50		nS
Reverse Recovery Charge	Q_{rr}			61		nC

TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

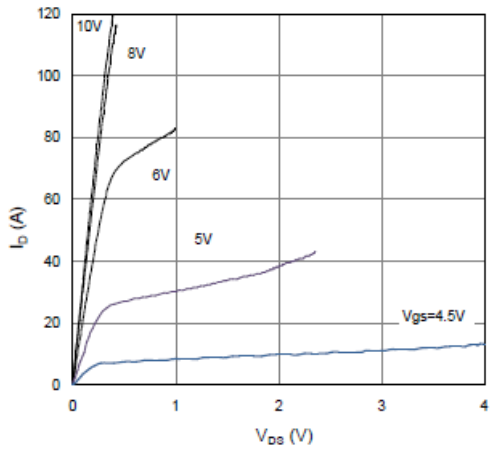


Figure 2. On-Resistance vs. Gate-Source Voltage

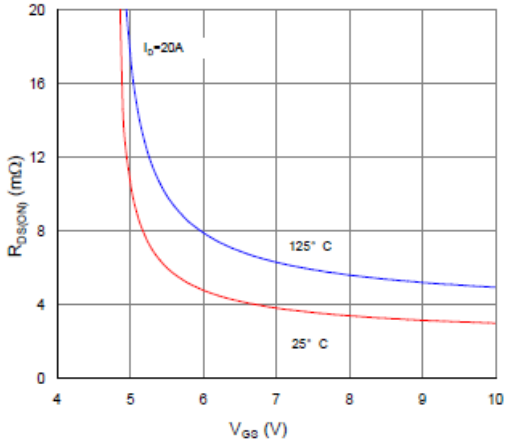


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

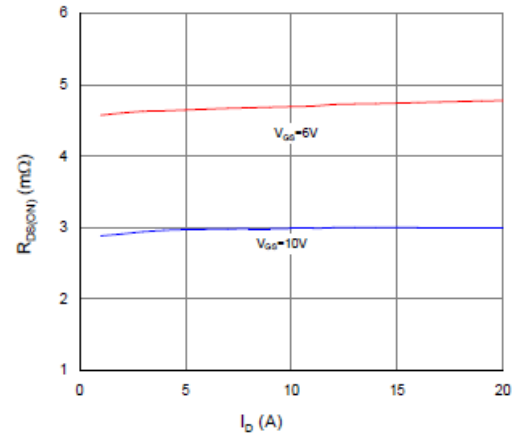


Figure 4. Normalized On-Resistance vs. Junction Temperature

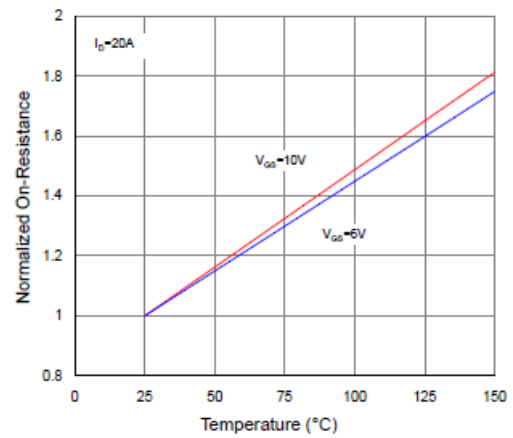


Figure 5. Typical Transfer Characteristics

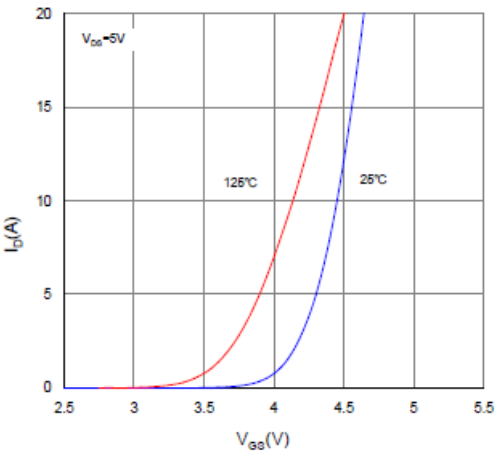
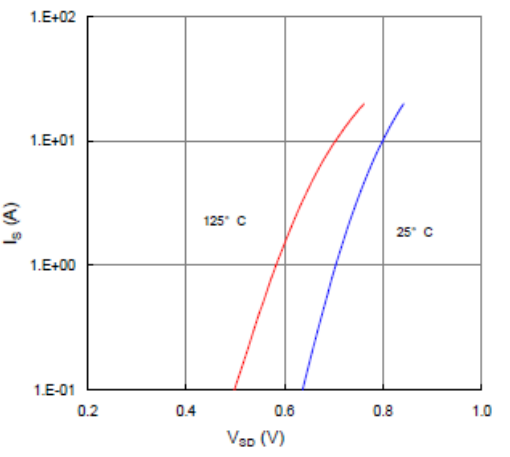


Figure 6. Typical Source-Drain Diode Forward Voltage



TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

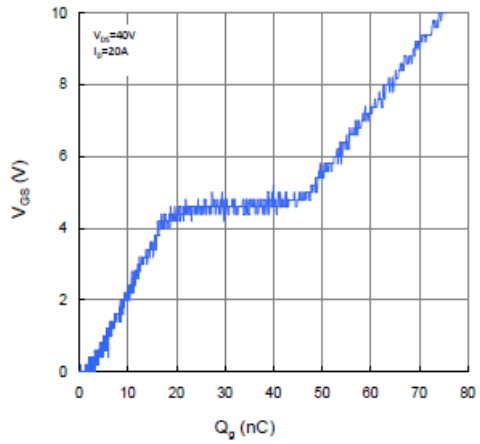


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

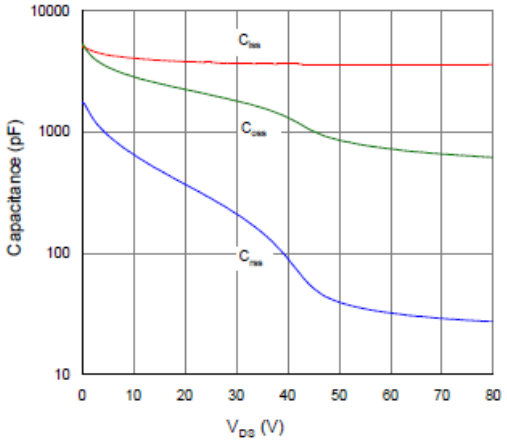


Figure 9. Maximum Safe Operating Area

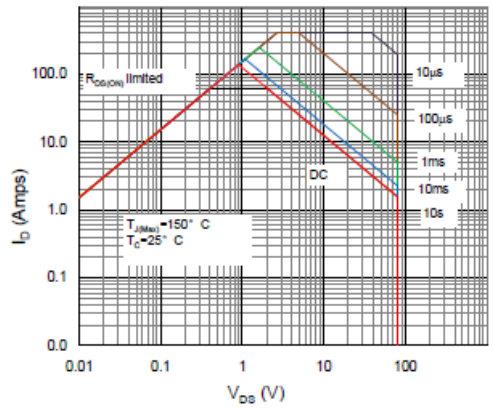


Figure 10. Maximun Drain Current vs. Case Temperature

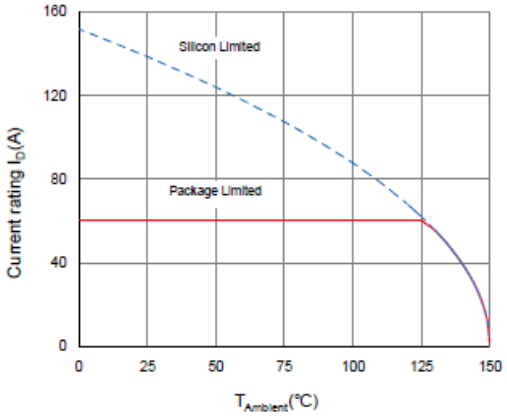
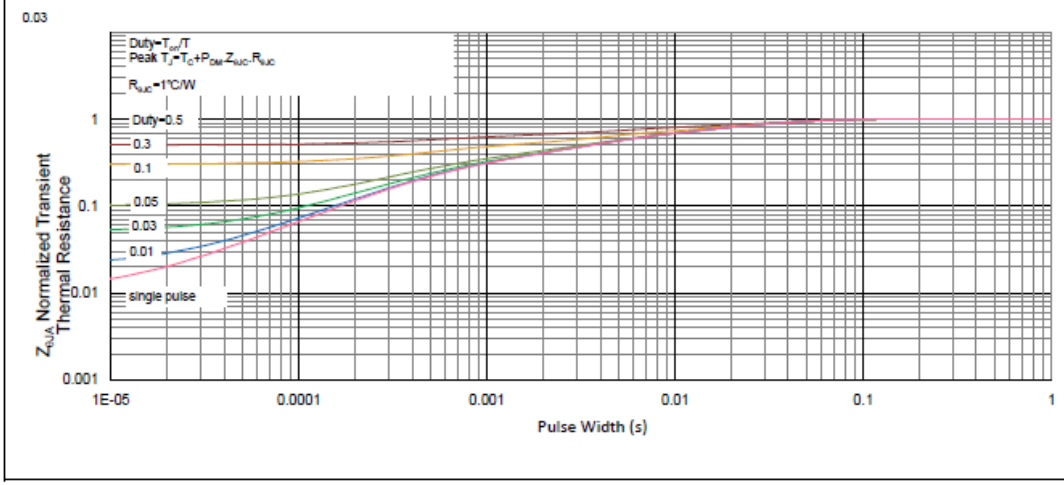


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient



SYNC Power Corporation
7F-2, No.3-1, Park Street
NanKang District (NKSP), Taipei, Taiwan 115
Phone: 886-2-2655-8178
Fax: 886-2-2655-8468
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