



SPN166N06

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN166N06 is the N-Channel enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suitable for synchronous rectifier application, Motor control power management and other Power Tool circuits. It has been optimized for low gate charge, low RDS(ON) and fast switching speed.

FEATURES

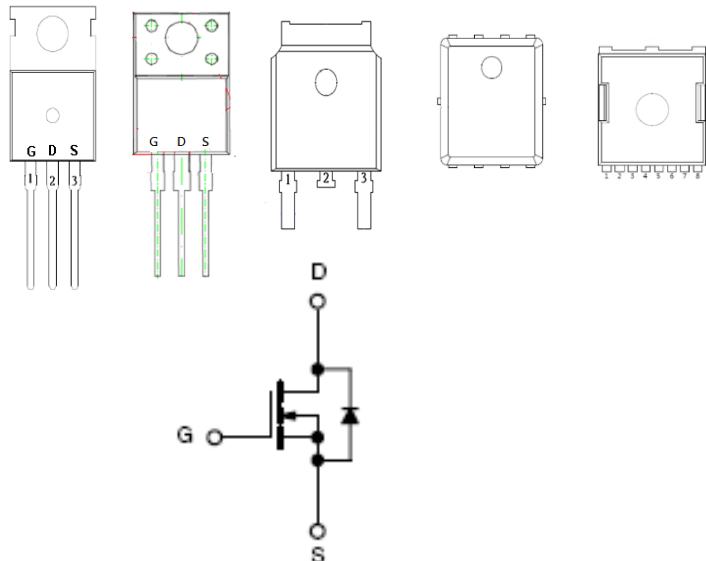
- ◆ 60V/166A,RDS(ON)=3.1mΩ@VGS=10V
- ◆ Super high density cell design for extremely low RDS(ON)
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-220-3L/TO-252-2L/PPAK5x6-8L/ TOLL-8 package design

APPLICATIONS

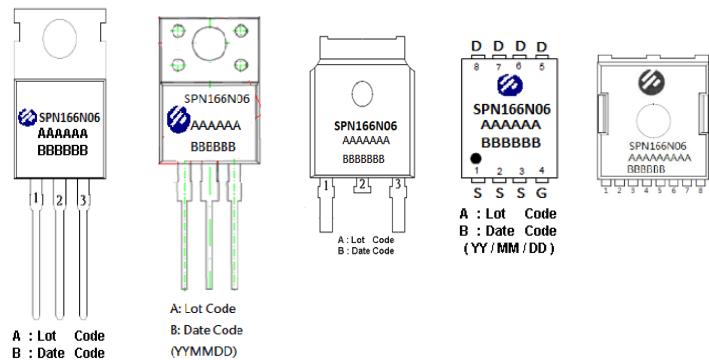
- DC/DC Converter
- Load Switch
- SMPS Secondary Side Synchronous Rectifier
- Motor Control
- Power Tool

PIN CONFIGURATION

TO-220 TO-220F TO252 PPAK5x6 TOLL8



PART MARKING





SPN166N06

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PIN DESCRIPTION TO220/TO220F/TO252

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

PPAK5x6 PIN DESCRIPTION

Pin	Symbol	Description
1~3	S	Source
4	G	Gate
5~8	D	Drain

TOLL-8

Pin	Symbol	Description
1	G	Gate
2~8	S	Source
Tab	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN166N06T220TGB	TO-220-3L	SPN166N06
SPN166N06T220FTGB	TO-220F-3L	SPN166N06
SPN166N06T252RGB	TO-252-2L	SPN166N06
SPN166N06DN8RGB	PPAK5x6-8L	SPN166N06
SPN166N06TOL8RGB	TOLL-8	SPN166N06

- ※ SPN166N06T220TGB : Tube ; Pb – Free ; Halogen – Free
- ※ SPN166N06T220FTGB : Tube ; Pb – Free ; Halogen – Free
- ※ SPN166N06T252RGB : Tape&Reel ; Pb – Free ; Halogen - Free
- ※ SPN166N06DN8RGB : Tape&Reel ; Pb – Free ; Halogen – Free
- ※ SPN166N06TOL8RGB: Tape&Reel ; Pb – Free ; Halogen – Free



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ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	60	V
Gate –Source Voltage	V _{GSS}	±20	V
Continuous Drain Current (Silicon Limited)	T _c =25°C	ID	A
	T _c =100°C		
Pulsed Drain Current	I _{DM}	400	A
Power Dissipation @ T _c =25°C	TO-220	P _D	W
	TO-252		
	PPAK5x6		
	TOLL-8		
Avalanche Energy with Single Pulse (T _c =25°C, L=0.1mH.)	EAS	259	mJ
Operating Junction Temperature	T _J	-55/175	°C
Storage Temperature Range	T _{STG}	-55/175	°C
Thermal Resistance-Junction to Case (TO-220/TO-220F)	R _{θJC}	1.2	°C/W
Thermal Resistance-Junction to Case (TO-252)	R _{θJC}	1.35	°C/W
Thermal Resistance-Junction to Case (PPAK5x6)	R _{θJC}	1.5	°C/W
Thermal Resistance-Junction to Case (TOLL-8)	R _{θJC}	0.42	°C/W

Note :

The maximum current rating is package limited at 120A for TO-220-3L

The maximum current rating is package limited at 70A for TO-252-2L

The maximum current rating is package limited at 80A for PPAK5x6-8L



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ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

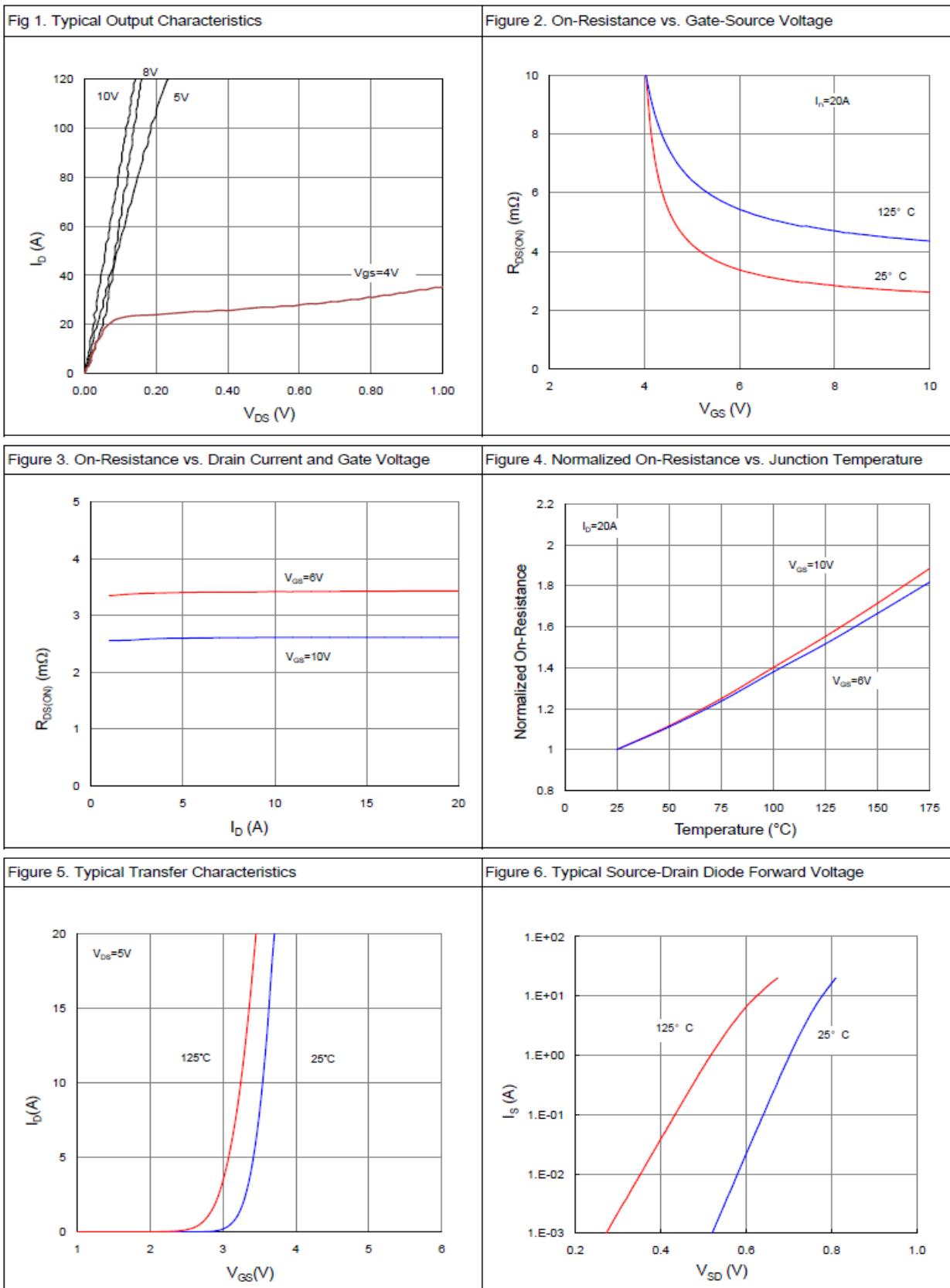
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250uA	60			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	2.0		4.0	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =48V, V _{GS} =0V T _J =25°C			1	uA
		V _{DS} =48V, V _{GS} =0V T _J =100°C			100	
Drain-Source On-Resistance	R _{D(on)}	V _{GS} =10V, I _D =20A		2.6	3.1	mΩ
				2.9	3.3	
Forward Transconductance	g _{fs}	V _{DS} =5V, I _D =20A		66		S
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V		0.9	1.2	V
Gate Resistance	R _G	V _{GS} =0V, V _{DS} open, f=1MHz		1.25		Ω
Dynamic						
Total Gate Charge (10V)	Q _g	V _{DS} =30V, V _{GS} =10V I _D =20A		66		nC
Gate-Source Charge	Q _{gs}			16		
Gate-Drain Charge	Q _{gd}			16		
Input Capacitance	C _{iss}	V _{DS} =30V, V _{GS} =0V f=1MHz		4348		pF
Output Capacitance	C _{oss}			1501		
Reverse Transfer Capacitance	C _{rss}			92		
Turn-On Time	td(on)	V _{DD} =30V, I _D =20A V _{GEN} =10V, R _G =10Ω		15		nS
	tr			12		
Turn-Off Time	td(off)			52		
	tf			19		



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TYPICAL CHARACTERISTICS





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TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

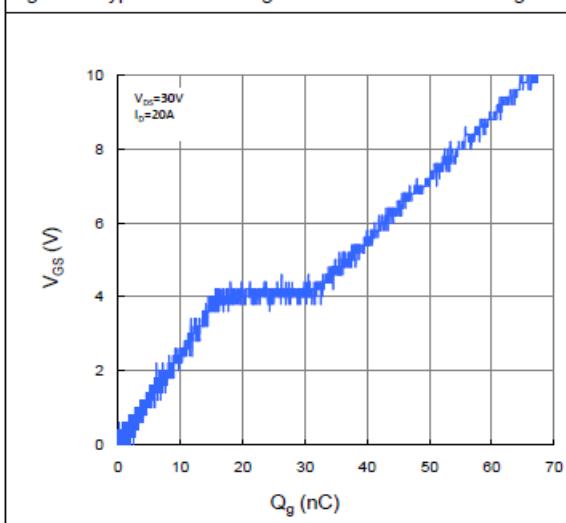


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

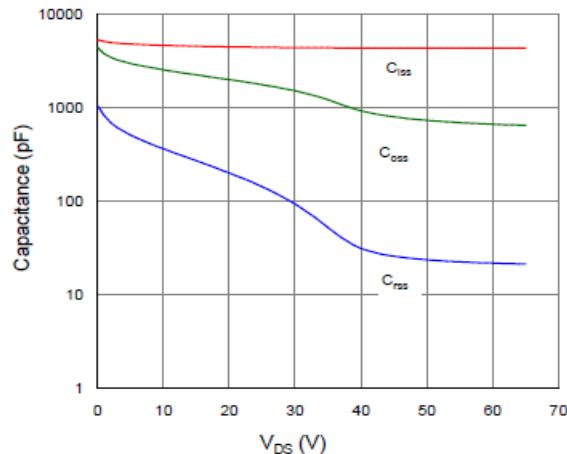


Figure 9. Maximum Safe Operating Area

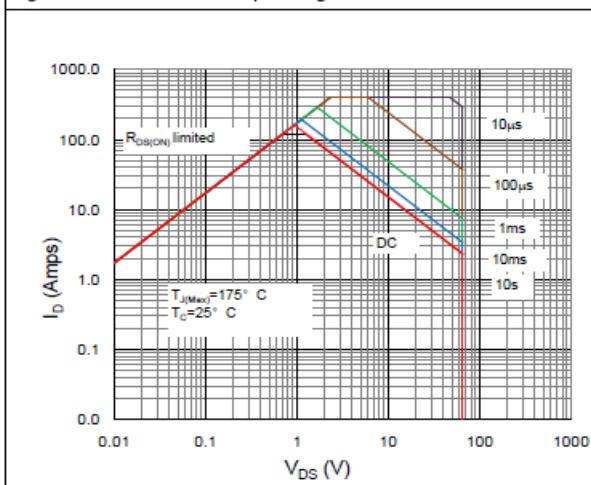


Figure 10. Maximum Drain Current vs. Case Temperature

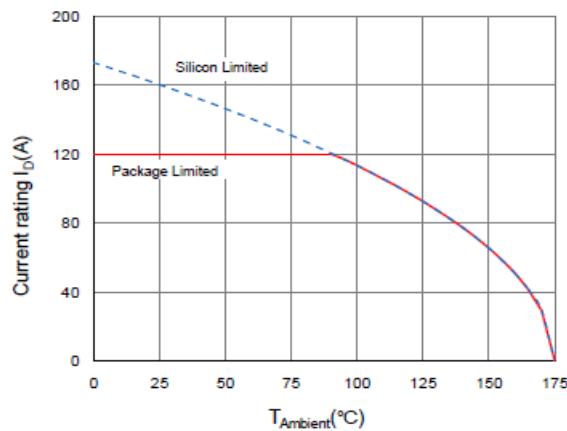
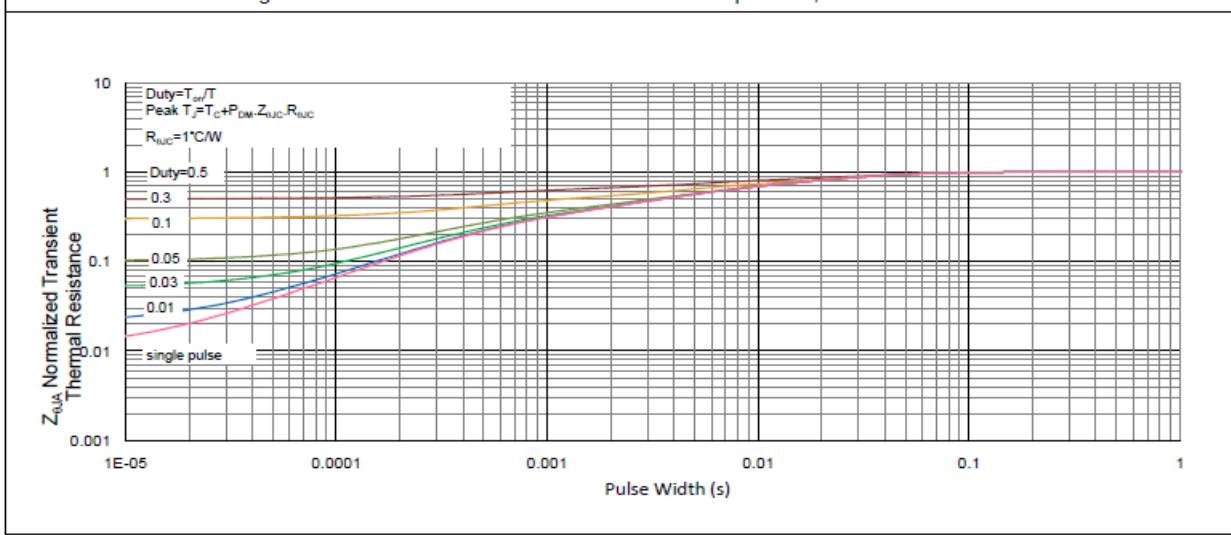


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient





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