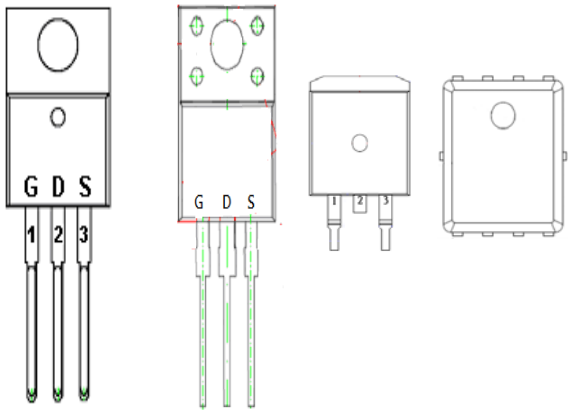
SPN180N10
N-Channel Enhancement Mode MOSFET

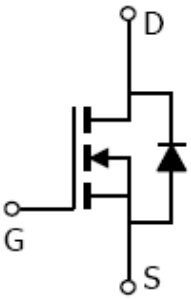
DESCRIPTION
The SPN180N10 is the N-Channel enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suitable for synchronous rectifier application, Motor control power management and other Power Tool circuits. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

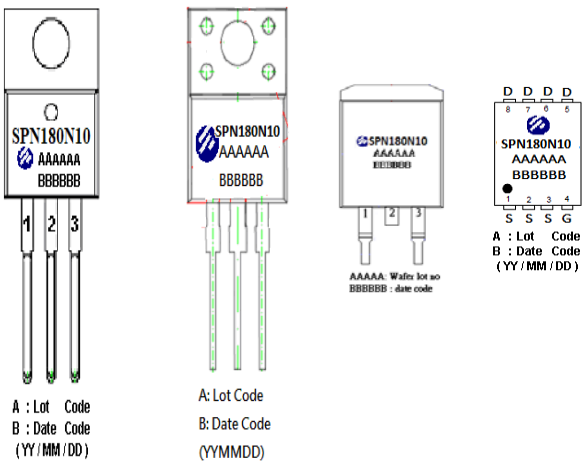
APPLICATIONS
- AC/DC Synchronous Rectifier
- Load Switch
- UPS
- Power Tool
- Motor Control

FEATURES
- 100V/184A, $R_{DS(ON)}$=3.7mΩ@V_{GS}=10V
- High density cell design or extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-220-3L/TO-220F-3L/TO-263-2L/PPAK5x6 package design

PIN CONFIGURATION
TO-220-3L TO-220F-3L TO-263-2L PPAK5x6





PART MARKING


TO-220-3L/TO-220F-3L/TO-263-2L PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

PPAK5x6-8L

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN180N10T220TGB	TO-220-3L	SPN180N10
SPN180N10T220FTGB	TO-220F-3L	SPN180N10
SPN180N10T262RGB	TO-263-2L	SPN180N10
SPN180N10DN8RGB	PPAK5x6	SPN180N10

※ SPN180N10T220TGB : Tube ; Pb – Free ; Halogen - Free
※ SPN180N10T220FTGB : Tube ; Pb – Free ; Halogen – Free
※ SPN180N10T262RGB : Tape&Reel ; Pb–Free ; Halogen – Free
※ SPN180N19DN8RGB：Tape&Reel ; Pb–Free ; Halogen – Free

SPN180N10
N-Channel Enhancement Mode MOSFET

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current (Silicon Limited)	T_C=25℃	I_D	184	A
Continuous Drain Current (Silicon Limited)	T_C=100℃		130	
Pulsed Drain Current		I_{DM}	520	A
Avalanche Energy Single Pulse(L=0.1mH, T_C=25℃)		E_{AS}	180	mJ
Power Dissipation @ T_C=25℃	TO-220/TO-263	P_D	104	W
	TO-220F		30	
	PPAK5x6		83	
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Case	TO-220/TO-263	$R_{\theta JC}$	1.2	℃/W
	TO-220F		4.2	℃/W
	PPAK5x6		1.5	℃/W

Note :

The maximum current rating is package limited at 130A for TO-263-2L
The maximum current rating is package limited at 120A for TO-220-3L
The maximum current rating is package limited at 78A for TO-220F-3L

ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	2.0	2.8	4.0	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=80V,V_{GS}=0V T_J=25℃			1	uA
		V_{DS}=80V,V_{GS}=0V T_J=100℃			100	
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=20A		3.2	3.7	mΩ
Forward Transconductance	gfs	V_{DS}=5V,I_D=20A		70		S
Gate Resistance	R_G	V_{GS}=0V,V_{DS} Open, f=1MHz		0.6		Ω
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V		0.9	1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=50V,V_{GS}=10V I_D=20A		87		nC
Gate-Source Charge	Q_{gs}			22		
Gate-Drain Charge	Q_{gd}			21		
Input Capacitance	C_{iss}	V_{DS}=50V,V_{GS}=0V f=1MHz		5995		pF
Output Capacitance	C_{oss}			923		
Reverse Transfer Capacitance	C_{rss}			13.8		
Turn-On Time	$t_{d(on)}$	V_{DD}=50V,V_{GS}=10V I_D=20A, R_G=10Ω		24		nS
	t_r			18		
Turn-Off Time	$t_{d(off)}$			36		
	t_f			9		

TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

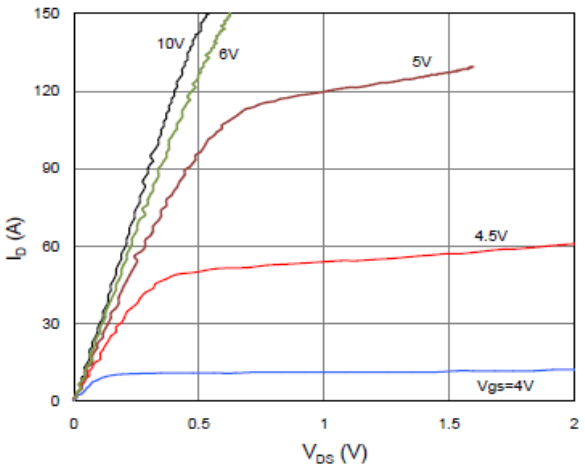


Figure 2. On-Resistance vs. Gate-Source Voltage

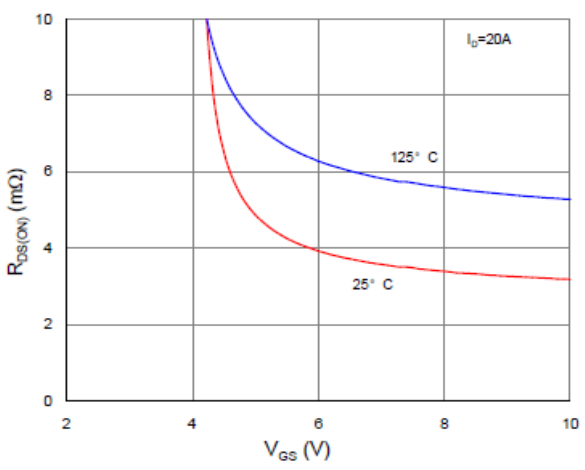


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

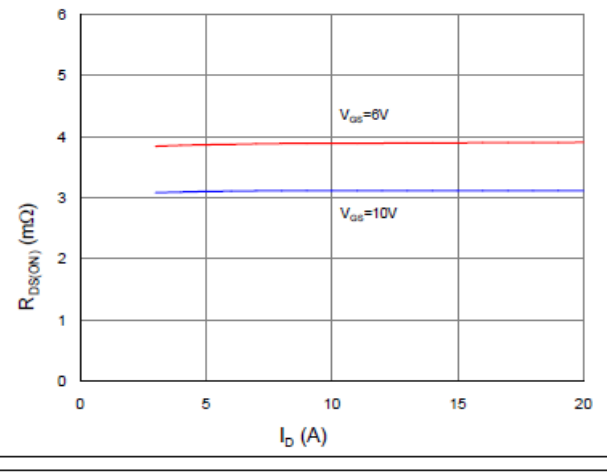


Figure 4. Normalized On-Resistance vs. Junction Temperature

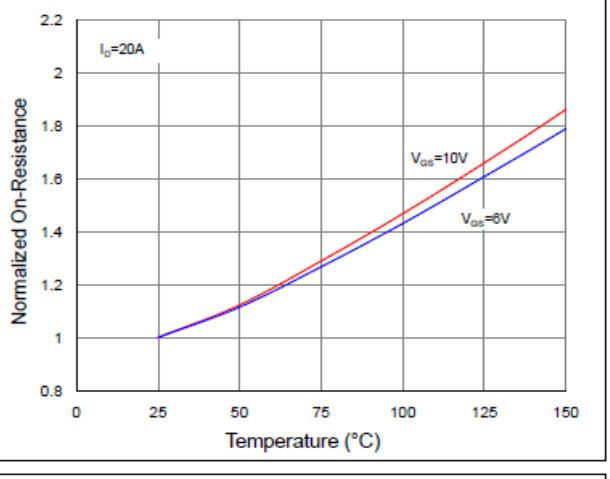


Figure 5. Typical Transfer Characteristics

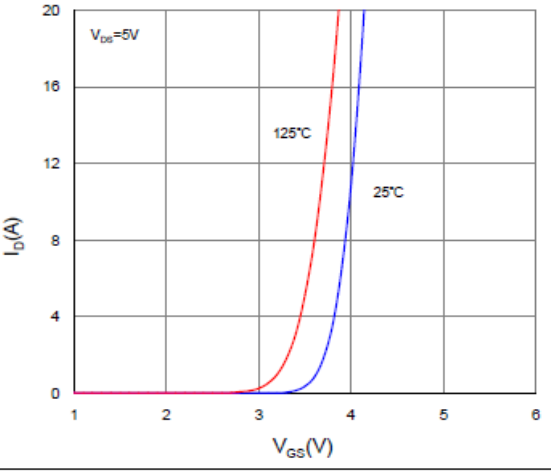
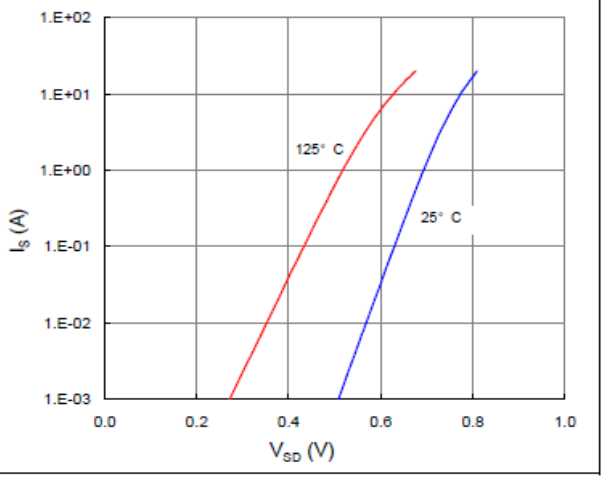


Figure 6. Typical Source-Drain Diode Forward Voltage



TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

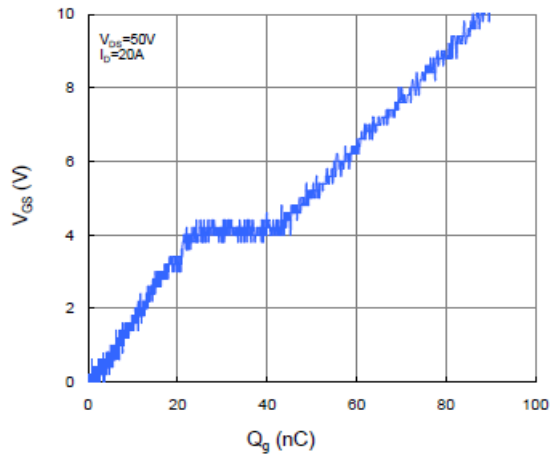


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

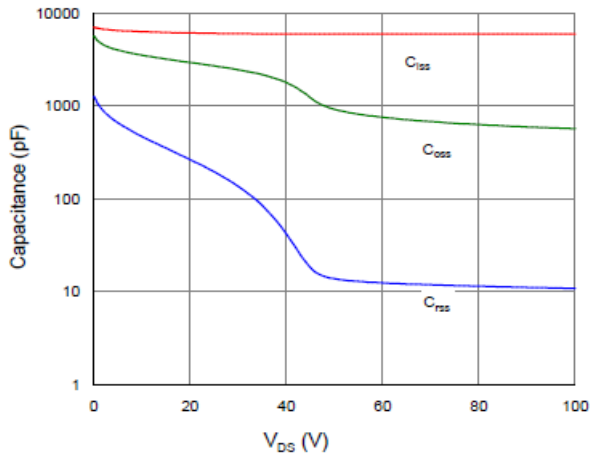


Figure 9. Maximum Safe Operating Area

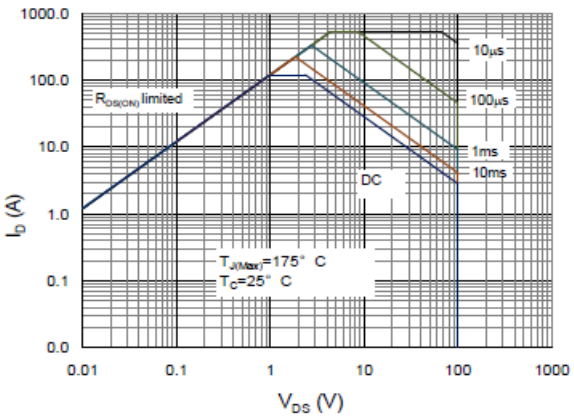


Figure 10. Maximun Drain Current vs. Case Temperature

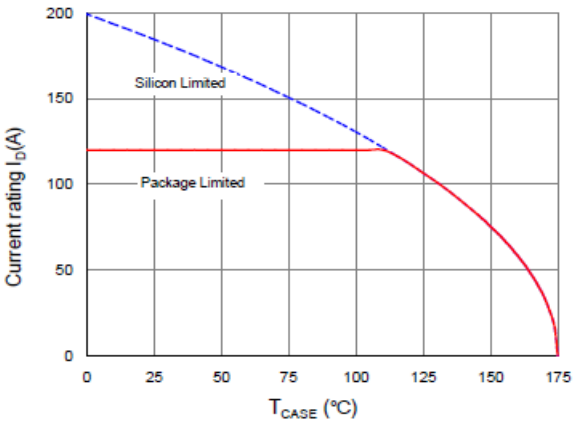
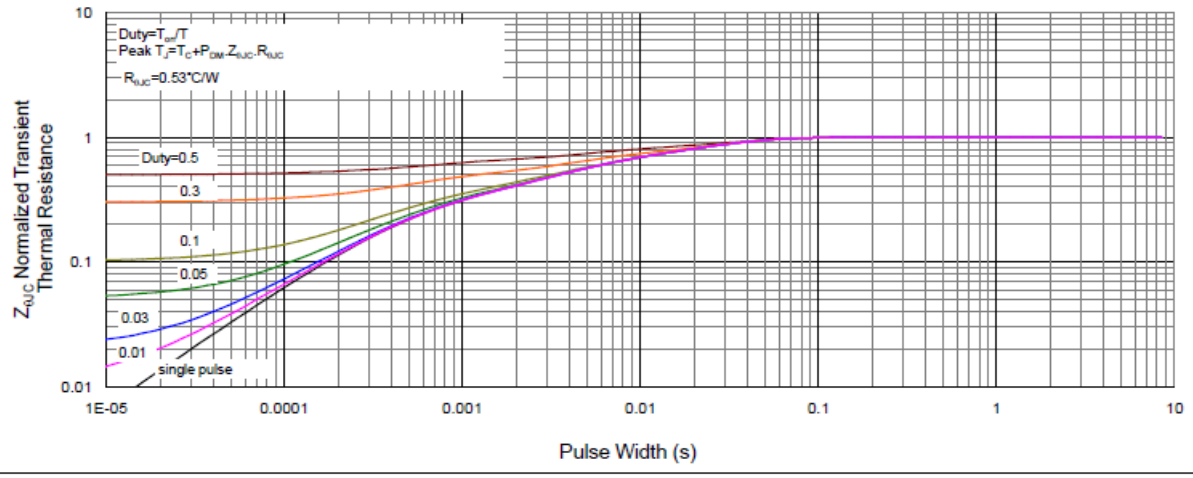


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case



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