



SPN2342W

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN2342W is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

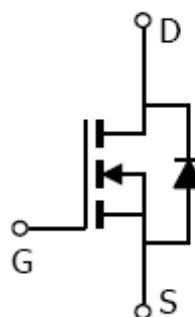
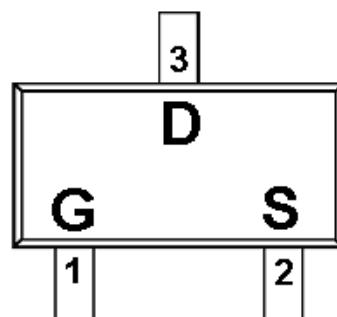
FEATURES

- ◆ 20V/4.0A,R_{DS(ON)}=35mΩ@V_{GS}=4.5V
- ◆ 20V/3.0A,R_{DS(ON)}=40mΩ@V_{GS}=2.5V
- ◆ 20V/2.0A,R_{DS(ON)}=55mΩ@V_{GS}=1.8V
- ◆ Super high density cell design for extremely low R_{DS(ON)}
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-23 package design

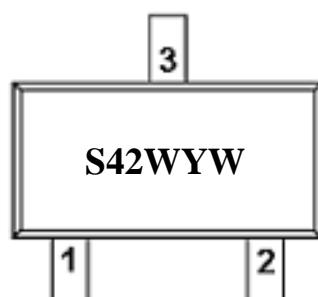
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION(SOT-23)



PART MARKING



Y : Year Code
W : Week Code



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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN2342WS23RGB	SOT-23	S42W

- ※ Week Code : A ~ Z(1 ~ 26) ; a ~ z(27 ~ 52)
- ※ SPN2342WS23RGB : Tape Reel ; Pb – Free ; Halogen – Free

ABSOULTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V _{DSS}	20	V	
Gate –Source Voltage	V _{GSS}	±12	V	
Continuous Drain Current(T _J =150°C)	TA=25°C	6.0	A	
	TA=70°C			
Pulsed Drain Current	I _{DM}	24	A	
Power Dissipation	T _A =25°C	P _D	1.4	W
Operating Junction Temperature	T _J	-55/150	°C	
Storage Temperature Range	T _{STG}	-55/150	°C	
Thermal Resistance-Junction to Ambient	R _{θJA}	90	°C/W	



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ELECTRICAL CHARACTERISTICS

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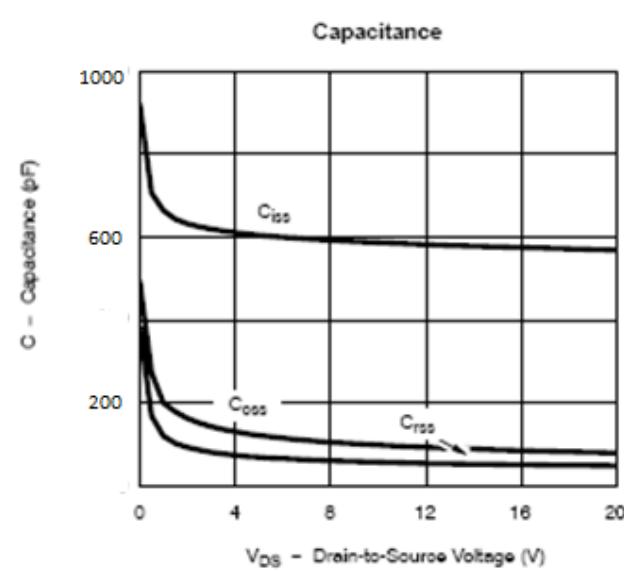
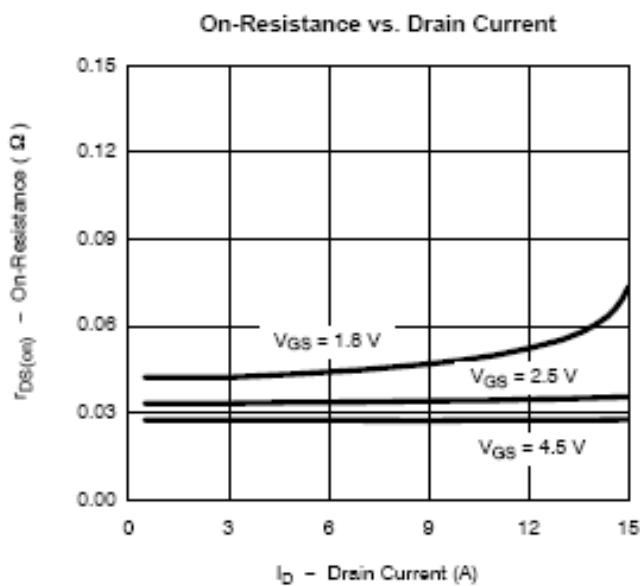
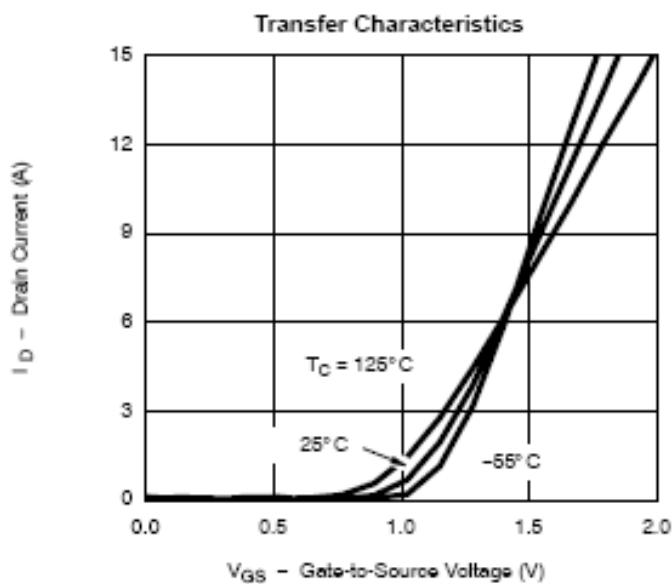
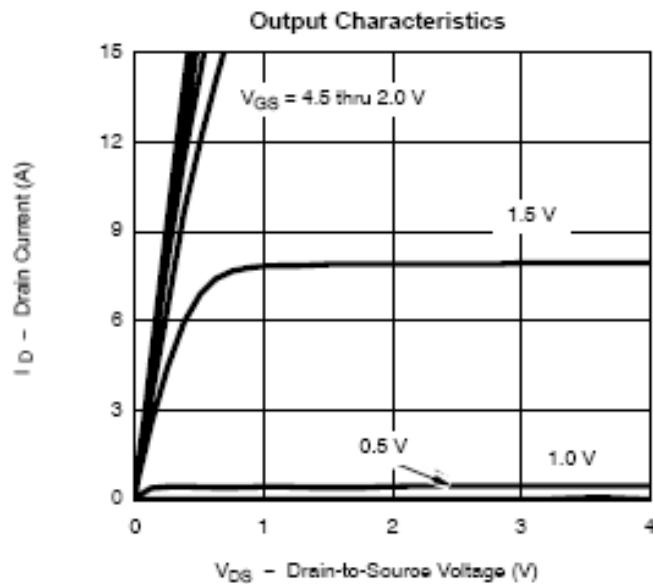
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, ID=250uA	20			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , ID=250uA	0.4		1.0	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±12V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =16V, V _{GS} =0V			1	uA
		V _{DS} =16V, V _{GS} =0V T _J =55°C			10	
On-State Drain Current	I _{D(on)}	V _{DS} ≥5V, V _{GS} =4.5V	6			A
Drain-Source On-Resistance	R _{DSS(on)}	V _{GS} = 4.5V, ID=4.0A		25	35	mΩ
		V _{GS} = 2.5V, ID=3.0A		30	40	
		V _{GS} = 1.8V, ID=2.0A		42	55	
Forward Transconductance	g _{fs}	V _{DS} =10V, ID=3.0A		6.5		S
Diode Forward Voltage	V _{SD}	I _S =1.0A, V _{GS} =0V		0.8		V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =10V, V _{GS} =4.5V ID=4.0A		7.8	11	nC
Gate-Source Charge	Q _{gs}			1		
Gate-Drain Charge	Q _{gd}			2.4		
Input Capacitance	C _{iss}	V _{DS} =10V, V _{GS} =0V f=1MHz		600		pF
Output Capacitance	C _{oss}			60		
Reverse Transfer Capacitance	C _{rss}			34		
Turn-On Time	t _{d(on)}	V _{DD} =10V, ID=1.0A V _{GEN} =4.5V, R _G =25Ω		4.1	8	nS
	t _r			11.5	22	
Turn-Off Time	t _{d(off)}			24	45	
	t _f			7.6	14	



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TYPICAL CHARACTERISTICS

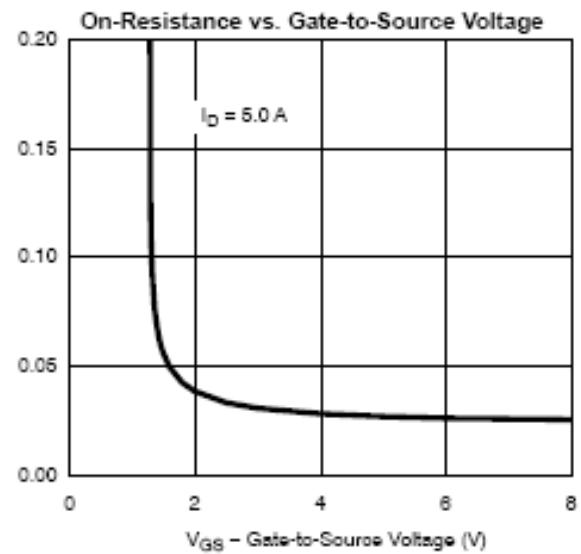
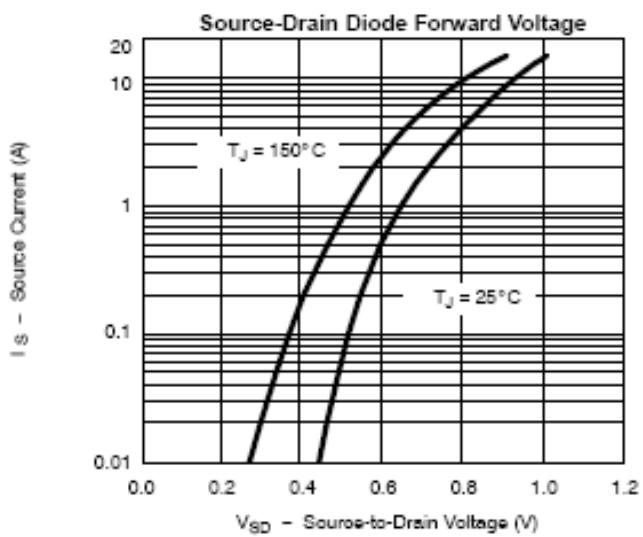
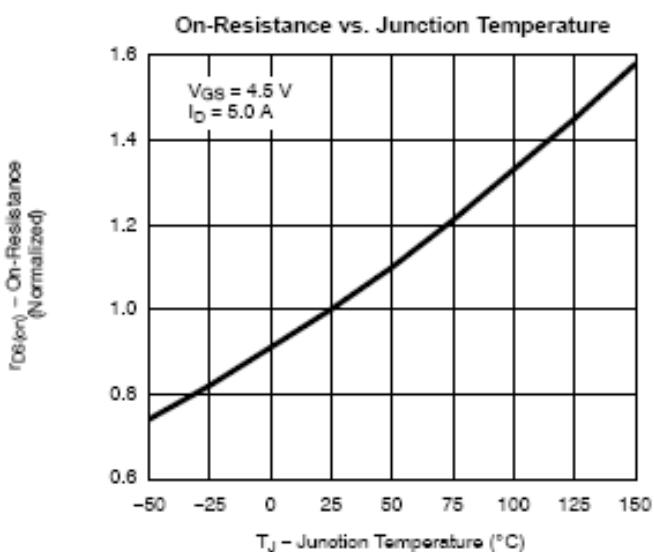
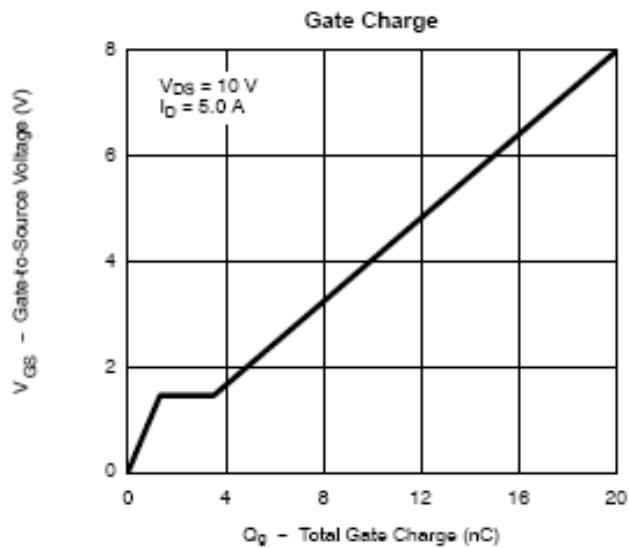




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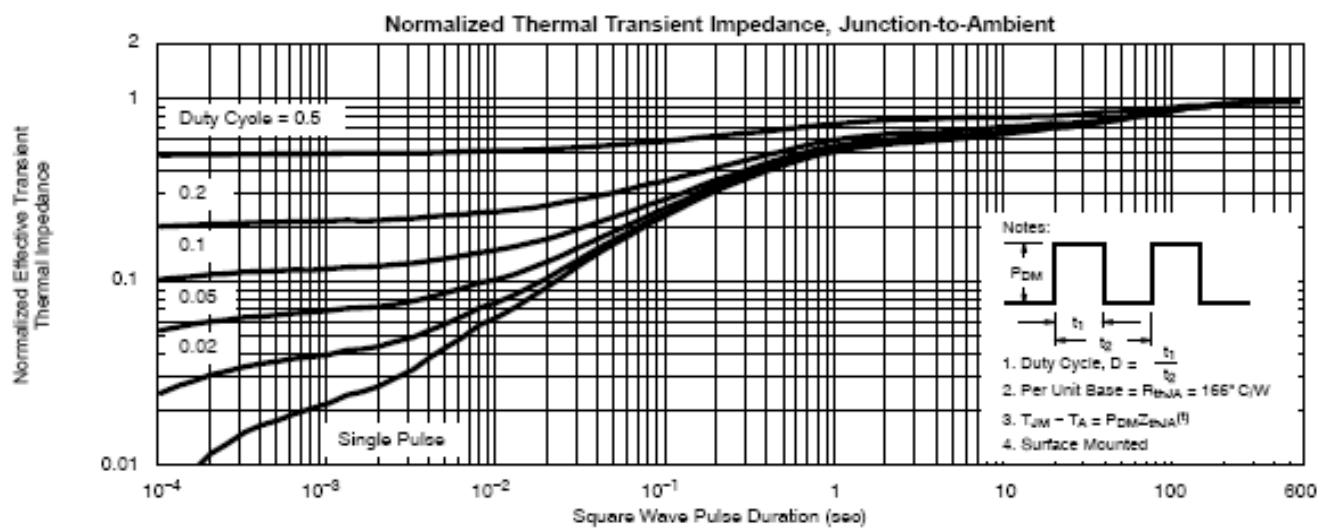
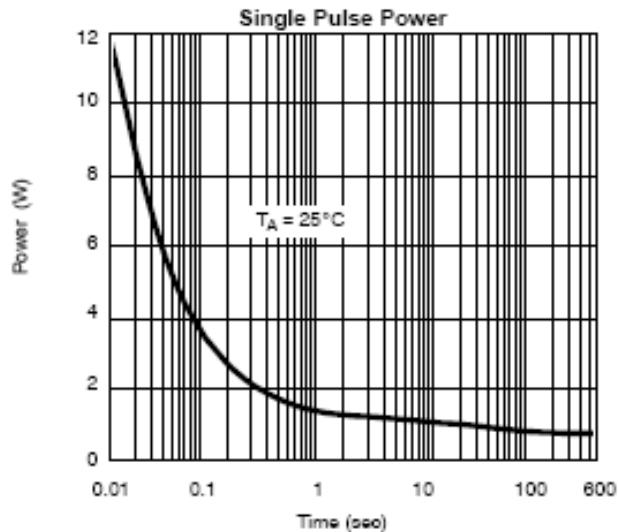
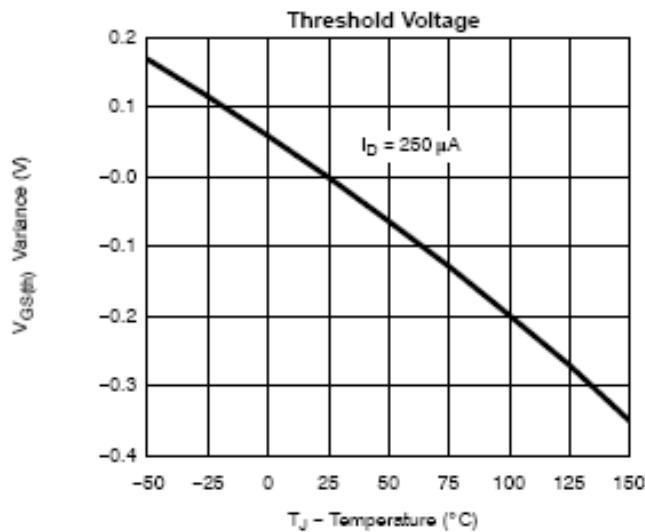




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TYPICAL CHARACTERISTICS





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