SPN3004
N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN3004 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

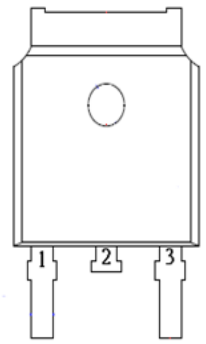
APPLICATIONS

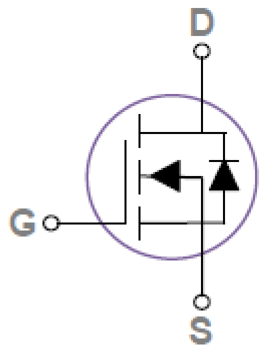
- MB/VGA/Vcore
- POL Applications
- SMPS 2nd SR
- High Frequency Synchronous Buck Converter
- DC/DC Power System
- Load Switch

FEATURES

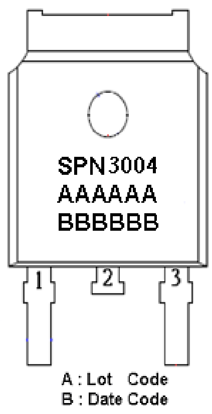
- 30V/96A,$R_{DS(ON)}$=4.2mΩ@V_{GS}=10V
- 30V/96A,$R_{DS(ON)}$=6.0mΩ@V_{GS}=4.5V
- Super high density cell design for extremely low R_{DS} (ON)
- Exceptional on-resistance and maximum DC current capability
- TO-252-2L package design

PIN CONFIGURATION(TO-252-2L)





PART MARKING



SPN3004
N-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN3004T252RGB	TO-252-2L	SPN3004

※ SPN3004T252RGB : Tape Reel ; Pb – Free; Halogen - Free

ABSOULTE MAXIMUM RATINGS

(T_A=25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	30	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(T_J=150°C)	T_A=25°C	I_D	96	A
	T_A=100℃		68	
Pulsed Drain Current		I_{DM}	192	A
Avalanche Current		I_{AS}	53.8	A
Single Pulse Avalanche Energy		EAS	317	mJ
Power Dissipation	T_A=25°C	P_D	93	W
Operating Junction Temperature		T_J	-55/150	°C
Storage Temperature Range		T_{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	62	°C/W

ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250uA	30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_{DS}=250uA	1.2	1.6	2.5	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=24V,V_{GS}=0V, T_J=25℃			1	uA
		V_{DS}=24V,V_{GS}=0V, T_J=125℃			10	uA
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V, ID=30A		3.8	4.2	mΩ
		V_{GS}=4.5V, ID=15A		5.2	6.0	mΩ
Forward Transconductance	gfs	V_{DS}=10V, I_D=6A		12		S
Diode Forward Voltage	V_{SD}	I_F=1A,V_{GS}=0V			1	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=15V,V_{GS}=4.5V, I_D =12A		24	34	nC
Gate-Source Charge	Q_{gs}			4.2	6	nC
Gate-Drain Charge	Q_{gd}			13	18	nC
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V, F=1MHz		2200	3190	pF
Output Capacitance	C_{oss}			280	405	pF
Reverse Transfer Capacitance	C_{rss}			177	255	pF
Turn-On Time	$t_{d(on)}$	(V_{DD}=15V,I_D=15A, V_{GEN}=10V,R_G=3.3Ω)		12.6	24	nS
	t_r			19.5	37	nS
Turn-Off Time	$t_{d(off)}$			42.8	81	nS
	t_f			13.2	25	nS

TYPICAL CHARACTERISTICS

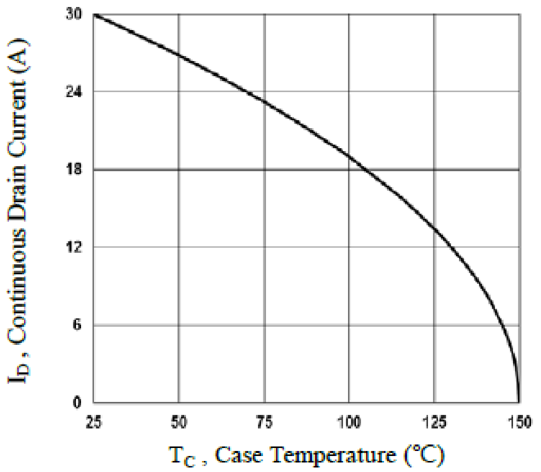


Fig.1 Continuous Drain Current vs. T_C

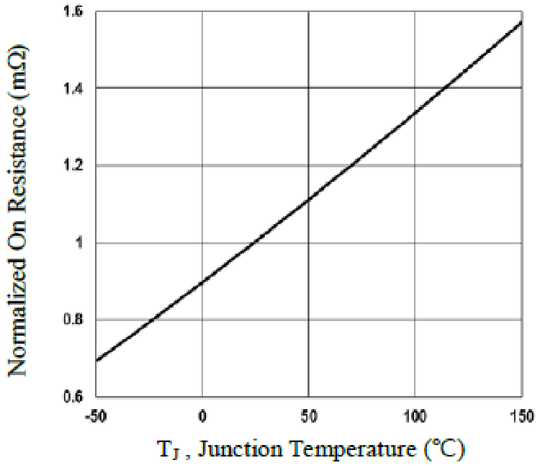


Fig.2 Normalized RDSON vs. T_J

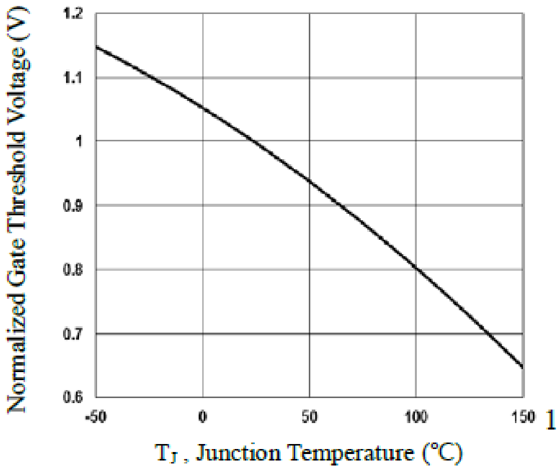


Fig.3 Normalized V_{th} vs. T_J

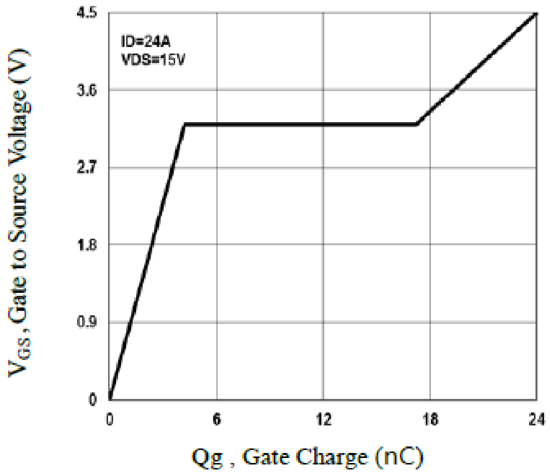


Fig.4 Gate Charge Waveform

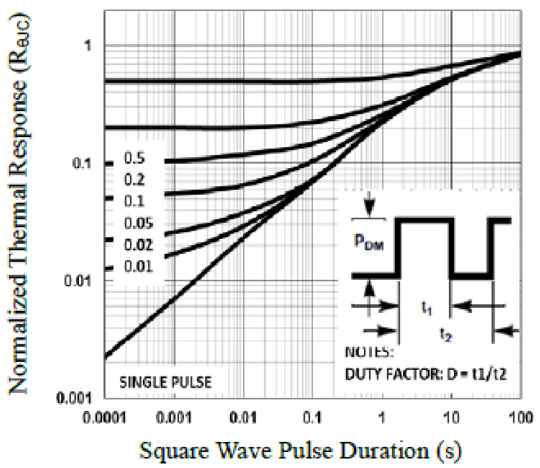


Fig.5 Normalized Transient Impedance

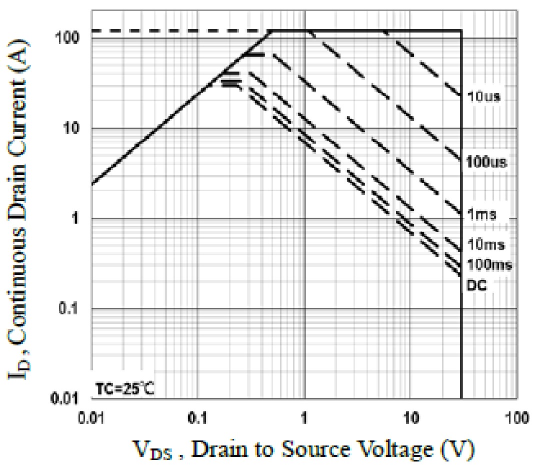


Fig.6 Maximum Safe Operation Area

TYPICAL CHARACTERISTICS

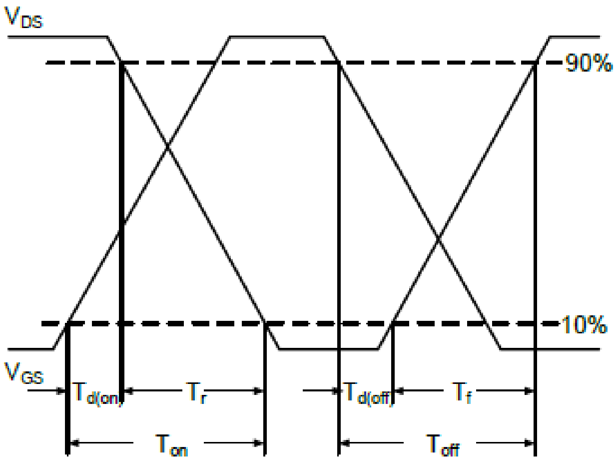


Fig.7 Switching Time Waveform

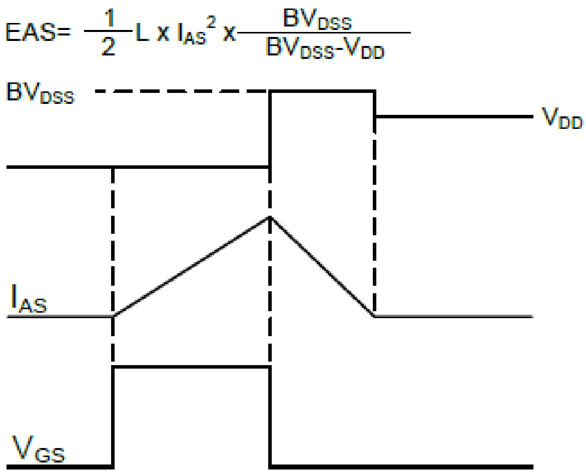


Fig.8 EAS Waveform

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