SPN30T25
N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN30T25 is the N-Channel enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. The SPN30T25 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

APPLICATIONS

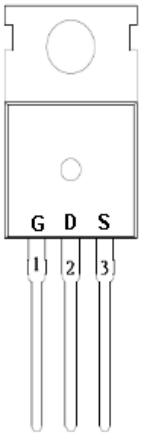
- DC/DC Converter
- Load Switch
- SMPS Secondary Side Synchronous Rectifier
- Motor Control
- Power Tool

FEATURES

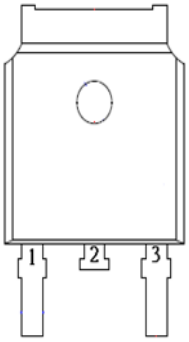
- 250V/29A,$R_{DS(ON)}$=64mΩ@V_{GS}=10V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-220-3L/TO-252-2L/PPAK5x6-8L package design

PIN CONFIGURATION

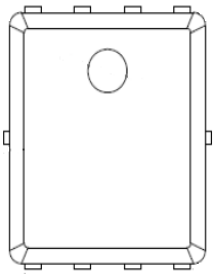
TO-220-3L

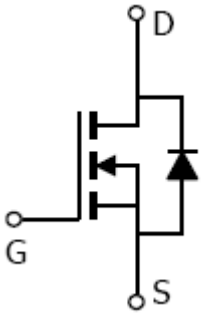


TO-252-2L



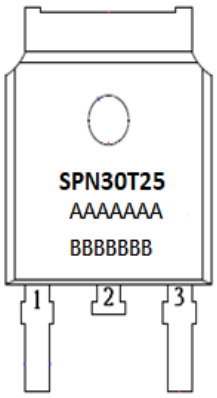
PPAK5x6-8L



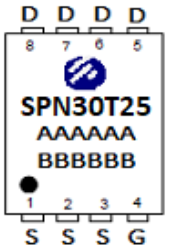


PART MARKING

A : Lot Code
B : Date Code



A : Lot Code
B : Date Code



A : Lot Code
B : Date Code
(YY / MM / DD)

SPN30T25
N-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN30T25T220TGB	TO-220-3L	SPN30T25
SPN30T25T252RGB	TO-252-2L	SPN30T25
SPN30T25DN8RGB	PPAK5x6-8L	SPN30T25

※ SPN30T25T220TGB : Tube ; Pb – Free ; Halogen – Free

※ SPN30T25T252RGB : Tape&Reel ; Pb – Free ; Halogen - Free

※ SPN30T25DN8RGB : Tape Reel ; Pb – Free ; Halogen - Free

SPN30T25
N-Channel Enhancement Mode MOSFET

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	250	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current (Silicon Limited)	T_C=25℃	I_D	29	A
	T_C=100℃		18	
Pulsed Drain Current		I_{DM}	110	A
Single Pulse Avalanche Energy (T_C=25℃, L=1mH.)		E_{AS}	112	mJ
Power Dissipation @ Tc=25℃	TO-220	P_D	104	W
Power Dissipation @ Tc=25℃	TO-252		93	
Power Dissipation @ Tc=25℃	PPAK5x6		83	
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Case (TO-220)		$R_{\theta JC}$	1.2	℃/W
Thermal Resistance-Junction to Case (TO-252)		$R_{\theta JC}$	1.35	℃/W
Thermal Resistance-Junction to Case (PPAK5x6)		$R_{\theta JC}$	1.5	℃/W

Note :

The maximum current rating is package limited at 120A for TO-220-3L
The maximum current rating is package limited at 70A for TO-252-2L
The maximum current rating is package limited at 80A for PPAK5x6-8L

ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	250			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	2	3	4	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=200V,V_{GS}=0V			1	uA
		V_{DS}=200V,V_{GS}=0V, T_J=100℃			100	
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=10A		50	64	mΩ
Forward Transconductance	gfs	V_{DS}=5V,I_D=10A		31		S
Gate resistance	Rg	V_{DS} open ,V_{GS}=0V f=1MHz		4.4		Ω
Diode Forward Voltage	V_{SD}	I_S=10A,V_{GS}=0V		0.9	1.2	V
Dynamic						
Total Gate Charge	Qg	V_{DS}=125V,V_{GS}=10V I_D=10A		20		nC
Gate-Source Charge	Q_{gs}			7		
Gate-Drain Charge	Q_{gd}			3		
Input Capacitance	C_{iss}	V_{DS}=100V,V_{GS}=0V f=1MHz		1584		pF
Output Capacitance	C_{oss}			104		
Reverse Transfer Capacitance	C_{rss}			7.6		
Turn-On Time	$t_{d(on)}$	V_{DD}=125V, I_D=10A,V_{GS}=10V R_G=10Ω		13		nS
	t_r			18		
Turn-Off Time	$t_{d(off)}$			25		
	t_f			10		

TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

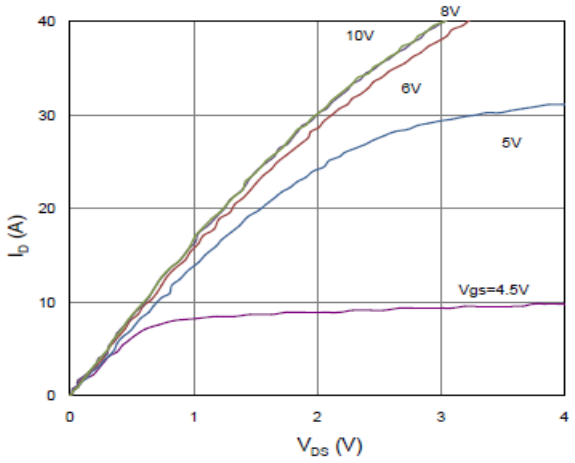


Figure 2. On-Resistance vs. Gate-Source Voltage

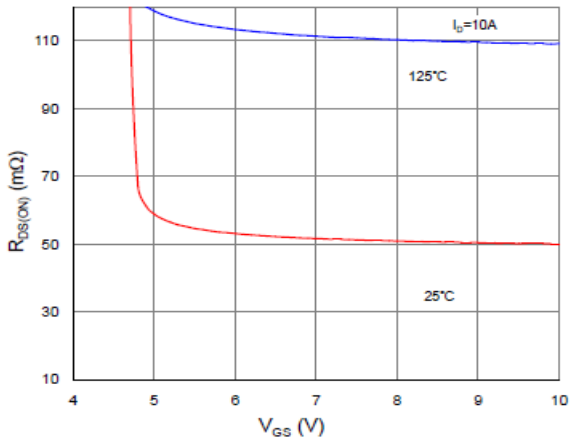


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

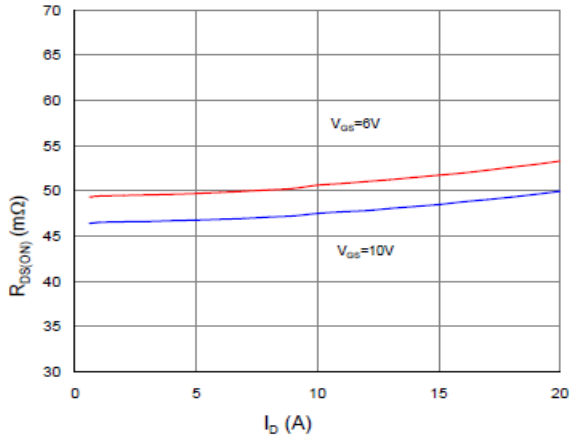


Figure 4. Normalized On-Resistance vs. Junction Temperature

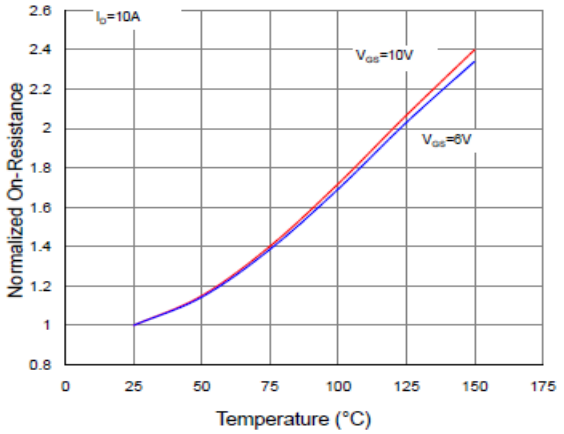


Figure 5. Typical Transfer Characteristics

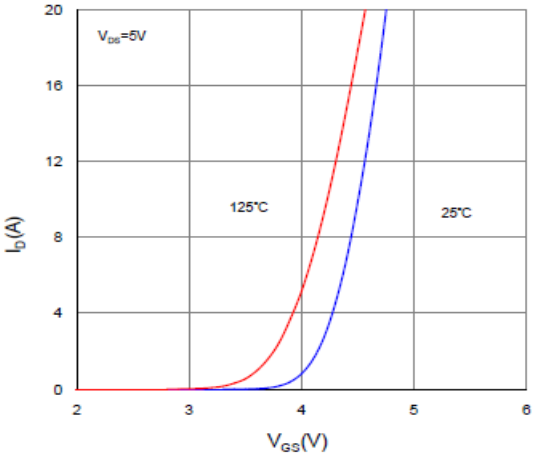
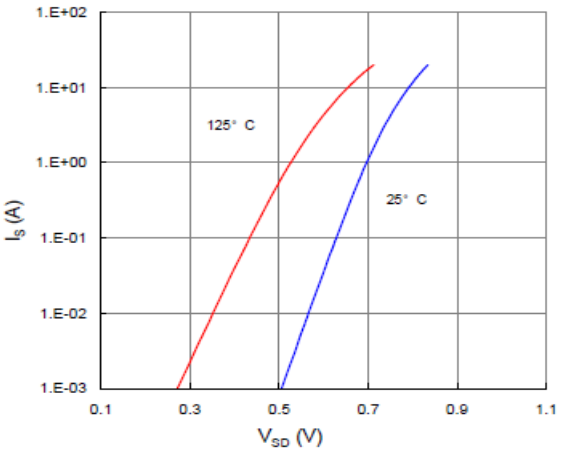


Figure 6. Typical Source-Drain Diode Forward Voltage



TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

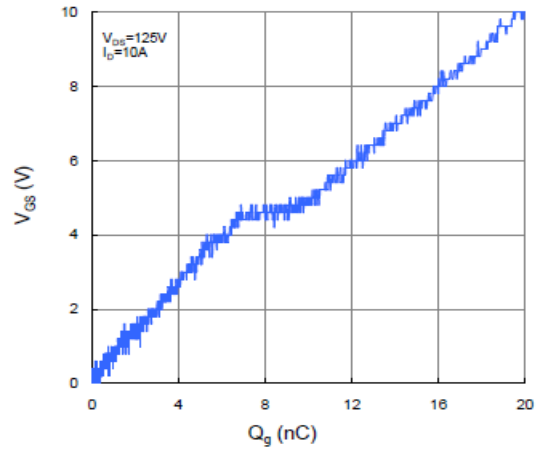


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

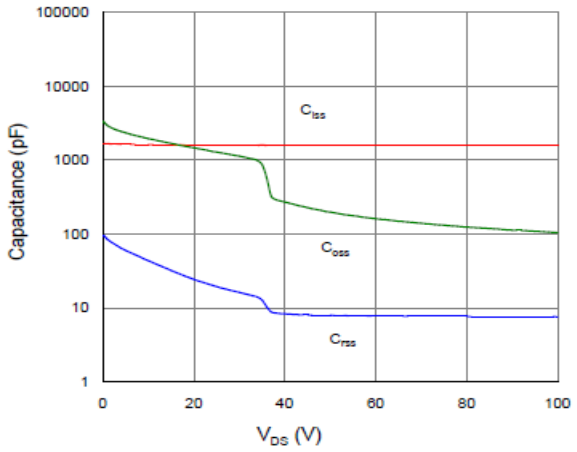


Figure 9. Maximum Safe Operating Area

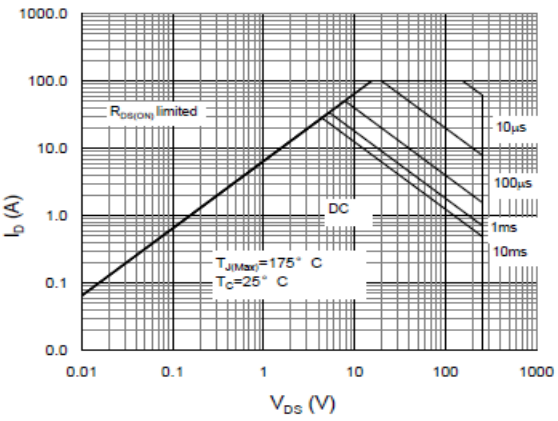


Figure 10. Maximun Drain Current vs. Case Temperature

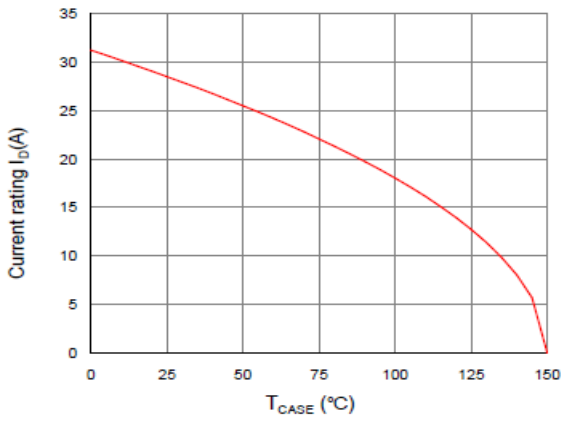
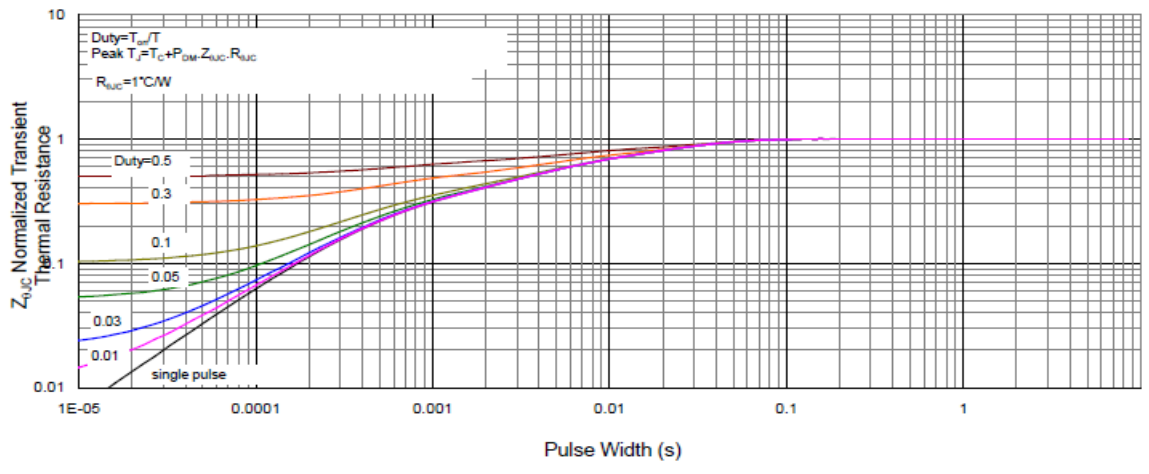


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case



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SYNC Power Corporation
7F-2, No.3-1, Park Street
NanKang District (NKSP), Taipei, Taiwan 115
Phone: 886-2-2655-8178
Fax: 886-2-2655-8468
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