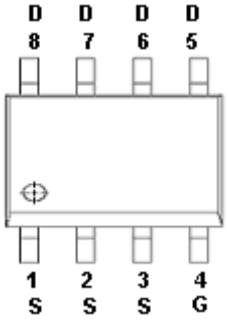
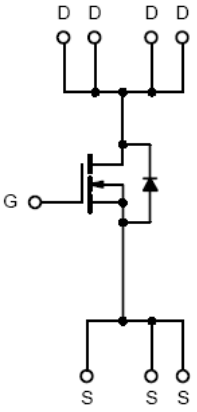
SPN4814A
N-Channel Enhancement Mode MOSFET

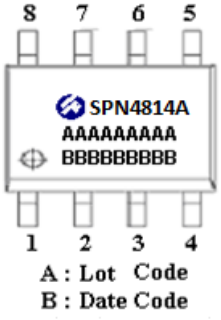
DESCRIPTION
The SPN4814A is the N-Channel enhancement mode power field effect transistors are produced using high cell density DMOS trench technology.
This high density process is especially tailored to minimize on-state resistance.
These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching.

APPLICATIONS
- DC/DC Converter
- Load Switch
- Synchronous Buck Converter
- SMPS Secondary Side Synchronous Rectifier
- Power Tool
- Motor Control

FEATURES
- 100V/20A,$R_{DS(ON)}$=10.5mΩ@V_{GS}=10V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP–8 package design

PIN CONFIGURATION(SOP–8)




PART MARKING


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PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN4814AS8RGB	SOP-8	SPN4814A

※ SPN4814AS8RGB : 13" Tape Reel ; Pb – Free ; Halogen – Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(T_J=150℃)	T_C=25℃	I_D	13	A
	T_C=100℃		8	
Pulsed Drain Current		I_{DM}	120	A
Avalanche Energy, Single Pulse (L=0.1mH , Tc=25℃)		E_{AS}	31	mJ
Power Dissipation	T_C=25℃	P_D	3.1	W
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Case		$R_{\theta JC}$	0.85	℃/W
Thermal Resistance-Junction to Ambient (steady state)		$R_{\theta JA}$	75	

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ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	2.0	3.0	4.0	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=80V,V_{GS}=0V T_J=25℃			1	uA
		V_{DS}=80V,V_{GS}=0V T_J=100℃			100	
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=20A		9.4	10.5	mΩ
Forward Transconductance	gfs	V_{DS}=5V,I_D=20A		39		S
Gate Resistance	R_G	V_{GS}=0V,V_{DS}=Open, f=1MHz		1.5		Ω
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V		0.9	1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=50V,V_{GS}=10V I_D=20A		23.0		nC
Gate-Source Charge	Q_{gs}			5.5		
Gate-Drain Charge	Q_{gd}			6.5		
Input Capacitance	C_{iss}	V_{DS}=50V,V_{GS}=0V f=1MHz		1326		pF
Output Capacitance	C_{oss}			262		
Reverse Transfer Capacitance	C_{rss}			7.7		
Turn-On Time	$t_{d(on)}$	V_{DD}=50V, I_D=20A,V_{GS}=10V R_G=10Ω		6		nS
	t_r			3		
Turn-Off Time	$t_{d(off)}$			17		
	t_f			4		

TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

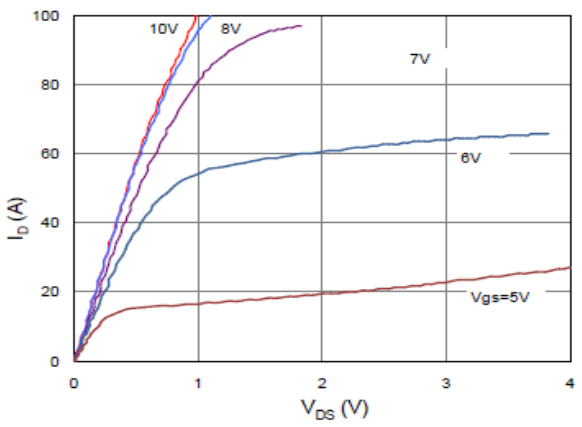


Figure 2. On-Resistance vs. Gate-Source Voltage

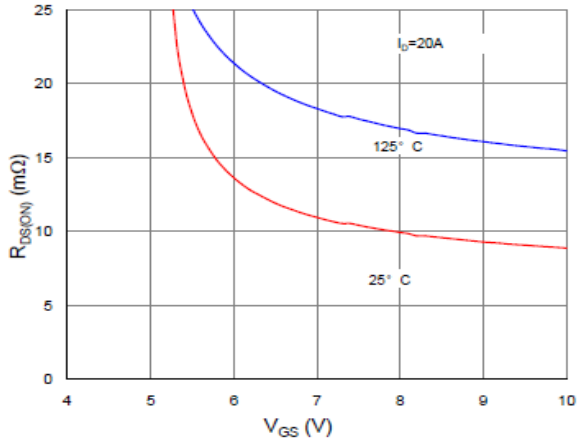


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

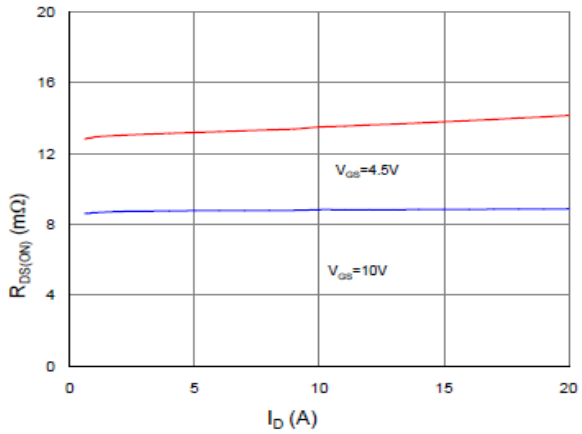


Figure 4. Normalized On-Resistance vs. Junction Temperature

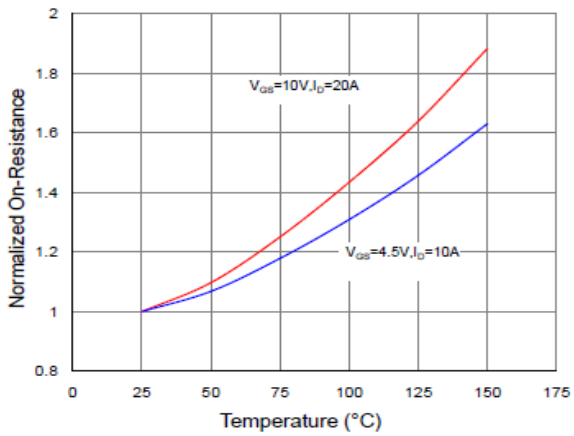


Figure 5. Typical Transfer Characteristics

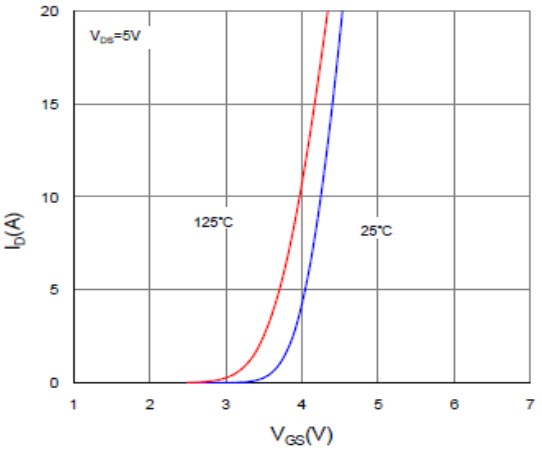
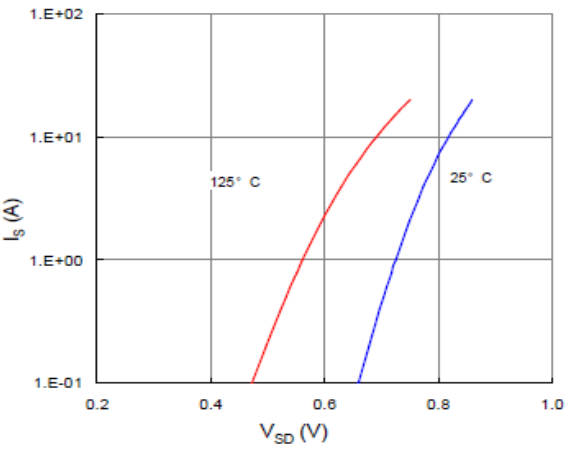


Figure 6. Typical Source-Drain Diode Forward Voltage



TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

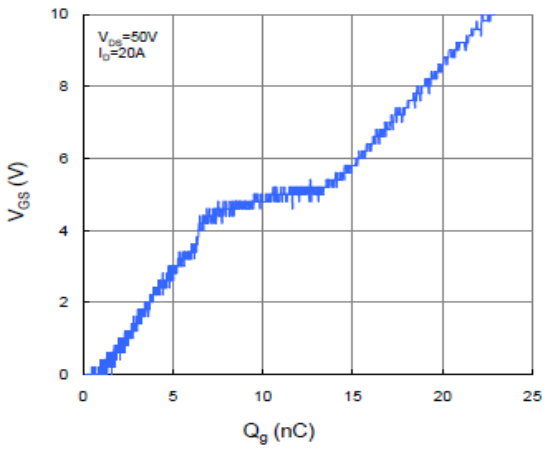


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

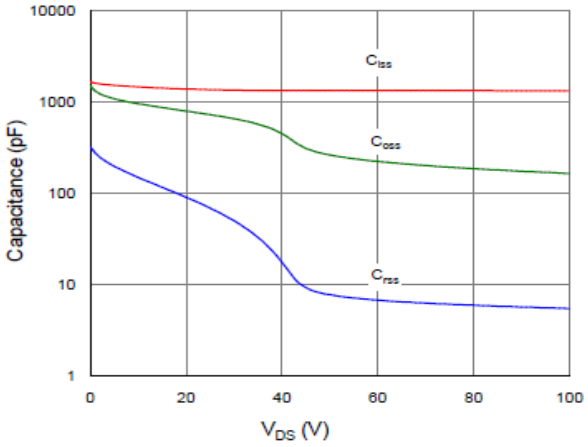


Figure 9. Maximum Safe Operating Area

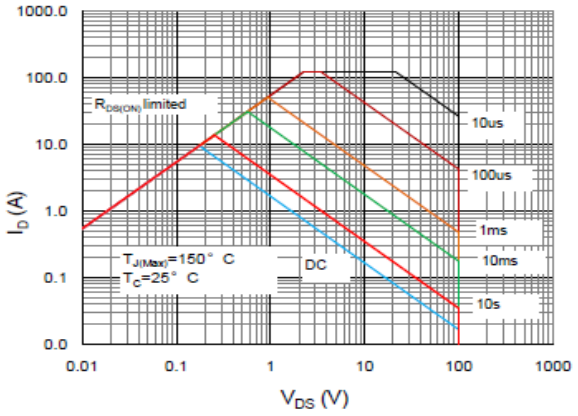


Figure 10. Maximun Drain Current vs. Case Temperature

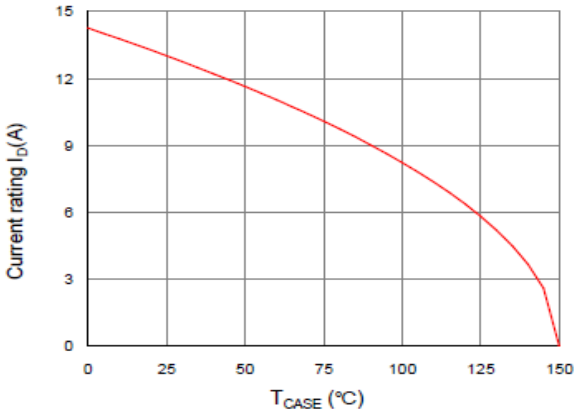
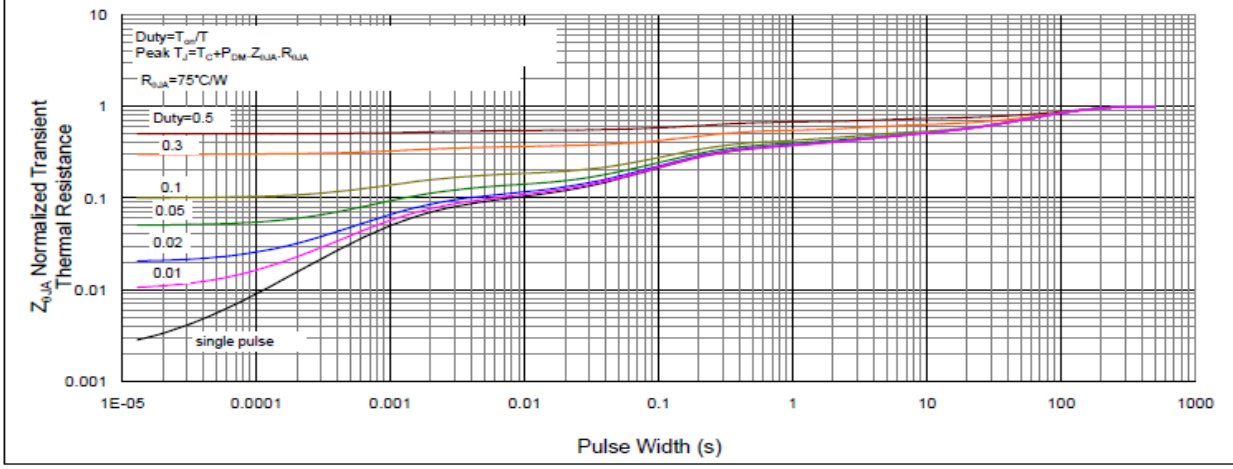


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case



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